



JEITA/EDA-TC/STD-SC/ SystemVerilog Task Group

Mar. 4th 2004



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Panasonic

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- Outline -

- JEITA / Organization and Management
- EDA-TC / Current major activities
- SystemVerilog Task Group activities
- SystemVerilog Task Group members

JEITA : Japan Electronics and Information Technology Industries Association
(URL <http://www.jeita.or.jp>)



JEITA / Organization and Management

Japan Electronics and Information Technology Industries Association

JEITA was inaugurated on November 1, 2000, merger of JEIDA+EIAJ

- Information System Committee Group
- Personal Information Committee Group
- Digital Home Appliances Committee Group
- Industrial Equipment and Social System Committee Group
- Electronics Components Committee Group

Electronic Devices Committee Group

- Electronic Display Devices Committee
- Global Warming Countermeasures Committee

Semiconductors Committee

- Marketing Committee
- Road Map Committee

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EDA Technical Committee(EDA-TC)

◆ EDA Technical Committee was formed to handle EDIF 2.0 standard as one of technical committees in JEITA (former EIAJ) in April 1990.



EDA-TC / Current major activities

EDA Technical Committee(EDA-TC)

1. Standardization Subcommittee(STD-subcom.)

- To contribute EDA related standardization efforts by supporting EDA standards related groups and organizations such as Accellera, IEEE/DASC, IEC/TC93.

(1) SystemVerilog TaskGroup

(2) SystemC TaskGroup

2. DMD (Deci-Micron Design) Study Group

- To investigate and propose solutions for technical issues raised by very deep sub-micron (0.10um and below) SOC design

3. eD&S Fair Executive Committee

- To organize and support events to promote and encourage EDA techno and standards. To sponsor the "eD&S Fair 2003"



SystemVerilog Task Group activities

- Members: Experts from Academia, Semiconductor industries
- Chair : K.Hamaguchi(Panasonic)
- Activities :
 - ✓ organized in October, 2003
 - ✓ meetings is held in 2003
10/17, 11/28-29, 2/12, next 3/15
 - ✓ Studying SystemVerilog Now!
 - ✓ Review V3.1a Draft4 and
feedback IssueReport to Accellera or IEEE WG by Q4/2004
 - ✓ Participate in balloting
 - ✓ Delegation to DVCon and Accellera meeting in March, 2004
 - ✓ Planning to attend panel discussion about System Level
Design Language at DA symposium in Japan in July, 2004



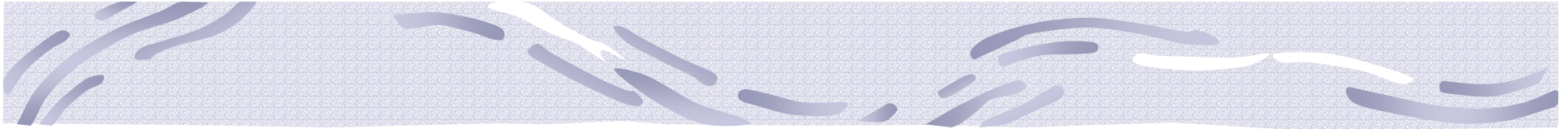
SystemVerilog Task Group Member

- ◆ Chair : Kasumi Hamaguchi (Panasonic)
ViceChair : Takaaki Akashi (Nihon Synopsys)

Cadence Design Systems,Japan
FUJITSU LIMITED
Renesas Technology Corp.
Mentor Graphics Japan Co., Ltd.
Matsushita Electric Industrial Co.,Ltd.
Nihon Synopsys Co.,Ltd
Oki Electric Industry Co.,Ltd.
Toshiba Corporation

Kenji Goto
Yukio Chiwata
Yoshio Takamine
Wataru Yamamoto
Kasumi Hamaguchi
Takaaki Akashi
Takeharu Yui
Takehiko Tsuchiya





Thank You!



History of EDA-TC

- ◆ EDA Technical Committee was formed to handle EDIF 2.0 standard as one of technical committees in JEITA (former EIAJ) in April 1990 .
- ◆ The committee is an only organization to handle EDA technology standards in Japan which semiconductor companies, EDA vendors and Academia
- ◆ The committee has been contributed EDA standardization activities such as EDIF, VHDL, Verilog, VITAL, AHDL, DPC, --- .
- ◆ And also sponsored Electronic Design & Solution Fair (eD&S Fair) in conjunction with ASP-DAC.



New organization structure in Japan

- JEITA EDA-TC will be strongly involved to manage WG2 activities in TC93 JPN NC such as sending a chairperson and experts

