



SystemVerilog 3.1a SV-AC Update 27 February 2004

Faisal Haque (Cisco) – Chairman
Arif Samad(Synopsys) – Co-Chairman



Status

- Extensions
 - All extensions are in LRM and have been reviewed
 - **Assume, accessing local variables, sampling local variables, NBA for assertions, access to sampled values, unbounded range arguments, \$past with enabling expression, recursive properties, clock flow, generalized implication, property conjunction and disjunction, if-else, property instance, property negation, negated booleans**
- Errata
 - Several errata have been identified and closed
- Committee members have reviewed relevant sections of the LRM
- Committee Membership
 - Active participants from Cadence, Cisco, Intel, LSI, Motorola, Novas, Sun Microsystems, Synopsys
 - 7 individuals have voting status
 - 6 companies have voting status

