

SystemVerilog 3.1a SV-BC Update 29 February 2004

Johny Srouji – Chairman Karen Pieper – Co-Chairman



Status

SystemVerilog

- Busy committee with 17 active participants and over 110 members on email reflector
- Overall, excellent progress in flushing design modeling issues in SV3.1a. Total of 177 issues were filed:
 - 146 (83%) have been addressed
 - 72 closed
 - 15 passed
 - 58 updated
 - 1 committed (separate compilation)
 - 31 (17%) issues are open or deferred
- Committee members reviewed design modeling sections of the LRM and checked for cross-references and index updates
- Plan to decide on the process for resolving current open Errata list