# SystemVerilog 3.1a
# SV-EC Update
# 27 February 2004

David Smith (Synopsys) – Chairman

Neil Korpusik (Sun Microsystems) – Co-Chairman

# Status

- Extensions
  - All extensions are in LRM and have been reviewed (multiple times for content):
    - Process control, Virtual Interfaces, Reacting to Assertions, RandCase, Stream Generation, Functional Coverage Goal Specification, Dynamic Queue Support, Pack/Unpack, Constraint Completion, Foreach, Coverage Event Control)
- Errata
  - 76 items have been identified and are closed
- Action Items
  - 58 Action items have been created and closed
  - 54 are closed
- Committee members reviewed all sections of the LRM, checked cross-references, did cross-section consistency checks, added to the glossary and index
- Committee Membership
  - Active participants from Cadence, Motorola, Mentor/Model Tech, Sun Microsystems, Sunburst Design, Sutherland HDL, and Synopsys
  - 10 individuals have voting status
  - 5 companies have voting status (IEEE participation is not up to date)

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# LRM Status

- Draft 1 Complete on 29 October 2003
- Draft 2 Complete on 15 December 2003
- Draft 3 Complete on 9 January 2003
- Draft 4 Complete on 31 January 2004
- Draft 5 Complete on 28 February 2004
  - 80 changes
  - Huge review cycle resulting in many editorial corrections
  - Small number of semantic clarifications and corrections in text and BNF
  - Small number of technical changes driven by committee review

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