Accellera Luncheon Seminar

Accellera Technical Committees

Sessions Plans

- Accellera technical team will present the slides.
- Questions and Answers:
  - The team will be available after the presentation is done on the floor.
  - Interactions will be done one on one on the floor.
  - Presentations will be available on the web for download within one day.

Accellera Seminar Agenda

- IEEE coordination and plan (Vassilios Gerousis, Infineon Technologies).
- PSL/SVA (Harry Foster, Jasper Design)
- SystemVerilog 3.1A users-based enhancement:
  - Testbench Enhancement (Neil Korpusik - Sun Microsystem)
  - Design Enhancement - (Matt Maidment - Intel)
  - DPI enhancement -- (Swapnajit Mittra - SGI)
  - Assertions Enhancement -- (Faisal Haque - CISCO)
- SV 3.1A Solidification (David Smith - Synopsys)