

P1076 Study Group: PAR supplement

1. Proposed Working Group Organization

The following is a proposed organization for the working group. This process is adapted from the Accellera VHDL working group that helped develop 1076-2008. The challenge of the working group is to organize the tasks to be done to engage those who are needed to participate without getting bogged down in details that do not concern them. The further challenge is to provide checks and balances to make sure the work that gets proposed and done is high value and matches the user driven expectation.

The proposed organization breaks the group into the below listed subgroups. Each subgroup will hold separate meetings to allow participants to choose the appropriate levels in which to participate.

Subgroup 1: Requirements Team

Who: All

Purpose: Develop and prioritize requirements.

Actions:

High priority requirements get forwarded to the proposals team.

Low priority requirements don't get WG authorization to go forward.

Subgroup 2: Proposals Team

Who: People who feel comfortable writing or reviewing one or more proposals

Purpose: Write proposals for implementation of requirements

Actions:

Champions volunteer to work on requirement.

If an enhancement does not get a champion, it does not go any further.

Internal review proposals before forwarding them to the next subgroup.

Subgroup 3: Proposal vs Requirements Review

Who: All (Requirements + Proposals team)

Purpose:

Verify that the proposals meet the requirements from the viewpoint of the requirements team.

Actions: Vote on proposals to make sure they address the requirements.

Subgroup 4: Write LRM changes

Who: LRM mechanics

Action: Write LRM language change specifications for the proposals.

Subgroup 5: LRM change vs. Proposal Review

Who: All (LRM + Proposals + ?Requirements?)

Purpose: Identify any differences in the proposal and the LRM change (if any).

Action: Vote to approve or disapprove differences in LRM change and proposals.

This organization is intended to facilitate having a both users and language experts involved in the language revision process. This is essential as when adding features that are intended to address a specific areas (such as DSP design) it is important to have experts in that area to comment - these people do not need to be VHDL language experts,

but instead are needed to request changes and review if the proposed change implementation meets their needs.

In the January 10, 2011 meeting, the study group approved passing this organization forward to the working group as its suggestion for working group organization.

2. Scope of Work

The following is a summary of the brain storming done by the study group both on the reflector and in the January 10 meeting. In the January 10, 2011 meeting, the study group approved passing these items to the 1076 working group as items to consider for the next revision:

- Review list of items not done by Accellera VHDL working group
- Coordinate with VHDL-AMS (1076.1)
 - Interfaces to spice models such as DACs, ...
 - Table driven modeling in AMS - generalization opportunities
 - Vector/matrix operations - generalization opportunities
- Extend type integer to have more than 32 bits.
- Bug fixes and updates to fixed/float packages.
- Make interfacing to other languages easy
 - Direct C calls
 - VHDL to SystemC TLM package/API
 - VHDL to SystemVerilog API
 - VHDL to Python, TCL, or other scripting languages
- Data structures (scoreboards, dynamic arrays, associative arrays, mailboxes, semaphores - syntax vs package based)
- Constrained Random
- Functional Coverage
- Transaction-level modeling
 - Simplify connections between models (interface object or other).
- OO/Classes
- Fork-join
- Designer Productivity Improvements
 - Extract simulation data into test data