Email This Letter

24 September 2004

Peter Ashenden
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P.O. Box 640
Stirling SA 5152
AUSTRALIA
peter@ashenden.com.au

Re: P1076 - Standard VHDL Language Reference Manual

Dear Peter:

I am pleased to inform you that on 23 September 2004 the IEEE-SA Standards Board approved the above referenced project until 31 December 2008. A copy of the file can be found on our website at http://standards.ieee.org/board/nes/projects/1076.pdf.

Now that your project has been approved, please forward a roster of participants involved in the development of this project. This request is in accordance with the IEEE-SA Operations Manual, Clause 5.1.2i under Duties of the Sponsor which states:

"Submit annually to the IEEE Standards Department an electronic roster of individuals participating on standards projects"

For your convenience, an Excel spreadsheet for your use has been posted on our website at http://standards.ieee.org/guides/par/roster.xls. Please forward this list to me via e-mail at j.haasz@ieee.org no later than 21 December 2004.

Please visit our website, IEEE Standards Development Online (http://standards.ieee.org/resources/development/index.html), for tools, forms and training to assist you in the standards development process. Also, we strongly recommend that a copy of your draft be sent to this office for review prior to the final vote by the working group to allow for a quick review by editorial staff before sponsor balloting begins.

If you should have any further questions, please contact me at 732-562-6367 or by email at j.haasz@ieee.org.

Sincerely,

Jodi Haasz
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International Stds Programs and Governance
Standards Activities
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PAR FORM

PAR Status: Revision PAR
PAR Approval Date: 2004-09-23
PAR Signature Page on File: Yes

1. Assigned Project Number: 1076

2. Sponsor Date of Request: 2004-08-24

3. Type of Document: Standard for

4. Title of Document:
Draft: Standard VHDL Language Reference Manual

5. Life Cycle: Full-Use

6. Type of Project:
6a. Is this an update to an existing PAR? No

6b. The Project is a: Revision of Std 1076-2002

7. Working Group Information:
Name of Working Group: VHDL Analysis and Standardization Group (VASG), a.k.a VHDL-200x Project
Approximate Number of Expected Working Group Members:30

8. Contact information for Working Group Chair:
Name of Working Group Chair: Stephen A Bailey
Telephone: 303-775-1655 **FAX:** 303-652-1578
Email: stephen@srbailey.com

9. Contact information for Co-Chair/Official Reporter, Project Editor or Document Custodian if different from the Working Group Chair:
Name of Co-Chair/Official Reporter, Project Editor or Document Custodian: Peter Ashenden
Telephone: +61883397532 **FAX:** +61883392616
Email: peter@ashenden.com.au

10. Contact information for Sponsoring Society or Standards Coordinating Committee:
Name of Sponsoring Society and Committee: Computer Society Design Automation
Name of Sponsoring Committee Chair: Peter Ashenden
Telephone: +61883397532 **FAX:** +61883392616
Email: peter@ashenden.com.au
Name of Liaison Rep. (if different from the Sponsor Chair):
Telephone: FAX:
Email:

Name of Co-Sponsoring Society and Committee:
Name of Co-Sponsoring Committee Chair:
Telephone: FAX:
Email:
Name of Liaison Rep. (if different from the Sponsor Chair):
Telephone: FAX:
Email:

11. The Type of ballot is: Individual Sponsor Ballot
Expected Date of Submission for Initial Sponsor Ballot: 2005-01-31

12. Fill in Projected Completion Date for Submittal to RevCom: 2005-06-30

Explanation for Modified PAR that completion date is being extended past the original four-year life of the PAR:

13. Scope of Proposed Project:

This project will revise and enhance the VHDL LRM by including a standard C language interface specification; specifications from previously separate, but related standards 1164, 1076.2 and 1076.3; and general language enhancements in the areas of design and verification of electronic systems.

Is the completion of this document contingent upon the completion of another document? No

14. Purpose of Proposed Project:

The VHDL language was defined for use in the design and documentation of electronics systems. It is being revised to incorporate capabilities that will improve the language's usefulness for its intended purpose as well as extend it to address design verification methodologies that have developed in industry. These new design and verification capabilities are required to ensure VHDL remains relevant and valuable for use in electronic systems design and verification. Incorporation of previously separate, but related standards, will simplify the maintenance of the specifications.

14a. Reason for the standardization project:

General language enhancements improve designer productivity by allowing the specification of models more efficiently or the ability to specify functionality that was previously not possible or impractical to specify in VHDL. Verification capabilities are needed to improve the quality of the designs and to address the significant and growing portion of the electronic system design schedule that is being spent in ensuring the design is functionally correct before manufacturing. These capabilities directly address productivity and quality. Additional capabilities are being added to facilitate standard interfaces for tool interoperability.

The stakeholders for this project are:
- Electronics Design Automation (EDA) tool vendors
- Digital IC and FPGA IP developers
- Digital IC and FPGA developers and manufacturers
- Digital and embedded system developers, manufacturers and integrators

15. Intellectual Property:

Has the sponsor reviewed the IEEE patent policy with the working group? Yes

Is the sponsor aware of copyrights relevant to this project? Yes

The working group has benefitted from technology donations from EDA companies. These donations have been accompanied by letters of donation with signatures of authorized officials from the donating companies.

Is the sponsor aware of trademarks relevant to this project? No

Is the sponsor aware of possible registration of objects or numbers due to this project? No

16. Are there other documents or projects with a similar scope? Yes

P1364 (Verilog): Standard for Verilog Hardware Description Language. There is significant overlap between the capabilities of the two languages. However, both have proven to be accepted in the marketplace with multiple tools supporting one or both languages and with many users that use one or both languages. P1647 Standard for the Functional Verification Language 'e': Some proposed language enhancements in the area of verification will overlap capabilities that may eventually be standardized through this working group. P1800 Standard for SystemVerilog: Unified Hardware Design, Specification and Verification Language. This is a proposed effort to extend the capabilities of Verilog. As the market needs better design and verification capabilities, it is natural that both VHDL and Verilog would be working to meet those market requirements for their users.

Similar Scope Project Information:

SimSponsor: C/DA and CAG SimProjNo: See above SimProjD: 1991-06-17 SimTitle: See above

17. Is there potential for this document (in part or in whole) to be adopted by another national , regional or international

organization? Yes

If yes, please answer the following questions:

Which International Organization/Committee? IEC TC93 WG2

International Contact Information?
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650-323-4643
a.zamfirescu@ieee.org

18. If the project will result in any health, safety, or environmental guidance that affects or applies to human health or safety, please explain in five sentences or less.

19. Additional Explanatory Notes: (Item Number and Explanation)

Item 9. Peter Ashenden is the document custodian. The WG chair, vice chair and secretary are responsibile for all other duties.

Item 13. Previously, part of this work has been conducted under the P1076b PAR. When that work started, only new capabilities were proposed to be added to VHDL in the form of a C language interface for tools. The WG has decided additional enhancements and revision of the standard are required. Therefore, this PAR is being submitted to supersede the P1076b PAR and that work will be subsumed under the broader scope of this PAR.

The standards referenced in the scope are as follows:
- IEEE Std 1164-1993. IEEE standard multivalue logic system for VHDL model interoperability.
- IEEE Std 1076-2-1996. IEEE standard VHDL mathematical packages
- IEEE Std 1076.3-1997. IEEE standard VHDL synthesis packages