The IBIS Specification and Verilog-AMS

Michael Mirmak

Intel Corp.

Chair, EIA IBIS Open Forum

Accellera Verilog-AMS WG

February 14, 2005

Agenda

- **What is IBIS?**
- **IBIS Organization**
  - **The IBIS Open Forum**
  - **Open Forum members**
- **IBIS and Accellera Verilog-AMS WG**
  - **Timeline**
- **Backup**
  - **IBIS Model Format**
  - **IBIS Link to *-AMS Models**
    - ***Technical Vision of IBIS<->AMS relationship***
  - **A Related Specification: ICM**

some material from
Arpad Muranyi, Intel Corp.

What Is IBIS?

I **I/O**

B **Buffer**

I **Information**

S **Specification**

IBIS, common name for any of about 30 species of long-legged, long-necked wading birds.

http://www.eigroup.org/ibis/
http://www.eda.org/ibis/

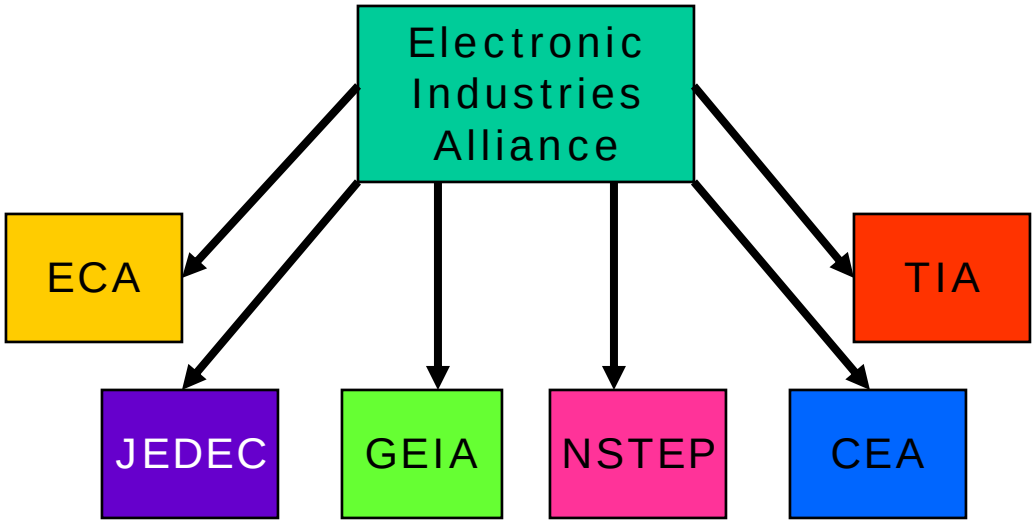
- **IBIS is a universal standard for describing the analog behavior of digital device buffers using data in ASCII text format**

  IBIS files are *not* really models, they just contain the data that will be used by the simulation tool's behavioral models and algorithms

- **Started in the early 90s to promote tool-independent I/O models for system-level signal integrity work**
- **IBIS 3.2 is an official standard: ANSI/EIA-656-A (1999), IEC 62014-1**
- ***IBIS 4.1 incorporates links to VHDL-AMS and Verilog-AMS***

IBIS Organization

- **"IBIS Specification Committee"**
  - **Informally, the IBIS Open Forum**
  - **Manages IBIS, ICM (IBIS Interconnect Modeling) specifications**
- **Part of the GEIA SSTC**
  - **GEIA = Government Electronics & IT Association**
  - **SSTC = Systems, Standards and Technology Council**



IBIS Open Forum

- **Primary Responsibilities**
  - **Manage changes to the ICM and IBIS specifications**
    - ***Latest IBIS revision is 4.1, approved January 2004***
    - ***IBIS 3.2 in wide use, with IBIS 4.0 ramping up***
  - **Maintain IBIS "Golden Syntax Parser" (closed source software)**
    - ***IBIS 4.1 parser expected Q1'05***
  - **Maintain ICM "Golden Syntax Parser" (open source)**
    - ***ICM 1.0 with parser released Q4'03***
  - **Foster technical advances and support user base**
- **Working Practices**
  - **Meets every three weeks via teleconference**
  - **Members may vote on specification changes**
  - **Hold several annual summits in US and Europe**
  - **Annual elections held during DAC in June**
  - **Four Committees: Cookbook, Futures, Model Review, Quality**

IBIS Open Forum Members

- **Twenty-three members in 2004**

- Ansoft
- Applied Simulation Technology
- Cadence Design Systems
- Cisco
- Freescale
- Hitachi ULSI Systems
- Huawei
- IBM
- Intel
- LSI Logic
- Mentor Graphics
- Micron
- NEC
- Panasonic
- Samtec
- Siemens
- Sigrity
- Signal Integrity Software
- Synopsys
- TDA Systems
- Teraspeed Consulting Group
- Texas Instruments
- Zuken

- **Trending to over 30 members in 2005**
  - New: Actel, Agere, AMD, Silicon Image, Xilinx…

IBIS Now Links to AMS

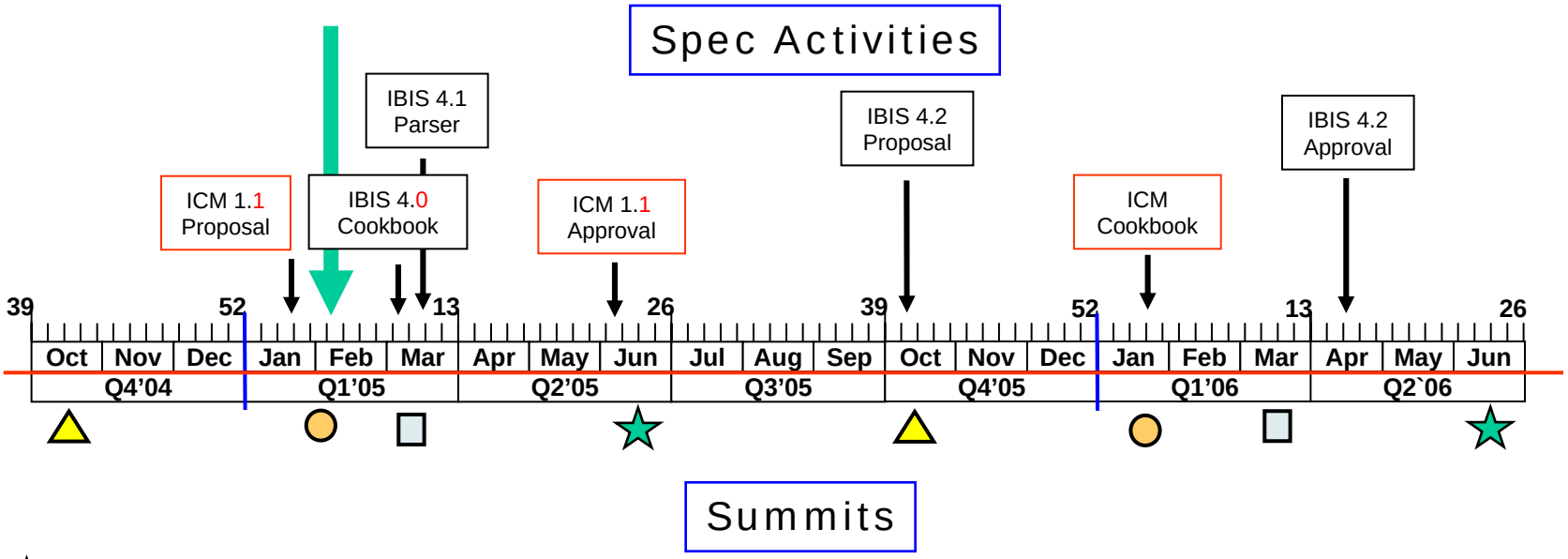
- **IBIS 4.1 incorporates multi-lingual extensions**
  - **Verilog-AMS**
  - **VHDL-AMS**
  - **Berkeley SPICE 3F5**
- **New IBIS keywords link to external code**
  - **IBIS port structure with *-AMS content**
- **IBIS Open Forum interested in WG liaison**
  - **Buffer and SI analysis are growing applications for *-AMS**
    - ***Interest in cross-domain (electrical, thermal) analysis***
  - **Work together to support user-education efforts**

Relationship would have mutual benefits:
- **IBIS can provide feedback on *-AMS language features**
- **Drive adoption by buffer design, SI communities**
- **Keep IBIS "in touch" with latest *-AMS revisions, trends**

IBIS Timeline

Not Shown

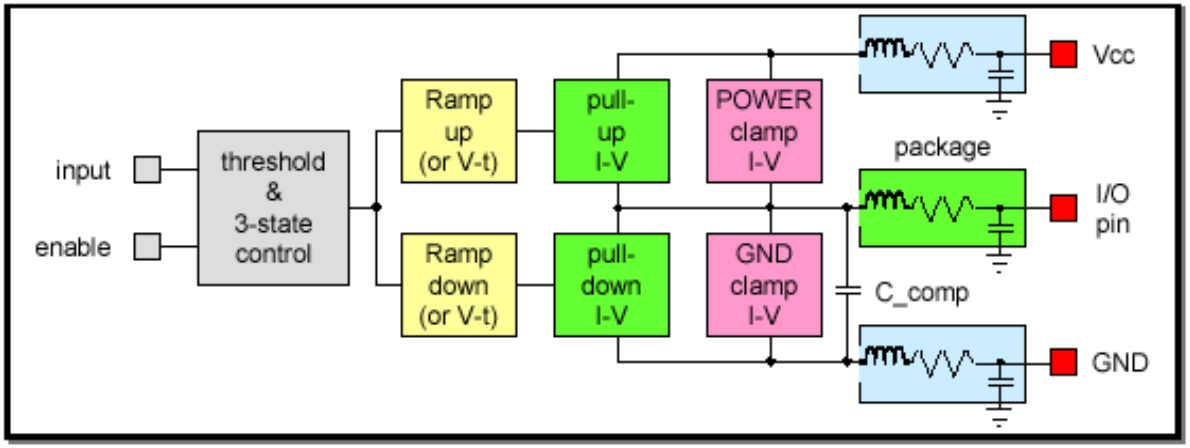
- July, 2002: IBIS 4.0 approved
- Sep., 2003: ICM 1.0 approved
- Jan., 2004: IBIS 4.1 approved



- DAC
- DATE
- DesignCon Summit
- PCB East

BACKUP

IBIS Model Format



Block diagram of CMOS buffer

Covered by keywords such as
[Model]
[Pullup]
[Pulldown]
[Rising Waveform]
[Falling Waveform]

A basic IBIS model consists of:

four I-V curves:	- pullup & POWER clamp
	- pulldown & GND clamp
two ramps:	- dV/dt_rise
	- dV/dt_fall
die capacitance:	- C_comp
packaging:	- RLC values

for each buffer on a chip

Example IBIS Model

```
|**************************************************************************
|
[IBIS Ver]      3.2
[File Name]     example.ibs
[File Rev]      0.00
[Date]          11/12/2004
[Source]        From silicon level SPICE model at Intel Corporation.
[Notes]         The following information is an example only
[Disclaimer]    This information is for modeling purposes only.
[Copyright]     Copyright 2004, IBIS Open Forum, All Rights Reserved.
|
|**************************************************************************
|
[Component]     EXAMPLE
[Manufacturer]  Them Corporation
[Package]
|               typ             min             max
R_pkg           0.000Ohm        0.000Ohm        0.000Ohm
L_pkg           0.00H           0.00H           0.00H
C_pkg           0.00F           0.00F           0.00F
|
|**************************************************************************
|
[Pin]  signal_name  model_name              R_pin  L_pin  C_pin
1      Data         EMP_B0I0P1F1F4P55890
2      Reset        EMP_B0I0P1F1F4P55890
|
|**************************************************************************
```

Example IBIS Model (cont.)

```
|*****************************************************************************
|
[Model]          EMP_B0I0P1F1F4P55890
Model_type       I/O
|
Vinl = 800.000mV
Vinh = 2.000V
Vmeas = 1.500V
Cref = 0.000F
|
|                               typ                 min                 max
|
C_comp                         2.500pF             2.000pF             3.000pF
[Voltage Range]                3.300V              3.135V              3.465V
[Power Clamp Reference]        5.000V              4.750V              5.250V
[Temperature Range]           50.0                100.0                0.0
|
|*****************************************************************************
|
[Pulldown]
|
|       Voltage            I(typ)              I(min)              I(max)
|
     -3.30000000E+0   -256.26000000E-6   -212.20000000E-6   -300.60000000E-6
     -2.24000000E+0   -428.37000000E-6   -346.23000000E-6   -526.48000000E-6
.........
```

IBIS Example – Pointing to AMS

```
|*****************************************************************************
[External Circuit] BUFF-Verilog
Language    Verilog-AMS
|
| Corner    corner_name   file_name       circuit_name (module)
Corner      Typ           buffer_typ.vams  buffer_io_typ
Corner      Min           buffer_min.vams  buffer_io_min
Corner      Max           buffer_max.vams  buffer_io_max
|
| Parameters List of parameters
Parameters  delay rate preemphasis
|
| Ports     List of port names (in same order as in VHDL-AMS)
Ports       A_signal A_puref A_pdref A_pcref A_gcref A_control
Ports       D_drive D_enable D_receive
|
[End External Circuit]
|*****************************************************************************
```

The long-term future of IBIS

- **IBIS originally consisted of two aspects**
  - **Device model behavioral data: V-t, I-V tables, etc.**
    - *Behavior is a "snapshot" at certain conditions (Temp, etc.)*
  - **Interface specs, for user automation: Vinh, Vmeas, etc.**
  - **Power supply information fits in both categories**
- **As industry goes to AMS, some of IBIS redundant**
  - **Behavioral modeling concepts in IBIS expanded in AMS**
  - **AMS much more flexible, includes non-electrical areas**
- **Second aspect of IBIS still very useful**
  - **AMS primarily describes device design behavior**
    - **Evaluation criteria may or may not be included with AMS data**
  - **Still exists a need for standard SI "wrapper" around AMS**
    - **Should include evaluation criteria with AMS model**
    - **Would help user judge device performance in system**
    - **IBIS serves this need – user-defined spec parameters coming…**

A Related Specification: ICM

- **ICM = IBIS Interconnect Modeling Specification**
  - **Standard text format for interconnect modeling data**
  - **"Interconnect" can be connector, cable, PCB traces or even an IC package**
    - ***Defines structure as path between "sections"***
    - ***Defines the electrical data for each section***