Impact on other 2.3 LRM sections of the changes in Chapter 8 (Scheduling Semantics)

Note: chapter numbers are those of the LRM2.3 DraftA.

1.0 Impact on Chapter 5

Action: Change syntax box 6-1 so that analog_construct is defined as

I changed the following based on feedback from Marq on 11/28/07

analog contruct ::=

analog analog_statement

| analog initial analog_function statement

p.s. i don't there should be a ';' after analog_statement - otherwise analog begin ... end wouldn't work.

Add new section 5.1.1

5.1.1 analog initial block

An analog initial block is a special analog (procedural) block, beginning with the keywords analog initial, for simulation initialization purposes.

Same as analog block, analog initial block is also comprised of a procedural sequence of statements. If there are multiple analog initial blocks, they will be executed as if concatenated. However, statements in analog initial blocks are restricted for initialization purposes. So analog initial block shall not contain the following statements:

- statements with access functions or analog operators;
- contribution statements;
- event control statements.

This is similar to the restrictions on the statements in analog functions. This is because an analog initial block will be executed before a matrix solution is available so statements in

an analog initial block are restricted to initialization purposes prior to the availability of a solution of both the digital and the analog modules.

Analog initial block is executed once for each analysis, or each sub-task of parameter sweep analysis (such as DC sweep). The initialization sequence of analog and digital blocks/statements are described in Section 8.3.1 Circuit Initialization. However if a parameter or variable that is referenced from an analog initial block is changed during a sub-task of a parameter analysis, then the analog initial block will be re-executed so that the new value is taken account of.

2.0 Revision to Chapter 8

The second sentenance is revised as:

It is a one time execution of nodeset statements (3.4.3.2), and then the procedural statements in analog initial block, and then the procedural statements in Verilog initial block.

3.0 Impact on Annex A (Syntax)

Action: Make the corresponding BNF syntax change as the syntax change outlined for Syntax6-1 in 1.0

Status = Stu to do

1.0 On Annex C (Verilog-A subset)

Action: This section needs to clearly describe which system tasks which are defined as being supported in the analog context are also supported in the analog subset.

Status: Done by Marq