This is a preliminary discussion of definition and scope of AMS assertions.

1 Problem Motivation and Definition

1. No robust way to check simulation that a trace of an AMS design conforms to the design specification.

2. Correct functionality of the mixed signal design is not thoroughly checked at the interface of analog-digital domains.

3. Minimal sharing of test-bench checkers/monitors across different abstraction levels (Spice, Verilog-AMS, Verilog).

4. Lack of ability to verify system level properties in mixed signal designs.

5. Design properties to be checked can be added progressively as assertions as the mixed signal design matures.

AMS Assertion: A formal way to specify behaviors of real (e.g., time, frequency) domain signals.

These AMS assertions will specify the behaviors of signals (input, output, internal) of the design and can become part of the specification document. Assertions can be used to constrain inputs to the design. Non-trivial exercise of AMS assertions will also provide coverage goals.

2 Scope of AMS Assertions

AMS assertions work aims to target real domain properties in analog mixed signal designs.

The verification of such properties can be done either -

1. Online, while the simulation is running, assertions are checked at runtime.

2. Offline, assertions are checked on the simulation results.

The assertions language permit running both in purely analog engines as well as analog mixed signal engines. This would enable verification engineers to 'lift' the assertions from one domain and port it to another domain.

3 Types of Assertions

The different type of checks that can be made are as follows -

1. Safety Checks: These check that something bad does not happen.
   (a) Single signal checks. This check involves only a single variable. Example: Voltage 'v' remains below a certain threshold.
   (b) Interaction of multiple signals: This check involves more than one variable. Example: Product of voltage 'v' and current 'c' always falls within a specified range.
2. Mixed Signal Protocol Checks: These are used to check that certain relationships hold between signals. The property being checked could pass the analog-digital domain. Example: While reset is true and voltage 'v' is less than a given value then current 'c' should also be greater than a given value.
3. Timing Checks: These check that two or more signals behave according to the specified timing. Example: Whenever current 'c' reaches a certain value the voltage 'v' should drop below a given value within 't' time.

4 More Examples

1. If 'a' $<$ 10 mV and 'b' is true, then 'c' is true.
2. Whenever 'a' goes from zero to one, 'b' remains low for at least 5 ms.
3. If 'a' $<$ 10 mV for more than 10 μs and 'b' is false, then the system should signal failure by making 'c' false. The system remains in the failed condition while 'a' $<$ 10 mV. The system comes out of the failed state when 'a' $>$ 10 mV and the system should make 'c' goto true within 50 μs of this crossing.
4. While 'a' is true, the frequency of 'b' is 100.0 Hz with a 1.0% tolerance.
5. The rise time of 'a' from 0.0 V to 5.0 V is 250.0 ns with a 0.1% tolerance.
6. From 0.0 ns, the settling time of 'a' to a value between -1.0 V and 1.0 V with a 10.0% tolerance is 250.0 ns with a 25.0 ns tolerance.

7. The mean slew rate of 'a' from 0.0 V to 5.0 V is 250.0 V/s with a 1.0% tolerance.

8. The maximum slew rate of 'a' from 0.0 V to 5.0 V is 275.0 V/s with a 1.0% tolerance.

9. The delay between the second rising crossing of 'a' at 2.5 V and the first falling crossing of 'b' at 4.5 V is 250.0 ns with a tolerance of 2.5 ns.

10. After the third falling crossing of 'a' at 2.5 V, 'b' is monotonically increasing from 0.0 V to 5.0 V.

11. From 25.0 ns to 250.0 ns the mean value of 'a' is 0.0 V with a tolerance of 1.0%.

12. After 'a' goes high, 'b' and 'c' must intersect within 25 ns.

13. The -3 dB low pass cut-off frequency from 'a' to 'b' is 25 Hz with a tolerance of 2.5%.

14. The gain-bandwidth product from 'a' to 'b' is 2.5 MHz with a tolerance of 1.0%.

15. The falling crossing of 'a' at 2.5 V is no earlier than (250.0 + f(s)) ns after the most recent falling crossing of 'b' at 2.5 V, where s is the slew rate of 'b' from 5.0 V to 2.5 V.

16. Let S be a finite set of signals defined over $[t, t']$. $(max_{s \in S} sup_{[t,t']} s) - (min_{s \in S} inf_{[t,t']} s) < 2.5$ V. (outer height)

17. Let S be a finite set of signals defined over $[t, t']$. Let $P = \{s \in S | s(\tau) > 0 \ \forall \tau \in [t, t']\}$ and let $N = \{s \in S | s(\tau) < 0 \ \forall \tau \in [t, t']\}$. Assume that $S = P \cup N$. Check that $(min_{s \in P} inf_{[t,t']} s) - (max_{s \in N} sup_{[t,t']} s) > 2.0$ V. (inner height)

18. Let T_1 and T_2 be two sets of crossing times of various signals. Check that $(max_{T_1} - min_{T_1}) + (max_{T_2} - min_{T_2}) < 2 * max\_jitter$. (eye jitter)

19. If $t' > t + \mu$, then
$$\int_{[t,t']} (f(\tau) > c)\, d\tau < M$$