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Wreal Items for Verilog-AMS Accellera Donation

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Preamble

- We are reviewing this technology contribution in order to vote on its potential inclusion in the Accellera Verilog-AMS committee process as extensions to the current standard

- We are NOT reviewing the technology contribution for immediate inclusion in the standard

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Motivation

- LRM needs more support for promoting “Wreal” type to represent typical AMS modeling scenarios
  - “Wreal” type lacks ability to represent Unknown and Hi-Impedence states; a common modeling requirement
    - Addresses Mantis 2162: Need ability to assign z to wreal
  - No support for determining resolution of multiple Wreal Drivers; a situation that is very likely in the real world
    - Addresses Mantis 2281: disciplines and wreal
  - No support for defining programming interaction of Wreals with Electricals
    - Request in Mantis 2160: reals and integers should be able to drive event-driven ports
  - No support for advanced sampling function for sampling continuous signals to discrete wreal
    - Request in Mantis 936: enhanced analog/digital event control

Items for Donation

- Wreals and disciplines
- Wreal Multiple Driver Resolution
  - X/Z States
  - Resolution function definitions
  - Resolution function and disciplines mapping
- Wreal-Electrical Connections
  - Selection and Insertion of Wreal-Electrical Connect Modules
  - New Analog event expression that helps with accurate sampling of analog signals to analog-to-wreal conversion

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Wreal-Disciplines Declaration

- Wreal is like a Verilog-AMS wire type from discipline resolution point of view with a real value type
- Wreal can have a discipline associated with it. Following ways can be used to associate a discipline with wreals
  - `` `default_discipline  wreal ddiscrete ``
  - Discipline declaration

```
wreal w;
ddiscrete w;
```

- Like Verilog-AMS wire, the wreal can get its discipline from discipline resolution process on the basis of its connectivity and usage

Z and X for Wreal discrete signals

- `wrealZState - High-impedance state
- `wrealXState - Unknown state
- This are predefined states that can be accessed in the behavioral source code

```
module buf1(in, en, out);
  input in, en;  output out;
  wreal in, out;
  real outval;
  always @(in,en)  begin
    if (!en)  outval=`wrealZState;
    else if (in === `wrealXState)  outval=0;
    else outval=in;
  end
  assign out=outval;
endmodule;
```

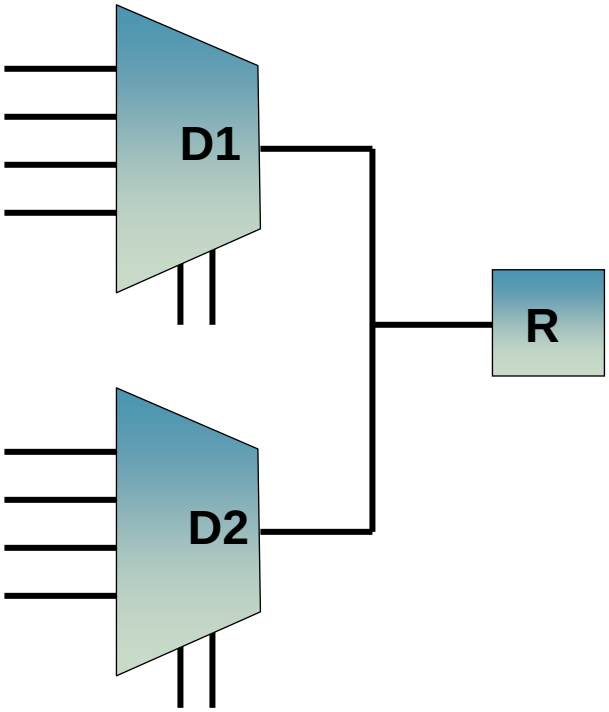
Example: analog buffer with enable

Resolution Functions for Wreal Nets

- When two or more wreal drivers are driving a receiver, a resolution of the wreal driver values is performed using wreal resolution function

- Defined Resolution Functions
  - **DEFAULT** – Single active driver only, support for Z state
  - **4STATE** – Similar to verilog 4-State resolution for digital nets
  - **SUM** – Resolves to a summation of all the driver values
  - **AVG** – Resolves to the average of all the driver values
  - **MIN** – Resolves to the least value of all the driver values
  - **MAX** – Resolves to the greatest value of all the driver values

Global Selectable Resolution Functions for Wreal Nets



D1	D2	Dflt	4st.	sum	avg	min	max
x	x	x	x	x	x	x	x
x	z	x	x	x	x	x	x
x	1.1	x	x	x	x	x	x
z	z	z	z	z	z	z	z
z	1.1	1.1	1.1	1.1	1.1	1.1	1.1
2.2	1.1	x	x	3.3	1.65	1.1	2.2
1.1	1.1	x	1.1	2.2	1.1	1.1	1.1

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Associating resolution functions with wreals

- Through discipline declaration

```
discipline  real_current;
        domain discrete;
        realresolve sum;
enddiscipline
```

- A default setting

```
`default_realresolve  sum
```

This setting should take effect where no other means are available.

Wreal-Electrical Connections

- Connect Module Selection
  - Extension of connect rule semantics

- @absdelta system function to support wreal sampling

absdelta system function for wreal sampling

– Performs real signal sampling based on user provided input
  - Time tolerance, Voltage tolerance, Voltage delta, Rise/Fall time

```
absdelta ( expr, delta [, time_tol [ , expr_tol ]])
```

This is triggered

- At time zero
- When the analog solver finds a stable solution during initialization
- When the expr value changes more than delta plus or minus expr_tol, relative to the previous absdelta event (but not when the current time is within time_tol of the previous absdelta event)
- When expr changes direction (but not when the amount of the change is less than expr_tol

Extensions to connect module to support Wreal-Electrical connections

- Will use following information for connect module selections
  - Disciplines (as before)
  - Port directions (as before)
  - Port/Net value type **(New!)**

  e.g.

```
connect R2E input ddiscrete output electrical;
connect L2E input ddiscrete output electrical;
```

- Note the 2 connect modules for same disciplines and port directions. The selection will depend on the actual net/port types in the design. If a port/net type of “wreal” R2E will be selected.

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An illustration of Electrical -> Wreal conversion

```
connectmodule E2R (Ain, Dout);
input Ain;
electrical Ain;    //input electrical
output Dout;
wreal Dout;        //output wreal
ddiscrete Dout;       //discrete domain

parameter real vdelta=1.8/64 from (0:inf);   // voltage delta
parameter real vtol=vdelta/4 from (0:vdelta); // voltage tolerance
parameter real ttol=10p  from (0:1m];     // time tolerance

real Dreg;   //real register for A to D wreal conversion

assign Dout = Dreg;

  //discretize V(Ain) triggered by absdelta function
always @(absdelta(V(Ain), vdelta, ttol, vtol))
        Dreg = V(Ain);
endmodule
```


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Summary

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