Verilog-A and Verilog-AMS and Cadence Patents

To: Implementor of Verilog-A and Verilog-AMS:
From: Cadence Design Systems, Inc ("Cadence")

During the course of Accellera's (formerly Open Verilog International ("OVI")), efforts in seeking IEEE approval of the Verilog-A/AMS specification, Accellera requested a letter as to Cadence's intent with respect to its patents which relate to Verilog-A and Verilog-AMS.

To that end, Cadence agreed that once a specification for Verilog-A /AMS is approved, Cadence will enter into mutual non-assertion agreements with any company planning to develop products that claim compliance to the approved Verilog A/AMS specification.

The non-assertion agreement states that Cadence shall covenant not to sue a party on any Cadence patents to the extent that those patents must be infringed upon to utilize the Verilog A/AMS specification in exchange for the same covenant by any company. The agreement shall be in the form of a letter, a copy of which is attached hereto, written to Cadence from an authorized officer of any company seeking to use the approved Verilog A/AMS specification. Cadence will then sign a copy of the submitted letter and return it to the requesting company within 10 working days upon receipt. Please note that this non-assertion agreement shall be for the specification only, and not any specific implementation of the specification. The agreement also does not cover an implementation which unnecessarily infringes patents held by Cadence Design Systems.

If your company intends to implement or develop a product that claims compliance with the Verilog A/AMS specification, please have an authorized officer of the company sign the attached letter and return to Cadence at the indicated address. If you have any questions regarding the above, please contact the Legal Department, Director of Intellectual Property, of Cadence at patents@cadence.com

Cadence Design Systems, Inc. *2655 Seely Avenue, San Jose, California 95134*
Phone: *408.943.1234* **World Wide Web**: *www.cadence.com*

To: Director of Intellectual Property, Legal Department
Cadence Design Systems, Inc.
2655 Seely Avenue
San Jose, California 95134
patents@cadence.com

cc: Lynn Horobin
Accellera (formerly Open Verilog International)
15466 Los Gatos Boulevard, Suite 109071
Los Gatos, California 95032

Re: Non-Assertion of Patents for Verilog-A/AMS Specification

It is our company's intent to develop products in support of the Accellera (formerly OVI) approved Verilog A/AMS specification. As per the terms of the agreement approved between the OVI (now Accellera) board and Cadence, we covenant not to sue Cadence Design Systems or it's customers on any patents to the extent that those patents must be infringed upon to utilize the Verilog A/AMS specification in exchange for the same covenant by Cadence Design Systems.

We understand that this non-assertion agreement shall be for the specification only, and does not cover an implementation which unnecessarily infringes patents held by either us or Cadence Design Systems.

It is requested that Cadence Design Systems acknowledge this agreement within 10 working from receipt of this letter.

_____	_____
Signature of Authorized Officer	Signature of Authorized Officer for Cadence Design Systems, Inc.
_____	_____
Print Name	Print Name
_____	_____
Date	Date
_____	
Company Name	