Syntax Explanation about table described below.

Bold Entries - The issue has been accepted in principle and a reasonable consensus arrived. A proposal has already been submitted and discussed. These will be put as part of LRM 2.1. Also some of the issues identified, which have been agreed but needs to updating to LRM come under this category.

Bold Italic Entries - The issue has been accepted in principle and identified as to be addressed as part of 2.1. A proposal has not been sent to the reflector or the contents discussed in committee calls, but action has been identified and assigned and shall be completed soon.

Normal Font - Further discussions/investigation needs to happen for these issues. These issue in most probablity would not be addressed as part of LRM 2.1 version

~~Issues Striked out -~~ No specific issue was identified in the spreadsheet. Probably some generic comments stated. These have been dropped.

All the issues that have been specified in the table, have a issue # and (priority # in brackets). The issue number refers to the number in the spreadsheet, and the priority number refers to the priority that was assigned to the issue. The spreadsheet with these issues could be found in the Verilog-AMS homepage. Some of the fields (Action, Assigned To, When) have been left blank because it was unclear from the discussions. This table deals with all the issues that have been logged with priorities 1 - 98 assigned to them.

Table 1: Updated LRM Issues after discussions (16th, 23rd, 30th April, 6th, 13th, 20th May 2002)

#	Description/Issue	Issue # (Priority #)	Action/Discussions	Assigned To	When
1	Real Valued Ports & real nets	21 (1) 12 (4)	Kevin has sent some write-up on wreal on his “Verilog-AMS views” documentation This document has to be reviewed in one of the committee calls sooner rather than later.	Kevin	Not Sure
2	Back Annotation problem	7 (2)	none. Kevin has sent some mails/docs related to this. He has reposted the same.	Kevin	Post 2.1
3	Discipline Resolution. Algorithm is based on net types rather than driver that appears on mixed net which is Antrim’s point of view. Related Issues: - remove algorithm from chp 8 and delete Annex F to make chapter 8 generic to include alternate views on MS nets - Driver-Reciever segregation - placement of A/D converter - empty disciplines, undeclared nets - how to deal with leaf level wires - no clear definition on OOMR	26 (3) 36 (7) 2 (10) 3 (8) 10 (39) 59 (27) 60 (28)	none. Some DR issues have been addressed as part of 2.1 which have been identified and addressed seperately		

Table 1: Updated LRM Issues after discussions (16th, 23rd, 30th April, 6th, 13th, 20th May 2002)

#	Description/Issue	Issue # (Priority #)	Action/Discussions	Assigned To	When
4	**LRM currently does not support instantiation of digital primitives in analog blocks**	**None**	**This came up as part of discipline resolution, and digital portnames have been reincluded to support this. A proposal has already been sent and these names shall not be used for named override in digital primitive instances**	**Jon**	**2.1**
5	**Ambiguity in connect-resolveTo statement during Discipline Resolution. Not clear how the connect rules apply**	**None**	**This came up as part of DR discussions. A proposal has been submitted related to the changes in Section 8.7.2 clarifying connect-resolveTo rules.**	**Sri**	**2.1**
6	Concurrency. MS synchronization mechanism is not clearly defined	25 (5)	Proposal is being written and shall be submitted soon.	Martin	Not Sure

Table 1: Updated LRM Issues after discussions (16th, 23rd, 30th April, 6th, 13th, 20th May 2002)

#	Description/Issue	Issue # (Priority #)	Action/Discussions	Assigned To	When
7	- LRM does not clearly illustrate the MS simulation cycle and the initilization is not clearly defined. Illustration of IC analysis in AMS is non-existent. - which solver starts first - Initialization mechanism - Rules for synchronization are not sufficient to produce portable code - Mixed Signal Initialization (digital). Verilog-D simulators are transient in operation and hence there is no mechanism defined for static/steady state simulation	31 (16) 17 (18) 5 (19) 64 (32) 65 (37) 23 (44) 92 (43)	Should try to sync up with VHDL-AMS.	Jon	Not Sure
8	***System tasks and function. Issue with $random*** ***1364 sync-up with random function*** ***duplicate for $random***	***32 (6)*** ***66 (69)*** ***83 (96)***	***$random from Verilog 1364-2001 is planned to be used in AMS along with application notes documented***	***??***	***2.1***
9	Truncation vs Rounding mechanism for converting from analog to digital times	1 (9)	Probably use VHDL-AMS mechanism. Resend issue to committee. This has been done and kevin has posted why “rounding” should be used. No other responses have been got in favour of “truncation”	Sri	Not Sure

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#	Description/Issue	Issue # (Priority #)	Action/Discussions	Assigned To	When
10	**Accessing discrte nets & variables (Section 8.3.2 cleanup) - X & Z bits access in analog**	**24 (11), 58 (20)**	**Rewrite section 8.3.2 and propose to committee. This has been completed**	**Sri**	**2.1**
11	***Issue with genvar***	***9 (12)***	***Use genvar mechanism from Verilog digital std. There are some issues with this since support of 'analog_for' and other related issues should be looked***	***Martin***	***2.1***
12	External module defintion to support and import spice netlists in Annex E	6 (13)	none. I think this is going to be vendor specific. Thats the way its looking from the Committee discussions.		
13	Support for global design variables	85 (14) 35 (15)	relook at dynamic parameter proposal. Martin to have a look and repost.	Martin	Post 2.1
14	***Ambiguities with if-else-if syntax***	***87 (17)***	***Martin to illustrate this example in his 'genvar' proposal which will address this problem.***	***Martin/ Sri***	***2.1***

Table 1: Updated LRM Issues after discussions (16th, 23rd, 30th April, 6th, 13th, 20th May 2002)

#	Description/Issue	Issue # (Priority #)	Action/Discussions	Assigned To	When
15	**'default_discipline usage is unclear, and how to deal with analog and digital primitives**	**45 (21)** **13 (24)** **47 (38)**	**Write a proposal on default disciplines for analog primitives and digital ones. This has been completed**	**Jon**	**2.1**
	Defining 'default_discipline for digital and analog primitives	**46 (62)**	**analog primitives shall have a default discipline as electrical. For digital primitives, they will use the 'default_discipline declaration. This action has been done and a proposal already been submitted.**		
	Compatible disciplines to analog primitives	**83 (95)**	**Same as above. Primitives like source, resistors, capacitors can often be used in other domains but if they are mechanical it will make it incompatible as per current LRM. Above proposal addresses this issue.**		
	Disciplines of analog primitives. How to set and defaults	**82 (98)**	**Duplicate. Same proposal as above.**		
16	***Initial value of wreal to be set to 0.0 if not defined***	***43 (22)***	***LRM will state that the value will be 0.0 if it hasnt been determined at t=0***	***Jon***	***2.1***
17	***Contribution statements in IC analysis***	***50 (23)***	***Contribution statements shall not be allowed as part of initial conditions***	***Martin***	***2.1***
18	***Confusion on the way bi-dir model is being stated in Section 8.6***	***61 (25)***	***The diagram illustrating the example will be rewritten and the example shall reflect the diagram***	***Jon***	***2.1***

Table 1: Updated LRM Issues after discussions (16th, 23rd, 30th April, 6th, 13th, 20th May 2002)

#	Description/Issue	Issue # (Priority #)	Action/Discussions	Assigned To	When
~~19~~	~~Mixed Signal language features~~	~~8 (26)~~	~~There is no specific issue that has been stated and hence shall be dropped for now~~		
20	***Driver Type function. There should be a driver access function for finding type of driver.*** ***driver_type_function ::=*** ***$driver_type(signal_name, signal_index)***	***4 (29)***	***This was agreed and kevin will prepare the writeup material for LRM Kevin has already posted the proposal to the committee***	***Kevin***	***2.1***
21	Analysis dependent function should be clearly defined with use of tables to denote how they behave.	16 (30)	This should also include clarifying currently existing confusion on DC Sweep mechanism. A seperate issue to be posted regarding behaviour of DC sweep		Not Sure
22	Net resolution function unclear. This replaced assign dval=dval syntax. Connectmodule missing digital sections and net resolution stuff	62 (31) 69 (86)	Jon is unclear on what this issue exactly is. Shall repost this. Also not sure what the purpose of net resolution is and how it is exactly to be used	Jon	Not Sure
23	Issues with discipline and nature compatibility.	86 (33)	Relook at this problem again	Sri	Not Sure

Table 1: Updated LRM Issues after discussions (16th, 23rd, 30th April, 6th, 13th, 20th May 2002)

#	Description/Issue	Issue # (Priority #)	Action/Discussions	Assigned To	When
24	*LRM cleanup typos* *- Section 8.3.2 fix*	*84b (34)*	*This has been accepted and shall be updated. Part of this has already been addressed in 2.0*	*Sri*	*2.1*
	LRM typos	*84a (85)*	*- Not to use "max" and use "maxval" instead since max is a keyword (Section 3.4.1.1, 3.4.3.5)* *- absdelay isntead of delay in section 4.4.14* *- @final_step for DCOP should be 1 in section 6.7.4* *- use "merged" instead of "merge" when referring to the keyword (sec 8)* *- Figure should have NetC.c_out instead of NetC.b_out (8.2.3)* *- MS examples should not use "==" for digital signal comparison in analog context. Should use case and methods using X & Z as in new proposal for section 8.3.2*		
	Spelling mistake on "boltzmann" and "planck" in constants file	*78 (97)*	*Shall be fixed.*		
25	*Issues with regards to example 3.8 where derived disciplines are used but BNF does not support them*	*88 (35)*	*This has been accepted and shall be updated in the document. Suggestion #3 would be dropped*	*Sri*	*2.1*

Table 1: Updated LRM Issues after discussions (16th, 23rd, 30th April, 6th, 13th, 20th May 2002)

#	Description/Issue	Issue # (Priority #)	Action/Discussions	Assigned To	When
26	***TRI & WIRE are aliases***	***42 (36)***	***LRM should specify tri & wire are aliases***	***Jon***	***2.1***
27	***Syntax consistencies with 1364 in BNF snippets specified while describing the feature***	***53 (40)***	***It was agreed that the snippets shall be the same as the way it has been specified in the BNF o(annex) f AMS lrm. Remove ";" in table 6-1 to make it consistent***	***Jon***	***2.1***
	Syntax 6-3, 6-4, 6-5 in Section 6.3, 6.4, 6.5 and consistency with BNF.	***54 (68)***	***The sytax as shown in the snippets (6-3, 6-4, 6-5) shall reflect BNF specified in Annex as is.***		
~~28~~	~~New mechanism for doing insertion of connect modules using connect rules from the previous versions~~	~~28 (41)~~	~~There is no real issue mentioned in this.~~		
~~29~~	~~Behaviour in top level modules~~	~~19 (42)~~	~~Its agreed that top level module can have behavioural stmts. There is no issue that has been identified.~~		

Table 1: Updated LRM Issues after discussions (16th, 23rd, 30th April, 6th, 13th, 20th May 2002)

#	Description/Issue	Issue # (Priority #)	Action/Discussions	Assigned To	When
30	Driver access and net resolution functions	29 (45)	~~For the time being it was agreed that the driver access functions would be called from connect modules only. Otherwise it would involve a change in Verilog-D.~~ ~~For missing functions - no way to discover what change caused driver_update(). Nothing new is going to be added. $driver_type might be extended later~~ Jon to clarify what “default” means in the explanation for net_resolution function.	Jon	
31	Spice vs Verilog name conflict. There is an issue while instatiating two modules with same name defined in different abstraction (spice v verilog)	80 (46)	Lots of discussion but not clear whether LRM is going to change with regards to this. There is no name scoping mechanism in LRM currently. Error will be issued when there is a name conflict. Cadence uses some sort of header file mechanism to resolve this without error, and Antrim uses standard library methodology (pick the first match from the library). Looks like this is going to go the vendor specific way.	??	??

Table 1: Updated LRM Issues after discussions (16th, 23rd, 30th April, 6th, 13th, 20th May 2002)

#	Description/Issue	Issue # (Priority #)	Action/Discussions	Assigned To	When
32	Supplementary driver access functions.	30 (47)	none		Post 2.1
33	***Switch branch syntax not defined in BNF tho' explained in an example*** ***Implicit Switch Branches*** ***Indirect Assignment in conditionals. Should indirect branch assignment be made illegal in conditional***	***55 (48)*** ***51 (51)*** ***52 (66)***	***The BNF will be updated to allow switch branch syntax and made legal.*** ***We are going to allow direct contribution inside conditional (for switch modelling) so why not indirect. Also LRM restricts direct and indirect branch contribution for same branch. Should this be allowed?***	***Jon/Sri***	***2.1***
34	Adding Support for 'NaN & X' into Verilog-AMS. Contribution of these values to a branch would be an error, however analog variables should be able to propagate this value.	89 (49)	There has been lot of debate on this over many calls. Kevin has been pushing for support on this because Verilog-D handles it. Martin talked to 1364 committee with regards to this and apparently was told that its not a good choice to support the same.	Martin	
~~35~~	~~Discipline rules for branches.~~	~~48 (50)~~	~~Not clear what the issues stated is~~		
36	Discipline Compatibility - How do you resolve disciplines with different abstol. Currently LRM states that the tighter abstol will apply. Is that the correct approach? Should there be a resolution function?	90 (52)	For the time being it is going to have "minimum value" as the default.		Post 2.1
~~37~~	~~Ground Declations. Lot of changes from previous version~~	~~11 (53)~~	~~No real issue stated here.~~		

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#	Description/Issue	Issue # (Priority #)	Action/Discussions	Assigned To	When
38	**Uppercase issues. When you do -upcase with ncverilog there is a clash between nature Force and verilog keyword of same name.**	**79 (54)**	**Leave as is but warning issued by simulator. Nothing need be done in terms of updating LRM**		**2.1**
~~39~~	~~Restriction on analog operators. Currently no default for NULL arguments. LRM does not support null argument to some operators~~	~~14 (55)~~	~~No change required in LRM~~		
40	***The meaning of 'analysis point' in the table explaining initial_step/final_step for all analysis is not clear (Section 6.7.4)***	***18 (56)***	***Rephrase the explanation given for the table.***	***Jon***	***2.1***
41	Augment "external module" and "macromodule" definitions with a "simulator class". A syntax is actually suggested in the xls spreadsheet (repstop proposal) Case sensitivity of SPICE simulators should be accounted for. Rep-Stop proposal sent by Kevin to handle spice translations filters for foriegn languages Representation stops (duplicate of above)	?? (57) 81 (65) ?? (73) 93 (87) 95 (89)	"shell" already does this for the digital simulators. This will be investigated further, but wont be addressed as part of 2.1 This is the same as above issues. Proposal for extending "external module" with parameters and/or keywords indication source file, language, and a filter program to translate into VAMS same as the above issues stated. The acutual issues list includes two proposals that have been submitted by Kevin	Kevin	Post 2.1

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#	Description/Issue	Issue # (Priority #)	Action/Discussions	Assigned To	When
42	Specifying expressions for port connections.	39 (58)	What is the discipline of the expression. Might have to create driver as an unnamed implicit function etc etc. Name of driver?	Jon	Post 2.1
43	***Supplementary drivers and delays. $driver_update is not sufficiently defined in terms of what delays should be accounted for. Example given in spreadsheet***	***63(59)***	***This section would be made more informative. It shall be clearly stated when it would be expected to work (gate level) and when it wont.***	***Kevin***	***2.1***
44	***When should range checking for paramenters be done. Should it done on default or instance value?***	***38(60)***	***Checking should be done only on the final value of the parameter for that instance. This feature is used for users to set value, not during model development. Clarify this point further in LRM***	***Sri***	***2.1***
45	***Using OOMR to override disciplines on behavioural nets be allowed? Example specified as part of spreadsheet.***	***40 (61)***	***Should be limitations on OOMR declaration of nets that are used behaviourally. Cannot change the discipline of net used behaviourally. Can be done only for a undeclared net. Using OOMRs to override discipline of behavioural nets shall be disallowed***	***Jon***	***2.1***
46	***Compatibility of contionous disciplines on the same signal.***	***57(64)***	***Should be stated in the LRM that the continous disciplines of a signal must all be compatible as they are solved to the same node.***	***Jon***	***2.1***

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#	Description/Issue	Issue # (Priority #)	Action/Discussions	Assigned To	When
~~47~~	~~Absolute delay operator. delay() has changed to absdelay().~~	~~15 (67)~~	~~No real issue. Closed.~~		
48	***'include does not support both <> and also ""***	***91 (70)***	***Verilog-AMS should support both the <> and the "" for inclusion of header files and differntiating system defined header files with user defined ones.***	***Kevin***	***2.1***
49	***Real Value port examples have error in them (Examples in section 3.5, 7.3.3)***	***44 (70)***	***Examples to be fixed to use assign for wreal and use wreal in instantiation, and also add a top level block for example in 7.3.3, and the testbench use wreal. However priority 1, 4 needs to be dealt with.***	***??***	***2.1 ??***
50	The specification of roots for the Zi filter has changed from Z^-1 to Z. Poles and zeros are roots of Z^-1 but this changed in post 1.4	72(72)	Expressing roots as Z^-1 seems more appropriate.	Peter	??
51	Do we need nuetral disciplines if wire is already nuetral	41 (74)	It was fealt that nuetral discipline is not required	Sri	
52	Should flow and potential etc be part of global keyword list	70 (75)	It was generally agreed that there should be one single global keyword list with namescoping.		
53	There are no rules for vector versus scalar connections if the entity is reg rather than a wire type	20 (76)		Peter	

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#	Description/Issue	Issue # (Priority #)	Action/Discussions	Assigned To	When
54	***Coercion of string to real does not make sense and is not defined, but is currently allowed***	***37(77)***	***It was decided that coercing a string to real would be given as error. String arguments shall have %s. Also assigning strings to real and integer does not make sense in analog.***	***Martin***	***2.1***
55	The concept of associating variables based on which context it is assigned is apparently felt as being ambigous.	22 (78)	Not sure of the origin of this problem. It was raised by Antrim and needs clarification	Peter	
~~56~~	~~In the connect statements can the connect rule block have "zero or more" rules specified. ie Empty block~~	~~68 (79)~~	~~Current LRM allows empty connect rule blocks and it was agreed that this need not be changed. Nothing need to be done as far as LRM is concerned~~		
57	***Null arguments using ,, syntax.***	***71 (80)***	***It was agreed to use the , , syntax for Null args instead of empty {}, and it was identified that NULL args for laplace and Zi can be given using , , syntax for the numerator/denominator. This should explicity be stated for these particular analog operators.***	***Jon***	***2.1 ??***
58	Current LRM makes it illegal to have incompatible continous disciplines on the same net. Antrim sees this as useful feature and allows user complete control	27 (81)	Raised by Antrim. Peter would look further in to it and address this LRM issue.	Peter	

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#	Description/Issue	Issue # (Priority #)	Action/Discussions	Assigned To	When
59	***Units for charge, angle and other things defined in disciplines.h should adhere to the SI standard.***	***75(82), 76(83)***	***It was agreed that std. notation be used. C for Charge, rad for Angle, rad/s for angular velocity, rad/s^2 for angular accelaration***		***2.1 ??***
60	***Values specified in constants file for charge, light, boltzman constant etc***	***77 (84)***	***This should adhere to std definitions and LRM should be consistent with this.***	***Sri***	***2.1***
61	defparam vs Instantiation precedence. (compiled vs last value given for parameter, compiler would not know about other modules)	56 (88)	There was discussion that Verilog-D is trying to get rid of it.		
62	Light Weight Conversion. connectmodule only addresses automatic conversion of signals passed through ports (structural). What about OOMRs where behavioural code asks for values not passed through ports? These are just probes which dont need resolution	94 (90)	Peter had prepared some documentation on this. To be sent to the AMS committee	Peter	??
63	***Annex C does not list boundstep arg changing from constant to expression (dynamic)***	***73 (91)***	***Add it to the list of changes in Annex C***		***2.1***
64	VPI issue. Nature and disciplines should not use param_assign, and instead there should be a new object called attr_assign	67 (92)	-		Post 2.1
~~65~~	~~'resetall? does it rest all the compiler directives?~~	~~33 (93)~~	~~'resetall resets all the compiler directives defined. No change required in LRM??~~		

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#	Description/Issue	Issue # (Priority #)	Action/Discussions	Assigned To	When
~~66~~	~~filenames have changed from foo.h to foo.vams. Why?~~	~~34 (94)~~	~~Change came from synopsys.No issues with this~~		