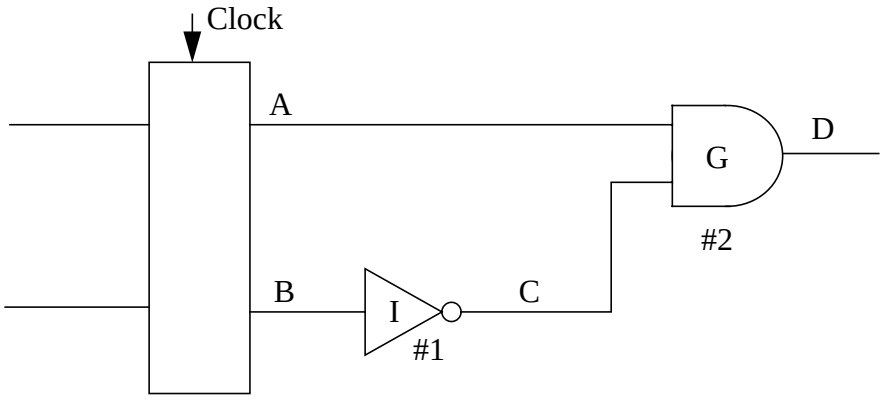
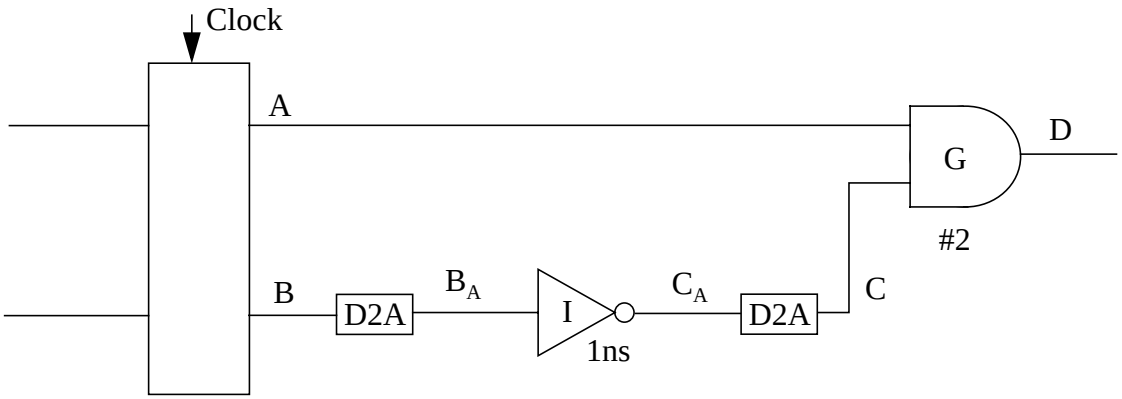
1.0 A2D Error

It is desirable when swapping components between digital and analog models in Verilog-AMS that timing errors are such that it is unlikely that the digital times change, that way test patterns etc. in digital testbenches do not need to be rewritten. Consider the following circuit:

‘timescale 1ns/1ns



The inverter (I) has a one unit delay and the gate (G) has a two unit delay, so the digital delay from the clock edge to a result at D is three units (3ns). If the inverter is replaced with an analog equivalent the delay from the clock edge to D should still be three units:



For the sake of argument we will assume the signal B is converted to B_A signal at C_A is converted to C with no timing errors, but the delay from B_A to C_A is only approximately 1nS so the signal C is handled in its own delta cycle. The evaluation of G to generate D occurs during that delta, but scheduling D requires rounding to the digital clock.

The rounding error introduced during the scheduling of D needs to be such that small variations in the B_A to C_A delay do not change the digital result. Since the base precision in this example is 1ns, the tolerable error on the analog side[1] should be +/- 0.5ns before the digital result changes.

If the approach to rounding is to truncate analog time to the base precision, then any delay less than 1ns through the analog inverter causes the scheduling of D to be for 2ns after the clock (not 3ns). I.e. a 0.99ns delay from B_A to C_A which is 0.01ns off the original digital timing results in a 1ns timing error at D. The average cumulative error with truncation is half a unit per unsynchronized path from digital to analog and back, the maximum is one unit per path, i.e. another analog inverter after G with the same delay of 0.99ns and a conversion back to digital would give a 2ns total path error.

Rounding to the nearest unit allows the analog delay to vary by half a unit before the digital behavior changes. The average cumulative error with rounding to the nearest unit is zero, the maximum error is half a unit per path.

Since the module ‘timescale is only used for module-local time calculation, the simulator can pick a finer global base precision for scheduling[2]. Rather than force simulators to use round-nearest, it is easier to stipulate what the maximum scheduling error should be for the A to D conversion: it should be the worst case of rounding i.e. half the base precision of the module where conversion is performed, or the base precision of the connect module if that is smaller.

1. From model evaluation
2. Normally the smallest found.