IEEE P1800 SystemVerilog Working Group
UNAPPROVED MINUTES
10 October 2005
10:00 a.m. – 2:45 p.m. PDT

1. CALL TO ORDER

Chair Srouji called the meeting to order at 10:15AM PDT. Attendance is shown below.

Key:
DR= Designated Representative
DRA= Designated Representative Alternate
O=Observer
S-Staff

Present	Entity Name	Representative Name	Representative Designation	IEEE-SA Member	Voting Member
X	**Accellera**	Karen Pieper	DR	**Yes**	**Yes**
X	**IBM**	Johny Srouji	DR	**Yes**	**Yes**
X	**Mentor**	Dave Rich	DRA	**Yes**	**Yes**
X	**Graphics**	Doug Warmke	O		
X	**Sutherland HDL**	Stu Sutherland	DR	**Yes**	**Yes**
X	**Synopsys**	Oz Levia	DR	**Yes**	**Yes**
X	**Fintronics**	Alec Stanculescu	DR	**Yes**	**Yes**
X	**Synopsys**	Brad Pierce	O		
X	**Sunburst Design**	Cliff Cummings	O		
X	**Sun**	Neil Korpusik	DR	**Yes**	**Yes**
X	**Intel**	Yossi Levi	DR		
X	**IEEE-SA**	Noelle Humenick	S		

2. Approve agenda

A motion (Victor Berman, Stu Sutherland) was made to approve the agenda. The motion approve unanimously.

3. CALL FOR PATENTS

Noelle Humenick read the patent slides.

4. Approval OF 29 JULY 2005 meeting minutes

A motion (Victor Berman, Karen Pieper) was made to approve the meeting minutes. The motion approved unanimously.

5. Action Items Review and Follow-up

Johny reported that all action items have been closed, except for Letters of Assurance (pending and on track)

6. Update from RevCom

Johny explained that P1800 and P1364 submittal packages were prepared and submitted to RevCom. Both Standards postponed pending inclusion of names of negative balloters for both ballots.

Noelle provided a report indicating that recirculation for P1800 is now closed and acceptable to Dave Ringle-RevCom. Recirculation for P1364 is now closed and also acceptable. Next RevCom meeting will occur on October 27 or 28, where both standards will be considered on that date. Publication for P1800 is targeted for November 9, 2005 (funded project). Publication date for P1364 is March 2006 (unfunded project and not eligible for accelerated publication).

ACTION REQUEST - Stu & Noelle have an action item to get Tapati Basu's name from sv-cc committee on the P1800 Standard.

7. Financial Report

Noelle presented that the working Group will have used all IEEE-paid funds as of the 9th of November. No outstanding invoices are expected. No expenses are anticipated beyond what is currently budgeted. (Thanks, Victor and Oz!)

8. Review overall schedule of the P1800 WG

P1800 approval date is November 3rd and a press release expected 1-2 days after P1800 release. The working group anticipates submitting the P1800 Standard to the IEC

9. Two year future roadmap discussion for 1800 & 1364

Johny presented the following document regarding possible items for discussion for future activities related to SystemVerilog: "P1800 and P1364 Long Term Plans; Structure and Operation"

Possible future activities voiced by Oz

- Support
- Bug-fixing
- Merging of 1800 & 1364
- Enhancements
- Further standardization into International Organizations

Alec noted IEC Standardization is very important as part of the original P1800/P1364 PARs

Perhaps Analog Mixed Signal (AMS) should be included in a future version of the SystemVerilog standard.

User comments:

Yossi - Intel

Intel is pleased with the SystemVerilog work. Need to have live committees to report problems and request enhancements. Some enhancements were not added to P1800 due to accelerated schedule. Yossi expressed the desire to consider extensions going forward. A two year turn of the standards is a good idea. More than two years might promote diverging standards. A desire to merge 1800, 1364 and AMS was also expressed. Also would like syncing of PSL & SVA. Enhancements are the most important issue.

Neil - Sun

Sun does not currently use SystemVerilog but will be using SVA shortly - limiting factor is tool availability. Next capability of interest is the design subset. No big need for AMS (not actively used) - merging LRMs is a good idea (not sure if two years is doable for the merge) - would like a new update in two years or less. Perhaps merge committees (1364 & 1800). Clarifications and bug-fixes are most important.

Cliff - Sunburst Design

Users are looking for live support for bug fixes and clarifications. Users are initially interested in SystemVerilog verification. Users would like enhancements like AMS, 2-State, and other incremental improvements to new SystemVerilog features. Merging is considered a good idea - some of the SystemVerilog sections can be moved into a new document without any merging effort.

Stu - Sutherland HDL

Seconds preceding comments - suggested separated volumes or dot-standards for modeling, testbench, SVA, and API. Take PLI into the API document. AMS could be another volume or dot-standard. Live document with errata and clarifications (highest priority) should be available until the next release. Enhancements are also important. If we stop doing enhancements, the language dies.

Victor - Cadence

Live standard with bug fixes and clarifications is the most important activity and must have consistent releases of addendums. Combining 1364 & 1800 could be more difficult than anticipated. It may make sense to re-write the LRM to put definitions in a single place and to make standard more concise. Note - re-write could cause difficulties with existing tools. Enhancements are nice but not the top priority. Groups should remain pretty much the same except merge 1364 and 1800 groups.

Dave Rich - Mentor

1800 & 1364 should be merged (important to users and vendors) - 1800 spec is not currently up to par and needs at least one round of updates and clarifications before merging documents. 1364 & 1800 committees could be merged, PLI/API/CC-partition, Bug-fixes/Modeling. A forum is needed to make clarifications and corrections that will be firm and web-available for the user community to view. Generic interoperability standard would be good (not just but including VHDL). Role of Accellera should be to form the support group for SystemVerilog.

Brad Pierce - Synopsys

Personally feels that merging standards is a waste of time. Interoperability with VHDL could be standardized. Enhancements are going to happen so it is matter of whether they will be captured or not (more important than fixes).

Doug Warmke - Mentor

Priority should be clarifications and bug-fixes - a forum to clarify and document fixes is required. Future enhancements need to be prioritized.

Oz Levia - Synopsys

EDA vendors want to make a profit and sell tools - SystemVerilog should be a viable business. Integration with other standards like VHDL is extremely useful. Priorities are:

#1 - bug fixes & clarifications

#2 - integration with other interesting standards

#3 - future extensions and enhancements to SystemVerilog (selecting enhancements needs to be carefully considered and accepted).

#4 - merged LRM is important, but a lot of work. Current organization is good, even the separate 1800 and 1364 committees.

Alec - Fintronics

The LRM is very large - there should be different books for different parts of the standard and the PLI should be part of the standard. Deprecation of features is a bad idea. Putting tf & acc features could be part of a separate book. Interoperability is an important issue - both in general and in particular with SystemVerilog, VHDL & SystemC. Most important interoperability is between Verilog & SystemVerilog. Support of committees should be done through the IEEE.

Karen - Synopsys

Agrees with Brad & Oz's comments - Should keep committees structured much as they are, perhaps with some minor merging between 1364 & 1800. Merging errata & enhancement committees would be a good idea because they have similar knowledge and skills. Personal opinion - prioritize errata and enhancements. Interoperability with VHDL is a good idea. No great return for merging multiple standards.

Johny - IBM

Prioritize between balanced set of enhancements and bug fixes. Fix important bug fixes. Add enhancements where divergence could happen to satisfy customer requests. Current committee structure is pretty good as is. Two years time-frame for next approved LRM is a good timeframe, but we do not need to fix this schedule. Errata and clarifications and a live standard, perhaps every 6 months would be a good idea. The #1 priority is to make sure there are no incompatibilities between SystemVerilog and Verilog. Merged LRM is a good idea but not as high of a priority and the effort will be large.

SUMMARY

We do not see major enhancements in the next 2-year period. We do see a need for prioritized bug-fixes and enhancements. Set a goal to complete the next IEEE SystemVerilog Standard in two years (completion could be anything from end of technical work to actual approved and published IEEE Standard).

We need an approved mechanism to make corrections and revisions for release at least every six months.

Merging Discussion

Stu believes it is essential to merge the 1364 & 1800 documents to (1) make tools support the full merged language, (2) users can write code without `ifdef's, (3) the working group already said we would do it.
Victor would like a re-written and merged LRM but does not believe it is critical to merge the documents.

Oz would like a merged LRM but is concerned that if merging has priority that the next revision will be significantly delayed.
Karen is concerned that it will require an engineering-year to edit the document, and 6 months - 1 year for a committee to review the edited document (committee of ~6 engineers).
Brad fears that nobody will want to participate on the merging committee.

Points of disagreement:
(1) The effort required to merge the documents
(2) The quality of the merged document

Discussion of Operation and Structure of Technical Committee

At this time, keep the committees as they are and Karen has the action item to return and propose changes if she deems the changes are beneficial.

Concerning 1364 Committees
BTF has been folded into the BC.

Encryption committee is now dissolved and errata will be addressed by the BC.

1364 Database will be merged with the SystemVerilog database.

Proposal (Karen - 2nd Neil - unanimous passed) - move the encryption and errata committees into SV-BC.

Action Requests

Johny to look into requirements and rules related to making SystemVerilog corrections and revisions available for public release. Johny to find the IEEE-proper method to possibly make enhancements to the SystemVerilog Standard.

Stu to do sizing and estimates related to merging the documents and report back to the committee at the next meeting.

Karen & Victor to also do sizing of the review effort and report back to the committee at the next meeting.

Karen has the action item to return and propose changes to the committees if she deems the changes are beneficial.

Proposal (motion: Victor - 2nd Stu - unanimous passed) this committee authorizes Karen to establish the P1800 errata committee to begin addressing issues related to the P1800 standard. Karen to report back to the P1800 working group with a proposed organizational structure to address errata in the next working group meeting.

10. Future P1800 Interface Work

Desire to enable interfaces to VHDL, AMS and SystemC.

First interface to address should be VHDL.

Action Item: Johny and Karen to facilitate first meeting between SystemVerilog and VHDL groups.

11. NEXT MEETINGS

Potential dates and places for the next meeting (November time frame) will be proposed by chair Srouji.

12. ADJOUNMENT

A motion (Stu Sutherland) was made to adjourn the meeting. The meeting adjourned at 2:45 p.m. PDT.