FDL'01

FORUM on DESIGN LANGUAGES

September 3-7, 2001 - Lyon, France

*A SIG-VHDL event sponsored by **ECSI**, co-sponsored by IFIP 10.5 *, ACM-SIGDA*, ITG*, GMM**

CALL FOR CONTRIBUTIONS

www.ecsi.org/ecsi/fdl/fdl01
fdl01@insa-lyon.fr

FDL is the European forum to exchange experiences and learn of new trends, in the application of languages, associated design methods and tools, to design electronic systems. By offering several co-located events, this multi-facetted forum gives an excellent opportunity to gain up-to-date knowledge across a wide field.

The forum is organized around several interrelated workshops with working sessions and technical discussions. The workshops are:

❶ Hardware Description Languages

The HDL workshop is dedicated to all topics around VHDL and other HDLs. It covers all aspects of today's HDL based system design from traditional digital circuit design to the latest development in multi-languages design, object oriented languages and link to HW/SW co-verification.

Keywords: HDL standardization, object oriented HDL, link to co-verification, multi-language design, languages for formal verification, language extensions

❷ Architecture Modeling & Reuse

This workshop will explore the practicality of abstract system modelling. Four topics will be addressed: characterizing the performance model (field-of-use, qualifying, benchmarks), relating language and modeling (best syntax for model requirements), test-bench migration (exposing property requirements, refining transactions, co-verification), and building a system modeling environment (management issues, IP exchange, design refinement).

Keywords: system modeling, performance modeling, design refinement, interface refinement, hierarchical verification

❸ System Specification & Design Languages

The wokshop (SSDL) has become the yearly event on system specification. It continues the SLDL workshop but also accomodates European system level projects and VSIA SLD. It aims at developing an industry-wide consensus on problems met by the designers of Systems-on-Chip (SoC) : system level specification formalism, proven refinement processes, task allocation, architecture languages, hardware and software co-synthesis, functional and implementation constraints, design flow and EDA tool support; including sensors, MEMs and optical components.

Keywords: SLDL, formal system specifications, proven system refinement, constraint propagation, functional and synchronous specification languages, OOD, models of computation

❹ Analog & Mixed Signal Specification

Analog and mixed signal (AMS) components are already a necessity in the strongly growing application market of embedded devices. In order to cope with their inherent complexity, new methodological approaches address areas like AMS behavioral specification, analog synthesis, mixed-signal simulations, AMS reuse, library developments, MEMS, RF specification, etc. The aim of this workshop is to present and discuss new research activities and exchange ideas in these and related areas.

Keywords: analog & mixed-signal specification languages, libraries development, analog & mixed-signal reuse, modeling, analog synthesis, mixed-signal simulation, RF issues

❺ C/C++ Based Hardware/Software Specification and Design

Recently a strong trend toward using C/C++ for hardware/software systems design has been observed. This workshop discusses pros and cons of C/C++ based design. Different examples of tools will be presented including synthesis, software generation and RTOS aspects, simulation, and performance evaluation and analysis. An overview of different standardization activities and their status will be given. Roadmaps for the future development of existing approaches will be presented and discussed.

Keywords: specification languages, C/C++ based design, synthesis and simulation, standardization, SystemC, SpecC, ...

❻ Real Time Specification for Embedded Systems

The challenge for embedded system specification is to integrate OO-based languages with typical modeling paradigms and constraints of embedded systems. This workshop addresses all issues associated with real-time systems like hard real time constraints, modeling paradigms for automata and differential equations, OO-based design and specification of intelligent services (adaptivity, learning, or proactiveness).

Keywords: UML-RT, RT Java, StateCharts, Petri Nets, synchronous languages, block diagrams, specification of intelligent features

❷ Design Environment & Languages

Todays EDA environments mostly come with a combination of graphical and textual design languages. Collaborative engineering is not well supported in current net-based environments, and is not making use of valuable infrastructure. This workshop will address new directions in the area of tool-specific design languages, language application, and means for the configuration of distributed design environments.

Keywords: graphical/textual design languages, usability, design methodologies, Web-based design, security, workflow specification, tool encapsulation

* With no financial participation

TUTORIALS

Proposals for half day tutorials will be accepted based on topic relevance and evidence of a 4 hour comprehensive agenda (to be sent to the tutorial chair Ralf Seepold before April 21st).

HANDS-ON-LABS

Hands-on-labs from EDA tool providers are invited. They will be given on Unix or PC workstations and held in parallel with technical sessions. A title and a summary of the lab contents are required (to be sent to the hands-on-labs chair : John Willis).

PANELS AND SPECIAL SESSIONS

Proposal for special sessions (panels, working sessions, standardization groups, embedded tutorials, etc.) are welcome. They will be embedded in regular workshops. Send your suggestion to FDL chairs (Eugenio Villar and Anne Mignotte before April 21st).

REQUIREMENTS FOR SUBMISSION

Each contribution should include a submission form and the proposed contribution for publication(forms and guidelines can be found on the web-site). The submission form contains the paper title, details of the main author, the name of the workshop and a list of topics that most closely match its content. The contribution is a paper not exceeding 5 pages in 12pt, one column format. Extended abstracts of at least 2 pages describing work in progress can also be submitted.

IMPORTANT NOTE: In case of acceptance, the original paper submitted will be in the CD ROM (no changes after April 21st are accepted). Authors are required to provide a poster at the forum. The best papers may be published in an edited book.

Late contributions can be submitted until July 6. Only outstanding contributions will be accepted not exceed 20% of all accepted contributions.

FORM OF SUBMISSIONS	IMPORTANT DATES IN 2001	
Interested authors are invited to send the requested information in electronic format to both FDL General Chair and FDL Program Chair. Preferred electronic formats are in this order: PDF, RTF, Postscript. Compressed submissions are also accepted : GNU gzip, Unix compress, PKZip.	Paper or abstract contributions due Panel session & tutorial proposals Notification of acceptance Late contributions	**April 21** **May 11** **June 8** **July 6**
	FDL2001 Tutorials Workshops	**September 3-7** **September 3** **September 4-7**
CONTACT	**ADDRESSES**	
Anne Mignotte (General Chair)	L3i INSA Lyon Bâtiment B. Pascal 20, av A. Einstein, 69621 Villeurbanne cedex, France **Anne.Mignotte@insa-lyon.fr**	
Eugenio Villar (Program Chair)	Microelectronics Engineering Group E.T.S.I.Industriales y Telecom. University of Cantabria Avda. Los Castros s/n, 39005 Santander, Spain **villar@teisa.unican.es**	
John Willis (Hands-on-Labs Chair)	**jwillis@ftlsys.com**	
Ralf Seepold (Tutorial Chair)	**Seepold@fzi.de**	
Jean-Jacques Schwarz (Local Organization)	**fdl01@insa-lyon.fr**	

www.ecsi.org/ecsi/fdl/fdl01