

## CoreAHB2APB Datasheet

# **DirectCore**

### **Key Features**

- Supplied in SysBASIC Core Bundle
- Bridges between AMBA AHB and APB
- Up to 16 APB Slave Devices Supported
- Automatic Connection to CoreAHB and CoreAPB in CoreConsole

### **Benefits**

- Allows Easy Connection of APB Devices to a CoreMP7 Subsystem
- Auto Stitch in CoreConsole for Rapid Development
- Compatible with AMBA and CoreMP7

## **ARM Supported Families**

- ProASIC®3 (M7A3P)
- ProASIC3E (M7A3PE)
- Fusion (M7AFS)

## **Synthesis and Simulation Support**

 Supported in the Actel Libero<sup>®</sup> Integrated Design Environment (IDE)

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# **General Description**

CoreAHB2APB (AMBA Bridge) is an AHB slave that links the AHB to the APB and acts as the master on the APB. Address decoding for the APB is carried out within CoreAHB2APB, and this provides select signals for up to 16 APB slave slots.

Read and write transfers on the AHB are converted to corresponding transfers on the APB. High-bandwidth peripherals, such as memory controllers, are typically connected to the AHB, whereas the APB is used for less demanding peripherals, such as watchdogs. Unlike the AHB, transfers on the APB are not pipelined.

Figure 1 shows the CoreAHB2APB block diagram.

## **Verification and Compliance**

· Compliant with AMBA

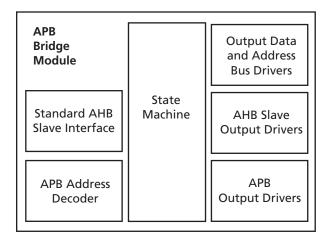


Figure 1 • CoreAHB2APB

# **Connecting CoreAHB2APB in CoreConsole**

Table 1 lists the ports present on the AMBA Bridge and describes how to connect these in CoreConsole.

Table 1 • AMBA Bridge Connections

Connection	CoreConsole Label	Description	
Required Connections			
AHB Slave Interface	AHBslave	Connect this to any of the 16 available slave slots on the AHB (CoreAHB).	
APB Master Interface	APBmaster	Connect this to the APBmaster interface on the APB (CoreAPB).	
HCLK	HCLK	AHB system clock input. Connect this to the HCLK output of the CoreMP7Bridge.	
HRESETn	HRESEETn	Active low AHB system reset. Connect this to the HCLK output of the CoreMP7Bridge.	

# **Resource Requirements**

The utilization for CoreAHB2APB in a ProASIC3E device is 250 tiles.

# **Ordering Information**

CoreAHB2APB is included in the SysBASIC core bundle that is supplied with the Actel CoreConsole IP Deployment Platform tool. The obfuscated RTL version of SysBASIC (SysBASIC-OC) is available for free with CoreConsole. The source RTL version of SysBASIC (SysBASIC-RM) can be ordered through your local Actel sales representative. CoreAHB2APB cannot be ordered separately from the SysBASIC core bundle.

2 Advanced v0.1

# **Datasheet Categories**

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," and "Production." The definitions of these categories are as follows:

### **Product Brief**

The product brief is a summarized version of an advanced or production datasheet containing general product information. This brief summarizes specific device and family information for unreleased products.

### **Advanced**

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

### **Unmarked (production)**

This datasheet version contains information that is considered to be final.

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