CoreGPIO Datasheet

DirectCore

Product Summary

Intended Use

- General Purpose Input/Output Block. Intended for Use in a CoreMP7-Based Subsystem to Read and Write to the External System in the Memory Map.

Key Features

- Supplied in SysBASIC Core Bundle
- 32 Unique Input and Output Pins per Core Implementation

Benefits

- Auto Stitch CoreGPIO in CoreConsole for Rapid Development
- Compatible with AMBA and CoreMP7

ARM Supported Families

- ProASIC®3 (M7A3P)
- ProASIC3E (M7A3PE)
- Fusion (M7AFS)

Synthesis and Simulation Support

- Supported in the Actel Libero® Integrated Design Environment (IDE)

Verification and Compliance

- Compliant with AMBA

Contents

General Description

CoreGPIO is an APB peripheral that provides 32 inputs and 32 outputs. There is a single register at offset 0x00 (and aliased throughout the slot). Writing to this register writes 32 bits to the outputs. Reading from the register reads the state of the inputs.

It is not required that all inputs and outputs are used. The user need only connect to those inputs and outputs which are actually used. Any unused inputs should be tied either high or low and unused outputs may be left unconnected.

Connecting CoreGPIO in CoreConsole

Table 1 lists the ports present on CoreGPIO and describes how to connect these in CoreConsole.

Table 1 • **GPIO Connections**

Connection	CoreConsole Label	Description
Required Connections		
APB Slave Interface	APBslave	Connect this interface to any available slave slot on the APB Bus.
PCLK	PCLK	APB clock signal. Normally connected to the HCLK output of the MP7Bridge.
PRESETn	PRESETn	Active low APB reset input. Normally connected to the HRESETn output of the MP7Bridge.
Optional Connections		
Input Data	dataIn	32-bit input data bus. This port provides the user with up to 32 inputs. Any unused input lines should be tied to a fixed value (high or low).
Output Data	dataOut	32-bit output data bus. This port provides up to 32 outputs. Any unused outputs may be left unconnected.

Programmer's Model

CoreGPIO contains a single 32-bit register, which is described in Table 2.

Table 2 • **GPIO Control/Status Register**

Bits	Name	Type	Function
31:0	I/O Control/ Status Register	Read/Write	A write to this register will set the values of the output lines.
			Reading this register gives the status of the input lines. The status is cleared on read.

Resource Requirements

The utilization for CoreGPIO in a ProASIC3E device is 100 tiles.

Ordering Information

CoreGPIO is included in the SysBASIC core bundle that is supplied with the Actel CoreConsole IP Deployment Platform tool. The obfuscated RTL version of SysBASIC (SysBASIC-OC) is available for free with CoreConsole. The source RTL version of SysBASIC (SysBASIC-RM) can be ordered through your local Actel sales representative. CoreGPIO cannot be ordered separately from the SysBASIC core bundle.

Datasheet Categories

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The product brief is a summarized version of an advanced or production datasheet containing general product information. This brief summarizes specific device and family information for unreleased products.

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This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

Unmarked (production)

This datasheet version contains information that is considered to be final.

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Actel Corporation	**Actel Europe Ltd.**	**Actel Japan** www.jp.actel.com	**Actel Hong Kong** www.actel.com.cn
2061 Stierlin Court Mountain View, CA 94043-4655 USA	Dunlop House, Riverside Way Camberley, Surrey GU15 3YL United Kingdom	EXOS Ebisu Bldg. 4F 1-24-14 Ebisu Shibuya-ku Tokyo 150 Japan	Suite 2114, Two Pacific Place 88 Queensway, Admiralty Hong Kong
Phone 650.318.4200 **Fax** 650.318.4600	**Phone** +44 (0) 1276 401 450 **Fax** +44 (0) 1276 401 490	**Phone** +81.03.3445.7671 **Fax** +81.03.3445.7668	**Phone** +852 2185 6460 **Fax** +852 2185 6488