CoreInterrupt

Product Summary

Intended Use

- Use As a Small-Footprint, Flexible Interrupt Controller for Advanced Microcontroller Bus Architecture (AMBA)–Based Systems and in Conjunction with CoreMP7

Key Features

- Optimized for Use with CoreMP7
- 0 to 32 Interrupt Request Line (IRQ) Interrupt Sources
- 0 to 8 Fast Interrupt Request (FIQ) Sources
- Supplied in SysBASIC Core Bundle

Benefits

- Expand the Number of Interrupts in Your Processor Subsystem
- Automatically Stitch into Your System in CoreConsole
- Compatible with AMBA and CoreMP7

ARM Supported Families

- ProASIC®3 (M7A3P)
- ProASIC3E (M7A3PE)
- Fusion (M7AFS)

Synthesis and Simulation support

- Supported in the Actel Libero® Integrated Design Environment (IDE)

Verification and Compliance

- Compliant with AMBA

Contents

Introduction

The CoreInterrupt module is an Advanced Peripheral Bus (APB) slave that provides configurable interrupt processing. Figure 1 shows a top-level block diagram of CoreInterrupt.

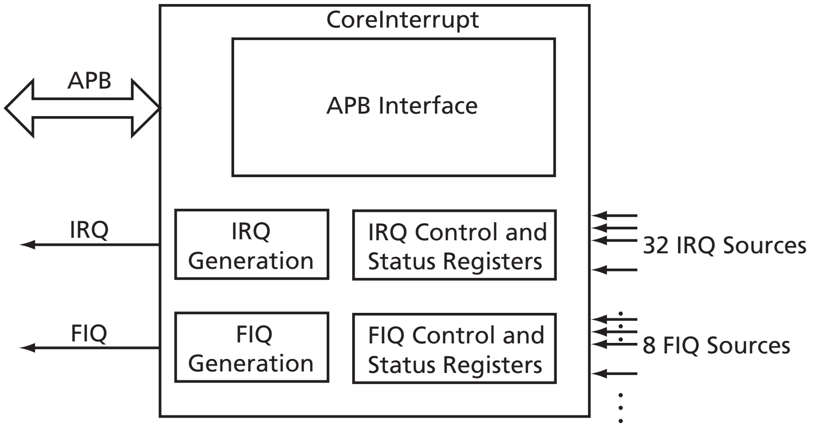

Figure 1 • **CoreInterrupt Block Diagram**

Functional Description

CoreInterrupt supports 0 to 32 IRQ sources and 0 to 8 FIQ sources. The IRQ and FIQ source inputs are level-sensitive, active high ports. These interrupt sources are processed to produce two output interrupt lines: IRQ and FIQ.

All interrupt processing is combinatorial; that is, the paths from the IRQ/FIQ source inputs to the IRQ/FIQ output contain no flip-flops. Peripherals that drive the interrupt source inputs must ensure that their interrupts remain asserted until they are serviced. CoreInterrupt performs no synchronization of source inputs, so any necessary synchronization should be handled externally.

Software driven IRQ/FIQ interrupts are supported, and each IRQ/FIQ source can be individually enabled or disabled via control registers.

FIQ Processing

Up to eight FIQ source inputs are processed to produce the FIQ output.

If less than eight FIQ sources are being used, the lower-order FIQ source inputs (from fiqSource0 upwards) should be used, and the upper inputs should be left unconnected. CoreConsole will automatically tie off any unused inputs to inactive levels. The **Number of FIQ Sources** configurable option should be set equal to the number of FIQ source inputs being used to minimize the area requirement for CoreInterrupt.

It is feasible to set the **Number of FIQ Sources** configurable option to eight and not make a connection to all eight FIQ source inputs; however, CoreInterrupt will then use up more area than is necessary.

The FIQ soft interrupt control register, FIQSoftInt, can be used to force an FIQ source active (high) under software control. Bits in the FIQSoftInt register are cleared by writing to the FIQSoftIntClear address.

The FIQ enable register, FIQEnable, can be used to enable or mask out particular FIQ interrupt sources. A high bit in the FIQEnable register indicates that the corresponding FIQ source input is enabled. Bits in the FIQEnable register are cleared by writing to the FIQEnableClear address.

The **FIQ Active Level** configurable option can be used to control whether the FIQ output is active low or active high. The default is active low, which is compatible with the CoreMP7 processor's FIQ input.

IRQ Processing

Up to 32 IRQ source inputs are processed to produce the IRQ output.

If less than 32 IRQ sources are being used, the lower-order IRQ source inputs (from irqSource0 upwards) should be used, and the upper inputs should be left unconnected. CoreConsole will automatically tie off any unused inputs to inactive levels. The **Number of IRQ Sources** configurable option should be set equal to the number of IRQ source inputs being used to minimize the area requirement for CoreInterrupt.

It is feasible to set the **Number of IRQ Sources** configurable option to 32 and not make a connection to all 32 IRQ source inputs; however, CoreInterrupt will then use up more area than is necessary.

The IRQ soft interrupt control register, IRQSoftInt, can be used to force an IRQ source active (high) under software control. Bits in the IRQSoftInt register are cleared by writing to the IRQSoftIntClear address.

The IRQ enable register, IRQEnable, can be used to enable or mask out particular IRQ sources. A high bit in the IRQEnable register indicates that the corresponding IRQ source input is enabled. Bits in the IRQEnable register are cleared by writing to the IRQEnableClear address.

The **IRQ Active Level** configurable option can be used to control whether the IRQ output is active low or active high. The default is active low, which is compatible with the CoreMP7 processor's IRQ input.

Connecting CoreInterrupt in CoreConsole

Table 1 lists the ports present on the CoreInterrupt module and describes how to connect these in CoreConsole.

Table 1 • **CoreInterrupt Connections**

Connection	CoreConsole Label	Description
Required Connections		
APB slave interface	APBslave	Connect this interface to any available slave slot on the APB Bus.
PCLK	PCLK	APB clock signal. Normally connected to the HCLK output of the MP7Bridge.
PRESETn	PRESETn	Active low APB reset input. Normally connected to the HRESETn output of the MP7Bridge.
Optional Connections		
Interrupt request	IRQ	Interrupt request output. The polarity of this signal is controlled by the **IRQ Active Level** configurable option and is active low by default. Normally connected to the IRQ port of MP7Bridge.
Fast interrupt request	FIQ	Fast interrupt request output. The polarity of this signal is controlled by the **FIQ Active Level** configurable option and is active low by default. Normally connected to the FIQ port of MP7Bridge.
IRQ source 0	irqSource0	Active high input for IRQ source 0. Tied low if no connection is made to this port.
…		
IRQ source 31	irqSource31	Active high input for IRQ source 31. Tied low if no connection is made to this port.
FIQ source 0	fiqSource0	Active high input for FIQ source 0. Tied low if no connection is made to this port.
…		
FIQ source 7	fiqSource7	Active high input for FIQ source 7. Tied low if no connection is made to this port.

CoreInterrupt Configurable Options

The configurable options for CoreInterrupt are described in Table 2.

Table 2 • **CoreInterrupt Configurable Options**

Configurable Option	Default Setting	Description
Number of FIQ Sources	0	Sets the number of interrupt sources that are processed to produce the FIQ output. There are always eight individual FIQ source inputs present on CoreInterrupt, but some of these are effectively redundant if the number of FIQ sources is less than eight. If the number of FIQ sources is less than eight, then the lower-numbered source inputs should be used first—that is, from fiqSource0 upwards. For example, if the number of FIQ sources is set to four, only inputs fiqSource0 to fiqSource3 are active, and any signals connected to inputs fiqSource4 to fiqSource7 will not contribute to the FIQ output. Possible settings: 0 to 8
Number of IRQ Sources	8	Sets the number of interrupt sources that are processed to produce the IRQ output. There are always 32 individual IRQ source inputs present on CoreInterrupt, but some of these are effectively redundant if the number of IRQ sources is less than 32. If the number of IRQ sources is less than 32, then the lower-numbered source inputs should be used first—that is, from irqSource0 upwards. For example, if the number of IRQ sources is set to eight, only inputs irqSource0 to irqSource7 are active, and any signals connected to inputs irqSource8 to irqSource31 will not contribute to the IRQ output. Possible settings: 0 to 32
FIQ Active Level	Low	Determines the active level for the FIQ output. Possible settings: High or Low
IRQ Active Level	Low	Determines the active level for the IRQ output. Possible settings: High or Low

Programmer's Model

Table 3 summarizes the CoreInterrupt registers.

Table 3 • **CoreInterrupt Registers**

Offset	Read/Write	Width	Reset Value	Name	Description
0x00	R/W	0 to 8	0	FIQSoftInt	FIQ soft interrupt register.
0x04	W	0 to 8	–	FIQSoftIntClear	FIQ soft interrupt clear register.
0x08	R/W	0 to 8	0	FIQEnable	FIQ enable register.
0x0C	W	0 to 8	–	FIQEnableClear	FIQ enable clear register.
0x10	R	0 to 8	0	FIQRawStatus	FIQ raw status register.
0x14	R	0 to 8	0	FIQStatus	FIQ status register.
0x18	R/W	0 to 32	0	IRQSoftInt	IRQ soft interrupt register.
0x1C	W	0 to 32	–	IRQSoftIntClear	IRQ soft interrupt clear register.
0x20	R/W	0 to 32	0	IRQEnable	IRQ enable register.
0x24	W	0 to 32	–	IRQEnableClear	IRQ enable clear register.
0x28	R	0 to 32	0	IRQRawStatus	IRQ raw status register.
0x2C	R	0 to 32	0	IRQStatus	IRQ status register.

FIQ Soft Interrupt Register – FIQSoftInt

If the **Number of FIQ Sources** configurable option is set to 0, this register has no function and reads 0. Otherwise, the width of this register is equal to the number of FIQ sources configured.

This read/write register provides a mechanism for software generated interrupts. A high bit in this register is equivalent to the corresponding FIQ source being asserted (high).

A bit in this register is set by writing a '1' in the appropriate bit position; writing a '0' has no effect and does not clear the corresponding bit. Bits in the FIQSoftInt register are cleared by writing to the FIQSoftIntClear register.

FIQ Soft Interrupt Clear Register – FIQSoftIntClear

If the **Number of FIQ Sources** configurable option is set to 0, this register has no function and reads 0. Otherwise, the width of this register is equal to the number of FIQ sources configured.

This write-only register is used for clearing bits in the FIQSoftInt register. Writing a '1' in any bit position will clear the corresponding bit in the FIQSoftInt register. Writing a '0' has no effect.

FIQ Enable Register – FIQEnable

If the **Number of FIQ Sources** configurable option is set to 0, this register has no function and reads 0. Otherwise, the width of this register is equal to the number of FIQ sources configured.

This read/write register provides a means of masking FIQ sources. A '1' in any bit position in this register enables the corresponding FIQ source, and a '0' masks the corresponding source. The masking provided by this register applies whether the interrupt source is driven by hardware (via one of the fiqSourcex inputs) or software (via the FIQSoftInt register).

A bit in this register is set by writing a '1' in the appropriate bit position; writing a '0' has no effect and does not clear the corresponding bit. Bits in the FIQEnable register are cleared by writing to the FIQEnableClear register.

FIQ Enable Clear Register – FIQEnableClear

If the **Number of FIQ Sources** configurable option is set to 0, this register has no function and reads 0. Otherwise, the width of this register is equal to the number of FIQ sources configured.

This write-only register is used for clearing bits in the FIQEnable register. Writing a '1' in any bit position will clear the corresponding bit in the FIQEnable register. Writing a '0' has no effect.

FIQ Raw Status Register – FIQRawStatus

If the **Number of FIQ Sources** configurable option is set to 0, this register has no function and reads 0. Otherwise, the width of this register is equal to the number of FIQ sources configured.

This read-only register gives the state of the FIQ sources. A '1' indicates an active interrupt source, which may be driven by either hardware (via one of the fiqSourcex inputs) or software (via the FIQSoftInt register).

FIQ Status Register – FIQStatus

If the **Number of FIQ Sources** configurable option is set to 0, this register has no function and reads 0. Otherwise, the width of this register is equal to the number of FIQ sources configured.

This read-only register indicates the status of the FIQ sources after any masking provided by the FIQEnable register has been applied.

IRQ Soft Interrupt Register – IRQSoftInt

If the **Number of IRQ Sources** configurable option is set to 0, this register has no function and reads 0. Otherwise, the width of this register is equal to the number of IRQ sources configured.

This read/write register provides a mechanism for software generated interrupts. A high bit in this register is equivalent to the corresponding IRQ source being asserted (high).

A bit in this register is set by writing a '1' in the appropriate bit position; writing a '0' has no effect and does not clear the corresponding bit. Bits in the IRQSoftInt register are cleared by writing to the IRQSoftIntClear register.

IRQ Soft Interrupt Clear Register – IRQSoftIntClear

If the **Number of IRQ Sources** configurable option is set to 0, this register has no function and reads 0. Otherwise, the width of this register is equal to the number of IRQ sources configured.

This write-only register is used for clearing bits in the IRQSoftInt register. Writing a '1' in any bit position will clear the corresponding bit in the IRQSoftInt register. Writing a '0' has no effect.

IRQ Enable Register – IRQEnable

If the **Number of IRQ Sources** configurable option is set to 0, this register has no function and reads 0. Otherwise, the width of this register is equal to the number of IRQ sources configured.

This read/write register provides a means of masking IRQ sources. A '1' in any bit position in this register enables the corresponding IRQ source, and a '0' masks the corresponding source. The masking provided by this register applies whether the interrupt source is driven by hardware (via one of the irqSourcex inputs) or software (via the IRQSoftInt register).

A bit in this register is set by writing a '1' in the appropriate bit position; writing a '0' has no effect and does not clear the corresponding bit. Bits in the IRQEnable register are cleared by writing to the IRQEnableClear register.

IRQ Enable Clear Register – IRQEnableClear

If the **Number of IRQ Sources** configurable option is set to 0, this register has no function and reads 0. Otherwise, the width of this register is equal to the number of IRQ sources configured.

This write-only register is used for clearing bits in the IRQEnable register. Writing a '1' in any bit position will clear the corresponding bit in the IRQEnable register. Writing a '0' has no effect.

IRQ Raw Status Register – IRQRawStatus

If the **Number of IRQ Sources** configurable option is set to 0, this register has no function and reads 0. Otherwise, the width of this register is equal to the number of IRQ sources configured.

This read-only register gives the state of the IRQ sources. A '1' indicates an active interrupt source, which may be driven by either hardware (via one of the irqSourcex inputs) or software (via the IRQSoftInt register).

IRQ Status Register – IRQStatus

If the **Number of IRQ Sources** configurable option is set to 0, this register has no function and reads 0. Otherwise, the width of this register is equal to the number of IRQ sources configured.

This read-only register indicates the status of the IRQ sources after any masking provided by the IRQEnable register has been applied.

Resource Requirements

Table 4 gives the approximate tile counts required for CoreInterrupt for a variety of configurations in a ProASIC3E device.

Table 4 • **CoreInterrupt Device Utilization for ProASIC3E**

Number of FIQ Sources	Number of IRQ Sources	Tile Count
8	32	549
4	16	292
1	16	261
1	8	132
0	8	139
1	4	87
0	4	68

Ordering Information

CoreInterrupt is included in the SysBASIC core bundle that is supplied with the Actel CoreConsole IP Deployment Platform tool. The obfuscated RTL version of SysBASIC (SysBASIC-OC) is available for free with CoreConsole. The source RTL version of SysBASIC (SysBASIC-RM) can be ordered through your local Actel sales representative. CoreInterrupt cannot be ordered separately from the SysBASIC core bundle.

Datasheet Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," and "Production." The definitions of these categories are as follows:

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The product brief is a summarized version of an advanced or production datasheet containing general product information. This brief summarizes specific device and family information for unreleased products.

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This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

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www.actel.com

Actel Corporation

2061 Stierlin Court
Mountain View, CA
94043-4655 USA
Phone 650.318.4200
Fax 650.318.4600

Actel Europe Ltd.

Dunlop House, Riverside Way
Camberley, Surrey GU15 3YL
United Kingdom
Phone +44 (0) 1276 401 450
Fax +44 (0) 1276 401 490

Actel Japan
www.jp.actel.com
EXOS Ebisu Bldg. 4F
1-24-14 Ebisu Shibuya-ku
Tokyo 150 Japan
Phone +81.03.3445.7671
Fax +81.03.3445.7668

Actel Hong Kong
www.actel.com.cn
Suite 2114, Two Pacific Place
88 Queensway, Admiralty
Hong Kong
Phone +852 2185 6460
Fax +852 2185 6488