CoreMP7 User's Guide

Actel®

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Trademarks

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Introduction

The CoreMP7 is an Actel technology optimized ARM7™ processor and is fully compatible with the ARM7 architecture. For further information on the ARM7 architecture, refer to the *ARM7 Technical Reference Manual* (DDI0234A-7TMIS-R4.pdf), published by ARM® Corporation, available for download from the ARM website (www.arm.com).

The CoreMP7 is supplied with an MP7Bridge (see Figure 3-1 on page 13) for interfacing to an Advanced Microcontroller Bus Architecture (AMBA) Advanced High-Performance Bus (AHB) based bus system such as the one generated by the Actel CoreConsole IP Deployment Platform (IDP). CoreConsole is used to create a system project which can be directly imported into the Actel Libero® Integrated Design Environment (IDE) for simulation, synthesis, layout, and bitstream generation for Actel FPGAs.

CoreMP7 Processor

The CoreMP7 is a general purpose 32-bit microprocessor offering high performance and low power consumption. It is fully compatible with the ARM7TDMI-S™ processor from ARM. The ARM architecture is based on Reduced Instruction Set Computer (RISC) principles. The RISC simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective processor core. Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

1 Software Development

ARM has developed a version of their RealView Developer Suite for use with CoreMP7 called the RealView Developer Kit (RVDK). The RVDK is available from Actel and provides a complete development environment for embedded systems applications running on CoreMP7. It consists of a suite of tools, together with supporting documentation and examples. The tools enable you to write, build, and debug the software program for your application, either on target hardware or on a software simulator.

You can use the compilation tools to build C, C++, or ARM assembly language programs. The following tools are included in the RVDK:

- ARM and Thumb® C and C++ compiler, armcc
- ARM and Thumb assembler, armasm
- ARM linker, armlink
- ARM librarian, armar
- ARM image conversion utility, fromelf
- Supporting libraries

There are other tools included in the RVDK as well, such as the RealView Debugger.

The interface and project management of RVDK is provided by the RealView Debugger.

A full set of manuals is provided by ARM with the RVDK.

2

CoreMP7 Design Entry Flow

The Libero IDE automatically manages CoreMP7 through various point tools when it is instantiated in a CoreConsole project system design. The project system can consist of only the CoreMP7 itself or it can include a range of subsystem and higher level IP blocks. The overall flow is shown in Figure 2-1.

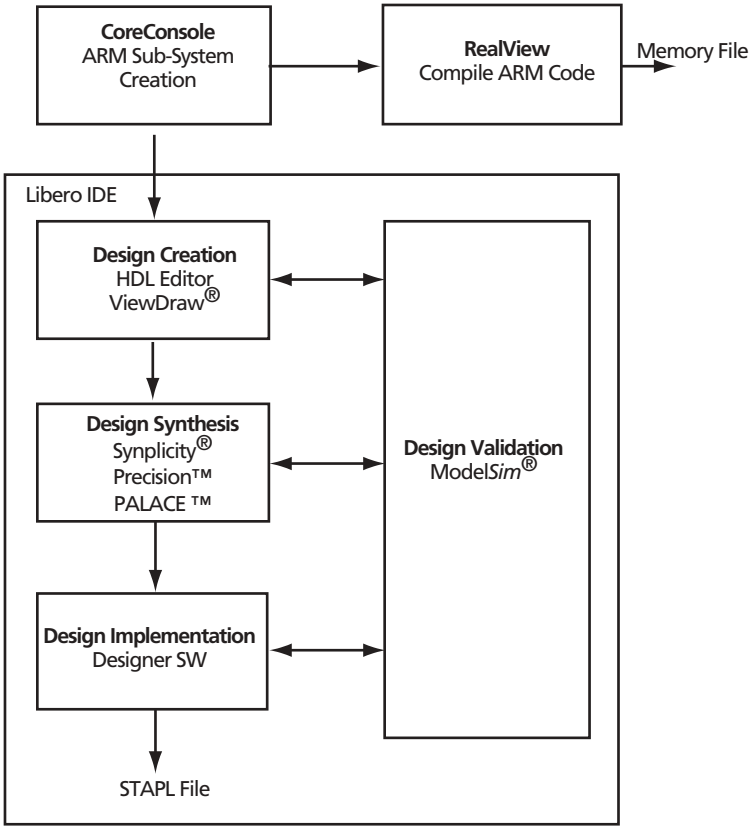

Figure 2-1. MP7 Design Entry Flow

To import a CoreConsole project into the Libero IDE, locate the CCP file for that project in the CoreConsole Libero IDE Export folder hierarchy. The CCP file is an XML file that fully describes

the CoreConsole project. It appears in the CoreConsole Projects section of the Libero IDE as shown in Figure 2-2.

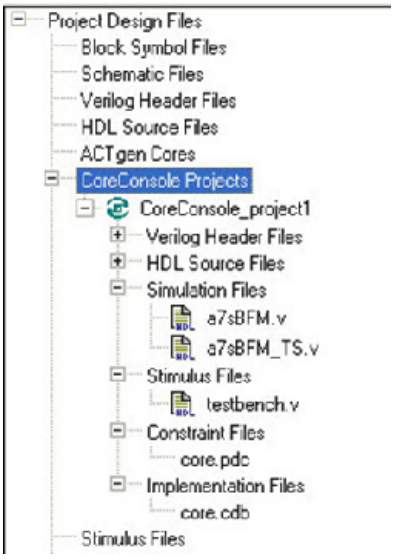

Figure 2-2. CoreConsole Project Section in Libero IDE

The CoreMP7 files associated with this flow are shown in Figure 2-3. Normally the CoreConsole system project imported into Libero IDE consists of a range of RTL IP components alongside the CoreMP7 that is implemented in a secure format that can only be read and used within the tools utilized by the Libero IDE.

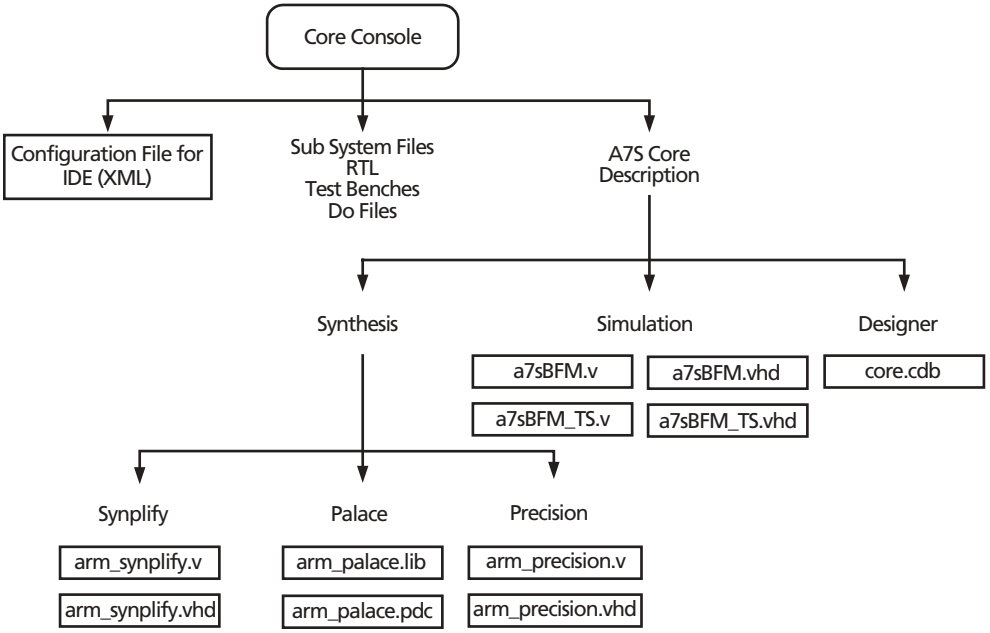

Figure 2-3. CoreMP7 File Flow

The Libero IDE manages all the files imported from CoreConsole, and passes them to the appropriate tools. The secure CoreMP7 implementation is represented inside the Libero IDE as A7S when the RTL wrapping has been removed (See Figure 2-4 and Figure 2-5).

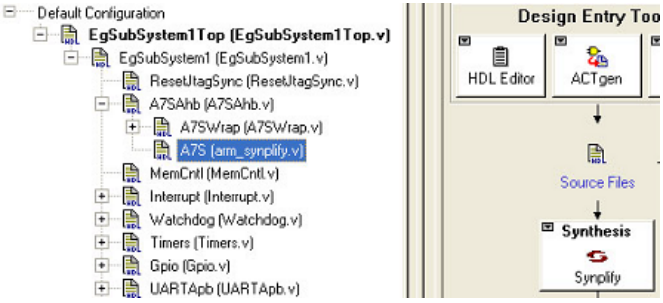

Figure 2-4. A7S Synplify in the Libero IDE

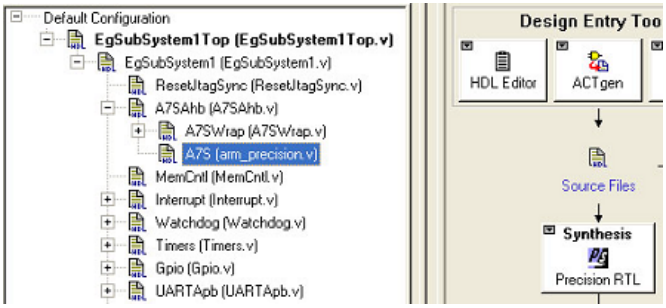

Figure 2-5. A7S Precision in the Libero IDE

CoreMP7 Security

CoreMP7 is imported as a CDB file along with a netlist that instantiates the CoreMP7 core. The CoreMP7 core is delivered in a blackbox that allows you to access the top-level I/O and use the core in Actel M7 ProASIC3/E devices. The contents of the blackbox are kept from view. The CoreMP7 core top-level interface is visible (external ports that need to be routed to the rest of the design). Timing constraints and analysis are done at the interface of the CoreMP7 core. The placement and routing of the CoreMP7 within the FPGA fabric core is fixed. The Libero IDE is aware of the core's placement and will fill in the unused tiles around the core with the IP that you have put together around CoreMP7 in your CoreConsole project system. The CoreMP7 blackbox cannot be unlocked, and can only be programmed in M7 ProASIC3/E devices.

3

CoreMP7Bridge Wrapper

CoreMP7Bridge is an important component used when building a CoreMP7-based project system. CoreMP7Bridge converts the native signals from the CoreMP7 processor into an AMBA AHB master interface suitable for connection to an AHB bus. It also includes circuitry that handles reset signals and the signals that connect to the ARM RealView ICE JTAG port, and a debug interface suitable for using GDB via FlashPro3. The incoming hardware reset signal is synchronized to the system clock, and provision is made for handling a watchdog generated reset when a watchdog component is included in the system. Some circuitry to condition the RealView ICE signals is also included.

The details of CoreMP7Bridge are covered in the *CoreMP7Bridge datasheet*. The interface is shown in Figure 3-1.

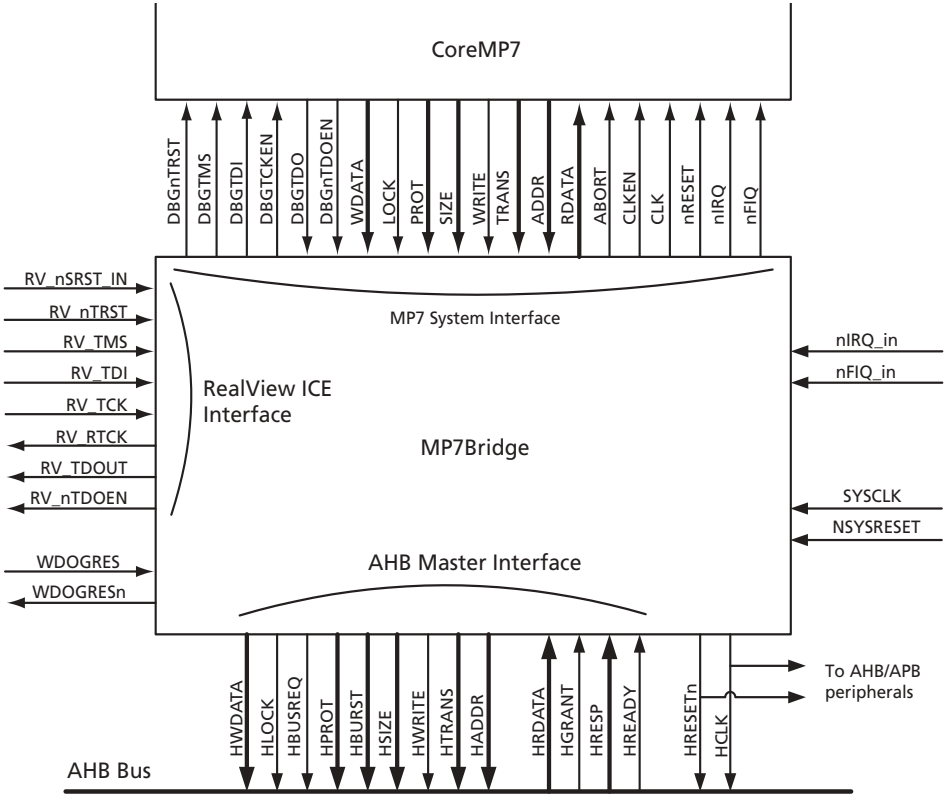

Figure 3-1. Interfacing CoreMP7 with MP7Bridge

4

Debug

The ARM debug architecture uses a protocol converter box to allow the RVDK debugger to talk via a Joint Test Action Group (JTAG) port directly to the core. The scan chains in the core that are required for test are reused for debugging.

The architecture uses the scan chains to insert instructions directly in to the ARM core. The instructions are executed on the core and, depending on the type of instruction that has been inserted, the core or the system state can be examined, saved, or changed. The architecture has the ability to execute instructions at a slow debug speed, or to execute instructions at system speed (for example if access to an external memory was required).

The fact that the debugger is using the JTAG scan chains to access the core is not a problem, because the front-end debugger remains the same. You can still use the debugger with a monitor program running on the target system, or with an Instruction Set Simulator that runs on the debugger host. In either case the debugging environment is the same.

The advantages of using the JTAG port are:

- Hardware access required by a system for test is re-used for debug.
- Core state and system state can be examined via the JTAG port.
- The target system does not have to be running in order to start the debug. A monitor program, for example, requires that some target resources are running in order for the monitor program to run.
- The traditional breakpoints and watchpoints are available.
- On-chip resources can be added to.

The debugging of the target system requires the following:

- A host computer to run the debugger software. The host could be a PC running Windows® or Linux, or a Sun workstation.
- An EmbeddedICE Protocols Converter. This is a separate box that converts the serial interface to signals compatible with the JTAG interface, and a target system with a JTAG interface and an ARM debug architecture compliant core.

Once the system is connected, the debugger can start communicating with the target system via the RVI-ME (one of the types of EmbeddedICE Interface Converters).

The debug extensions consist of several scan chains around the processor core and some additional signals that are used to control the behavior of the core for debug purposes. The most significant of these additional signals are described below.

BREAKPT

This core signal enables external hardware to halt processor execution for debug purposes. When HIGH during an instruction fetch, the instruction is tagged as breakpointed, and the core stops if this instruction reaches execute.

DBGRQ

This core signal is a level-sensitive input that causes the CPU core to enter debug state when the current instruction has completed.

DBGACK

This core signal is an output from the CPU core that goes HIGH when the core is in debug state so that external devices can determine the current state of the core.

RealView ICE uses these and other signals, through the debug interface of the processor core, for example, by writing to the control register of the EmbeddedICE logic.

JTAG Debug Interface

The RVI-ME ICE run control unit is supplied with a short ribbon cable. These both terminate in a 20-way 2.54 mm pitch IDC connector. You can use the cable to mate with a keyed box header on the target. The pinout is shown in Figure 4-1.

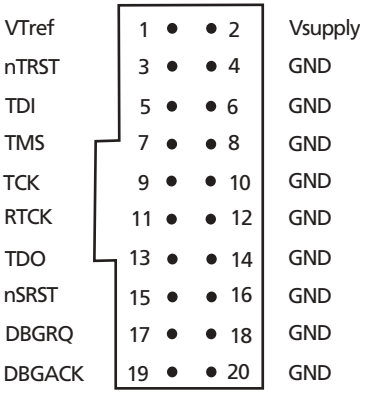

Figure 4-1. JTAG Interface Pinout

The signals on the JTAG interface are shown in Table 4-1.

Table 4-1. JTAG signals

Signal	I/O	Description
DBGACK	–	This pin is connected in the RealView ICE run control unit, but is not supported in the current release of the software. It is reserved for compatibility with other equipment to be used as a debug acknowledge signal from the target system. It is recommended that this signal is pulled LOW on the target.
DBGRQ_	–	This pin is connected in the RealView ICE run control unit, but is not supported in the current release of the software. It is reserved for compatibility with other equipment to be used as a debug request signal to the target system. This signal is tied LOW. When applicable, RealView ICE uses the core's scanchain 2 to put the core in debug state. It is recommended that this signal is pulled LOW on the target.
GND	–	Ground
nSRST	Input/ output	Open collector output from RealView ICE to the target system reset. This is also an input to RealView ICE so that a reset initiated on the target can be reported to the debugger. This pin must be pulled HIGH on the target to avoid unintentional resets when there is no connection.
nTRST	Output	Open collector output from RealView ICE to the Reset signal on the target JTAG port. This pin must be pulled HIGH on the target to avoid unintentional resets when there is no connection.
RTCK	Input	Return Test Clock signal from the target JTAG port to RealView ICE. Some targets must synchronize the JTAG inputs to internal clocks. To assist in meeting this requirement, you can use a returned and retimed TCK to dynamically control the TCK rate. RealView ICE provides Adaptive Clock Timing that waits for TCK changes to be echoed correctly before making further changes. Targets that do not have to process TCK can simply ground this pin.
TCK	Output	Test Clock signal from RealView ICE to the target JTAG port. It is recommended that this pin is pulled LOW on the target.
TDI	Output	Test Data In signal from RealView ICE to the target JTAG port. It is recommended that this pin is pulled HIGH on the target.
TDO	Input	Test Data Out from the target JTAG port to RealView ICE. It is recommended that this pin is pulled HIGH on the target.

Table 4-1. JTAG signals (Continued)

Signal	I/O	Description
TMS	Output	Test Mode signal from RealView ICE to the target JTAG port. This pin must be pulled HIGH on the target so that the effect of any spurious TCKs when there is no connection is benign.
Vsupply	Input	This pin is not connected in the RealView ICE run control unit. It is reserved for compatibility with other equipment to be used as a power feed from the target system.
VTref	Input	This is the target reference voltage. It indicates that the target has power, and it must be at least 0.628 V. VTref is normally fed from Vdd on the target hardware and might have a series resistor (though this is not recommended). There is a 10 kΩ pull-down resistor on VTref in RealView ICE.

The EmbeddedICE logic which implements the on-chip debug function in the CoreMP7 debug architecture is described in detail in the *ARM7TDMI-S (rev 4) Technical Reference Manual* (ARM DDI0234A), published by ARM Limited, and is available via Internet at http://www.arm.com.

The CoreMP7 debug architecture uses a JTAG port as a method of accessing the core. The debug architecture uses EmbeddedICE logic which resides on chip with the CoreMP7 core. The EmbeddedICE has its own scan chain that is used to insert watchpoints and breakpoints for the CoreMP7. The EmbeddedICE logic consists of two real time watchpoint registers, together with a control and status register. One or both of the watchpoint registers can be programmed to halt the CoreMP7 core. Execution is halted when a match occurs between the values programmed into the EmbeddedICE logic and the values currently appearing on the address bus, data bus, and some control signals. Any bit can be masked so that its value does not affect the comparison. Either watchpoint register can be configured as a watchpoint (i.e., on a data access) or a break point (i.e., on an instruction fetch). The watchpoints and breakpoints can be combined such that:

- The conditions on both watchpoints must be satisfied before the ARM7TDMI core is stopped. The CHAIN functionality requires two consecutive conditions to be satisfied before the core is halted. An example of this would be to set the first breakpoint to trigger on an access to a peripheral, and the second to trigger on the code segment that performs the task switching. Therefore when the breakpoints trigger, the information regarding which task has switched out will be ready for examination.
- The watchpoints can be configured such that a range of addresses are enabled for the watchpoints to be active. The RANGE function allows the breakpoints to be combined such that a breakpoint is to occur if an access occurs in the bottom 256 bytes of memory but not in the bottom 32 bytes.

The CoreMP7 has a built-in debug communication channel function. The debug communication channel allows a program running on the target to communicate with the host debugger or another separate host without stopping the program flow, or even entering the debug state. The debug communication channel is accessed as a co-processor 14 by the program running on the CoreMP7 core. The debug communication channel allows the JTAG port to be used for sending and receiving data without affecting the normal program flow. The debug communication channel data and control registers are mapped in to addresses in the EmbeddedICE logic. The signals in the debug communication channel are listed in Table 4-2.

Table 4-2. Debug Communication Channel Signals

Signal Name	Type	Description
TMS	Input	Test Mode Select. The TMS pin selects the next state in the TAP state machine.
TCK	Input	Test Clock. This allows shifting of the data in, on the TMS and TDI pins. It is a positive edge triggered clock with the TMS and TCK signals that define the internal state of the device.
TDI	Input	Test Data In. This is the serial data input for the shift register.
TDO	Output	Test Data Output. This is the serial data output from the shift register. Data is shifted out of the device on the negative edge of the TCK signal.
nTRST	Input	Test Reset. The nTRST pin can be used to reset the test logic within the EmbeddedICE logic.
RTCK	Output	Returned Test Clock. Extra signal added to the JTAG port. Required for designs based on COREMP7 processor core. Multi-ICE (Development System from ARM) uses this signal to maintain synchronization with targets having slow or widely varying clock frequency. For details, refer to *Multi-ICE System Design Considerations Application Note 72 (ARM DAI 0072A)*.

The EmbeddedICE logic contains 16 registers as shown in Table 4-3. The CoreMP7 debug architecture is described in detail in the *ARM7TDMI-S (rev 4) Technical Reference Manual* (ARM DDI 0234A) published by ARM Limited, and is available via Internet at http://www.arm.com.

Table 4-3. Debug Communication Channel Registers

Name	Width	Description	Address
Debug Control	6	Force debug state, disable interrupts	00000
Debug Status	5	Status of debug	00001
Debug Comms Control Register	32	Debug communication control register	00100
Debug Comms Data Register	32	Debug communication data register	00101
Watchpoint 0 Address Value	32	Holds watchpoint 0 address value	01000
Watchpoint 0 Address Mask	32	Holds watchpoint 0 address mask	01001
Watchpoint 0 Data Value	32	Holds watchpoint 0 data value	01010
Watchpoint 0 Data Mask	32	Holds watchpoint 0 data mask	01011
Watchpoint 0 Control Value	9	Holds watchpoint 0 control value	01100
Watchpoint 0 Control Mask	8	Holds watchpoint 0 control mask	01101
Watchpoint 1 Address Value	32	Holds watchpoint 1 address value	10000
Watchpoint 1 Address Mask	32	Holds watchpoint 1 address mask	10001
Watchpoint 1 Data Value	32	Holds watchpoint 1 data value	10010
Watchpoint 1 Data Mask	32	Holds watchpoint 1 data mask	10011
Watchpoint 1 Control Value	9	Holds watchpoint 1 control value	10100
Watchpoint 1 Control Mask	8	Holds watchpoint 1 control mask	10101

A

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From South Central U.S.A., call **650.318.4434**
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From Canada, call **650.318.4480**
From Europe, call **650.318.4252** or **+44 (0) 1276 401 500**
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Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. Several ways of contacting the Center follow:

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is tech@actel.com.

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Our Technical Support Center answers all calls. The center retrieves information, such as your name, company name, phone number and your question, and then issues a case number. The Center then forwards the information to a queue where the first available application engineer receives the data and returns your call. The phone hours are from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. The Technical Support numbers are:

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