CoreMemCtrl Datasheet

DirectCore

Product Summary

Intended Use

- Intended for Use in a CoreMP7-Based Subsystem to Interface to External Flash or SRAM

Key Features

- Supplied in SysBASIC Core Bundle
- Two Independent Flash and SRAM AHB Port for Separate Addressing
- Configurable External Memory Interfaces
- Automatic Correct Connection to CoreAHB and CoreAHBLite in CoreConsole

Benefits

- Allows Easy Integration of External Memory Resources in a CoreMP7 Subsystem
- Auto Stitch in CoreConsole for Rapid Development
- Compatible with AMBA and CoreMP7

ARM Supported Families

- ProASIC®3 (M7A3P)
- ProASIC3E (M7A3PE)
- Fusion (M7AFS)

Synthesis and Simulation Support

- Supported in the Actel Libero® Integrated Design Environment (IDE)

Verification and Compliance

- Compliant with AMBA

Contents

General Description

CoreMemCtrl is an AHB slave component which supports access to external SRAM and Flash memory resources.

CoreMemCtrl uses two slave slots on the AHB Bus. One slot is allocated to the SRAM, another to the Flash.

CoreAHB and CoreAHBLite have a Remap input that can be used to select whether SRAM or Flash appears at slot0. Typically the Flash slave interface is connected to slot0 and the SRAM slave interface to slot1. If Auto Stitching is used in CoreConsole, these connections will be made automatically.

Connecting CoreMemCtrl in CoreConsole

Table 1 lists the ports present on CoreMemCtrl and describes how to connect these in CoreConsole.

Table 1 • **Memory Controller Connections**

Connection	CoreConsole Label	Description
Required Connections		
Flash AHB slave interface	AHBslave_flash	This interface groups together all of the signals used to connect the Flash memory region to an AHB slot. Normally connected to slave slot0 (AHBmslave0) of the AHB bus.
SRAM AHB slave interface	AHBslave_sram	This interface groups together all of the signals used to connect the SRAM memory region to an AHB slot. Normally connected to slave slot1 (AHBmslave1) of the AHB bus.
External Memory Interface	ExternalMemoryInterface	This interface contains the signals used to connect to the actual memory devices and should be routed to the top-level of your subsystem.
HCLK	HCLK	AHB system clock input. Connect this to the HCLK output of the MP7Bridge.
HRESETn	HRESETn	Active low AHB system reset. Connect this to the HRESETn output of the MP7Bridge.

External Memory Interface

The External Memory Interface of the Memory Controller should be routed to the subsystem top-level to facilitate communication with Flash and SRAM resources.

CoreMemCtrl is designed to accommodate a variety of Flash and SRAM configurations. For this reason, the External

Memory Interface is somewhat generic in nature in order to enable connection to a range of different memory devices and memory systems.

Memory devices typically have a number of inputs that are fixed at static levels which are dependent on the particular memory architecture in place. If the memory devices in your system have such static inputs, it is intended that these are handled in the top-level description for your FPGA device; that is, above the subsystem top-level.

Similarly, any tri-state buffers must be instantiated above the subsystem top-level. The data bus connecting between the FPGA and the actual memory devices is normally a bidirectional bus which is driven by tri-state buffers.

Table 2 on page 2 lists and describes the signals which make up the External Memory Interface. Apart from "MemDataIn," all of the signals are outputs from the Memory Controller. All of the 1-bit wide control signals are active low, as indicated by the "N" at the end of the signal names.

Table 2 • **Memory Controller External Memory Interface**

Signal	Width	Description
Flash Control Signals		
FlashCSN	1	Flash chip select. In some systems, the chip select pin of the Flash will be fixed at an active level, in which case this signal may be left unconnected.
FlashOEnN	1	Flash output enable
FlashWEnN	1	Flash write enable
SRAM Control Signals		
SramCSN	1	SRAM chip select. In some systems the chip select pin of the SRAM will be fixed at an active level in which case this signal may be left unconnected.
SramOEnN	1	SRAM output enable
SramWEnN	1	SRAM write enable
SramByte0N	1	SRAM byte 0 enable
SramByte1N	1	SRAM byte 1 enable
SramByte2N	1	SRAM byte 2 enable
SramByte3N	1	SRAM byte 3 enable
Shared Memory Signals		
MemReadN	1	Combined Flash/SRAM read enable. This signal is asserted (low) when either FlashOEnN or SramOEnN is low and is intended for use in a memory system which does not have separate connections to the Flash and SRAM output enable pins.
MemWriteN	1	Combined Flash/SRAM write enable. This signal is asserted (low) when either FlashWEnN or SramWEnN is low and is intended for use in a memory system which does not have separate connections to the Flash and SRAM write enable pins.
MemAddr	28	Flash/SRAM address bus
MemDataOEnN	1	Flash/SRAM data out enable. Control signal for data bus tri-states. Active low; that is, low when data is driven on MemDataOut.
MemDataOut	32	Flash/SRAM data out
MemDataIn	32	Flash/SRAM data in

CoreMemCtrl Configurable Options

There are a number of configurable options that apply to CoreMemCtrl. These are detailed in Table 3. If a configuration different from the default is required, the user should use the configuration dialog in CoreConsole to select appropriate values for the configurable options.

Table 3 • **Memory Controller Configurable Options**

Configurable Option	Default Setting	Description
SRAM mode	Asynchronous	Selects either asynchronous or synchronous SRAM. Possible settings are "Asynchronous" or "Synchronous."
Flash data bus width	32-bit	Selects the data bus width for the Flash memory interface. Possible settings are "32-bit" or "16-bit".
Number of wait states for Flash read	1	Selects the number of wait states inserted during a Flash read access. Possible range is 0 to 3.
Number of wait states for Flash write	1	Selects the number of wait states inserted during a Flash write read access. Possible range is 1 to 3.
Number of wait states for SRAM read	1	Only applicable when SRAM mode is set to "Asynchronous". Selects the number of wait states inserted during an SRAM read access. Possible range is 0 to 3.
Number of wait states for SRAM write	1	Only applicable when SRAM mode is set to "Asynchronous." Selects the number of wait states inserted during an SRAM write access. Possible range is 1 to 3.

Resource Requirements

The utilization for CoreMemCtrl in a ProASIC3E device is 100 tiles.

Ordering Information

CoreMemCtrl is included in the SysBASIC core bundle that is supplied with the Actel CoreConsole IP Deployment Platform tool. The obfuscated RTL version of SysBASIC (SysBASIC-OC) is available for free with CoreConsole. The source RTL version of SysBASIC (SysBASIC-RM) can be ordered through your local Actel sales representative. CoreMemCtrl cannot be ordered separately from the SysBASIC core bundle.

Datasheet Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," and "Production." The definitions of these categories are as follows:

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The product brief is a summarized version of an advanced or production datasheet containing general product information. This brief summarizes specific device and family information for unreleased products.

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This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

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www.actel.com

Actel Corporation

2061 Stierlin Court
Mountain View, CA
94043-4655 USA
Phone 650.318.4200
Fax 650.318.4600

Actel Europe Ltd.

Dunlop House, Riverside Way
Camberley, Surrey GU15 3YL
United Kingdom
Phone +44 (0) 1276 401 450
Fax +44 (0) 1276 401 490

Actel Japan
www.jp.actel.com

EXOS Ebisu Bldg. 4F
1-24-14 Ebisu Shibuya-ku
Tokyo 150 Japan
Phone +81.03.3445.7671
Fax +81.03.3445.7668

Actel Hong Kong
www.actel.com.cn

Suite 2114, Two Pacific Place
88 Queensway, Admiralty
Hong Kong
Phone +852 2185 6460
Fax +852 2185 6488

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