CoreRemap Datasheet

DirectCore

Product Summary

Intended Use

- Intended for Use in a CoreMP7-Based Subsystem with Flash and RAM Memory

Key Features

- Supplied in SysBASIC Core Bundle
- Tiny Area
- Flexible – Software Programmable or Set Externally
- Optimized for Use with CoreMP7

Benefits

- Ideal for Debugging a Flash-Based Subsystem
- Auto Stitch in CoreConsole
- Compatible with AMBA and CoreMP7

ARM Supported Families

- ProASIC®3 (M7A3P)
- ProASIC3E (M7A3PE)
- Fusion (M7AFS)

Synthesis and Simulation Support

- Supported in the Actel Libero® Integrated Design Environment (IDE)

Verification and Compliance

- Compliant with AMBA

Contents

General Description

This APB slave is a small control block that has a single-bit register which is intended for use in control aliasing of memory resources at the bottom of the processor address space. Typically the nonvolatile Flash is located at slot 0 at the bottom of the memory map by default, but the SRAM may be made to appear at the base of the address space by setting Remap high (in which case slot 0 is addressable as slot 1).

The RemapDefault input determines the value of the Remap output following a reset.

The Remap output of the CoreRemap module is normally connected to the Remap input of the CoreAHB or CoreAHBLite. The RemapDefault input may be connected to the top-level of the subsystem to provide a means of controlling the reset value of Remap.

Connecting CoreRemap in CoreConsole

Table 1 lists the ports present on the CoreRemap and describes how to connect these in CoreConsole.

Table 1 • **System Control Block Connections**

Connection	CoreConsole Label	Description
Required Connections		
APB Slave Interface	APBslave	Connect this interface to any available slave slot on the APB Bus.
PCLK	PCLK	APB clock signal. Normally connected to the HCLK output of CoreMP7Bridge.
PRESETn	PRESETn	Active low APB reset input. Normally connected to the HRESETn output of CoreMP7Bridge.
Remap	Remap	This output is driven by an internal control register bit and is intended to be used for controlling memory aliasing. This signal should be connected to the Remap input of the AHB Controller (CoreAHB or CoreAHBLite).
Optional Connections		
Default Setting for Remap	RemapDefault	This input determines the value of the Remap output following a reset. This signal may be connected to the subsystem top-level to allow external control of memory aliasing after reset. If no connection is made to this port, it will be tied low.

Programmer's Model

CoreRemap contains a single register at offset 0x00 (and aliased throughout the slot) which is described in Table 2.

Table 2 • **System Control Register**

Bits	Name	Type	Function
31:1	–	–	Reserved
0	Remap	Read/Write	Control bit which drives Remap output

Resource Requirements

The utilization for CoreRemap in a ProASIC3E device is 15 tiles.

Ordering Information

CoreRemap is included in the SysBASIC core bundle that is supplied with the Actel CoreConsole IP Deployment Platform tool. The obfuscated RTL version of SysBASIC (SysBASIC-OC) is available for free with CoreConsole. The source RTL version of SysBASIC (SysBASIC-RM) can be ordered through your local Actel sales representative. CoreRemap cannot be ordered separately from the SysBASIC core bundle.

Datasheet Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," and "Production." The definitions of these categories are as follows:

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The product brief is a summarized version of an advanced or production datasheet containing general product information. This brief summarizes specific device and family information for unreleased products.

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This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

Unmarked (production)

This datasheet version contains information that is considered to be final.

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