CoreUARTapb Datasheet

DirectCore

Product Summary

Intended Use

- AMBA APB Interface to Industry Standard UART Controllers for Use in a CoreConsole Generated CoreMP7 Subsystem.
- Embedded Systems for Sharing Data Between Devices with Limited Pin Counts Using Standard UART Protocols

Key Features

- Supplied in SysBASIC Core Bundle
- AMBA APB Interface
- Size Efficient Asynchronous/Synchronous UART with FIFO Interface on Both Receive and Transmit
- Asynchronous (UART) Mode – Fully Programmable to Any Baud Rate up to 1/16th of the System Clock Frequency with Glitch Rejection
- Synchronous Mode – 12 Clock Cycles Required Per Byte Transfer
- Supports All Standard Baud Rates up to 921,600 Baud
- 7 or 8 Bits of Data
- Parity (Odd, Even, and None)
- Baud Rate Control for Asynchronous Mode
- FIFO Off Loads the Host Processor
- FIFO Depth up to 256 Bytes on Both Receive and Transmit
- Transmit has Normal and FIFO Modes
- Receive has Normal and FIFO Modes
- Both Receive and Transmit are Double-Buffered to Maximize Throughput in Normal Mode
- Supports RS232 Interface

Benefits

- Add Standard Serial Communications to CoreMP7 Designs
- Auto Stitch CoreUARTapb in CoreConsole for Rapid Development
- Compatible with AMBA and CoreMP7

ARM Supported Families

- ProASIC®3 (M7A3P)
- ProASIC3E (M7A3PE)
- Fusion (M7AFS)

Synthesis and Simulation Support

- Supported in the Actel Libero®Integrated Design Environment (IDE)

Verification and Compliance

- Compliant with AMBA

Contents

General Description

The CoreUARTapb is a serial communication controller with a flexible serial data interface that is intended primarily for embedded systems. The controller can operate in either an asynchronous (UART) or synchronous mode.

In the synchronous mode, the same UART protocols are used, but the baud rate is equivalent to the input clock frequency. When employing the CoreUARTapb in the synchronous mode, the interacting devices must operate off of the same system clock.

For the asynchronous mode, the clocks can be the same or different, including different frequencies.

The main reason for using the synchronous mode is to improve data bandwidth. In the asynchronous mode, the CoreUARTapb can be used to directly interface to industry standard UARTs. The CoreUARTapb is

intentionally a subset of the full UART capabilities in order to make the function cost effective.

CoreUARTapb

The CoreUARTapb component available in CoreConsole is an APB-wrapped version of the Actel DirectCore CoreUART. The serial communication interface is identical to that described in the *CoreUART datasheet* available on the Actel website.

The CoreConsole CoreUARTapb adds an APB interface that allows access to transmit and receive data registers, two control registers, and a status register. The CoreUART registers are described in "CoreUARTapb Programmer's Model" on page 3.

Figure 1 shows a block diagram of the CoreUARTapb.

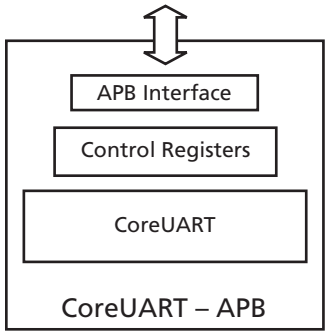

Figure 1 • **CoreUARTapb Block Diagram**

Connecting CoreUARTapb in CoreConsole

Table 1 lists the ports present on the CoreUARTapb component and describes how to connect these in CoreConsole.

Table 1 • **CoreUARTapb Connections**

Connection	CoreConsole Label	Description
Required Connections		
APB slave interface	APBslave	Connect this interface to any available slave slot on the APB Bus.
PCLK	PCLK	APB clock signal. Normally connected to the HCLK output of the MP7Bridge.
PRESETn	PRESETn	Active low APB reset input. Normally connected to the HRESETn output of the MP7Bridge.
rx	rx	Serial receive data input. Normally connected to subsystem top-level for subsequent connection to a pin of the FPGA.
tx	tx	Serial transmit data output. Normally connected to subsystem top-level for subsequent connection to a pin of the FPGA.
Optional Connections		
txrdy	txrdy	Status output. When low, the transmit data buffer/FIFO is not available for additional transmit data. The level of this signal is available in the status register (see the "Status Register" section on page 4).
receive_full	receive_full	Status output. When high, data is available in the receive data buffer/FIFO. The level of this signal is available in the status register (see the "Status Register" section on page 4).

CoreUARTapb Configurable Options

There are a number of configurable options which apply to the CoreUARTapb as shown in Table 2. If a configuration other than the default is required, the user should use the configuration dialog in CoreConsole to select appropriate values for the configurable options.

Table 2 • **CoreUARTapb Configurable Options**

Configurable Options	Default Setting	Description
Transmit FIFO	Disabled	Enables or disables transmit FIFO
Receive FIFO	Disabled	Enables or disables receive FIFO
Mode of Operation	Asynchronous	Selects mode of operation of CoreUART. Possible settings are Asynchronous and Synchronous.
Device Family	ProASIC3	Selects target family. Possible settings are ProASIC3 and ProASIC3E.

CoreUARTapb Programmer's Model

Table 3 lists the registers for CoreUARTapb.

Table 3 • **CoreUARTapb Registers**

Address	Type	Width	Reset value	Name	Description
base + 0x000	Write	32	0	TxData	Transmit Data Register
base + 0x004	Read	32	0	RxData	Receive Data Register
base + 0x008	Read/Write	32	0	Ctrl1	Control Register 1
base + 0x00C	Read/Write	32	0	Ctrl2	Control Register 2
base + 0x010	Read	32	0	Status	Status Register

Transmit Data Register

The 7- or 8- bit transmit data

Receive Data Register

The 7- or 8- bit receive data

Control Register 1

Control Register 1 contains a single field, baud value, which is used to set the baud rate for CoreUART when in asynchronous mode. The baud value should be set according to EQ 1.

Baud value (decimal) = (clock / ((baud + 1) x 16))

EQ 1

where clock is the APB system clock frequency in hertz.

The result of this calculation must be rounded to the nearest integer and converted to hexadecimal to obtain the value which should be written to Control Register 1, shown in Table 4.

For example, when the APB clock frequency is 10 MHz, and a baud rate of 9600 is desired, 0x41 should be written to Control Register 1.

Table 4 • **Control Register 1**

Bits	Name	Type	Function
7:0	Baud value	Read/Write	8-bit value setting the baud rate

Control Register 2

Table 5 shows Control Register 2, which is used to assign values to the configuration inputs available on the CoreUART.

Table 5 • **Control Register 2**

Bits	Name	Type	Function
0	bit8	Read/Write	Data width setting: Bit8 = 0 : 7 bit data Bit8 = 1 : 8 bit data
1	parity_en	Read/Write	Parity is enabled when this bit is set to 1
2	odd_n_even	Read/Write	Parity is set as follows: odd_n_even = 0 : even odd_n_even = 1 : odd
7:3			Unused

Status Register

Table 6 shows the Status Register, which provides information on the status of the CoreUART.

Table 6 • **Status Register**

Bits	Name	Type	Function
0	txrdy	Read Only	When low, the transmit data buffer/FIFO is not available for additional transmit data.
1	receive_full	Read Only	When high, data is available in the receive data buffer/FIFO. This bit is cleared by reading the Receive Data Register.
2	parity_err	Read Only	When high, a parity error occurs during a receive transaction. This bit is cleared by reading the Receive Data Register.
3	overflow	Read Only	When high, a receive overflow occurs. This bit is cleared by reading the Receive Data Register.
7:4			Unused

Resource Requirements

The utilization for CoreUARTapb in a ProAISCI3E device is 300 tiles.

Ordering Information

CoreUARTapb is included in the SysBASIC core bundle that is supplied with the Actel CoreConsole IP Deployment Platform tool. The obfuscated RTL version of SysBASIC (SysBASIC-OC) is available for free with CoreConsole. The source RTL version of SysBASIC (SysBASIC-RM) can be ordered through your local Actel sales representative. CoreUARTapb cannot be ordered separately from the SysBASIC core bundle.

Datasheet Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," and "Production." The definitions of these categories are as follows:

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The product brief is a summarized version of an advanced or production datasheet containing general product information. This brief summarizes specific device and family information for unreleased products.

Advanced

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

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This datasheet version contains information that is considered to be final.

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