Device Architecture

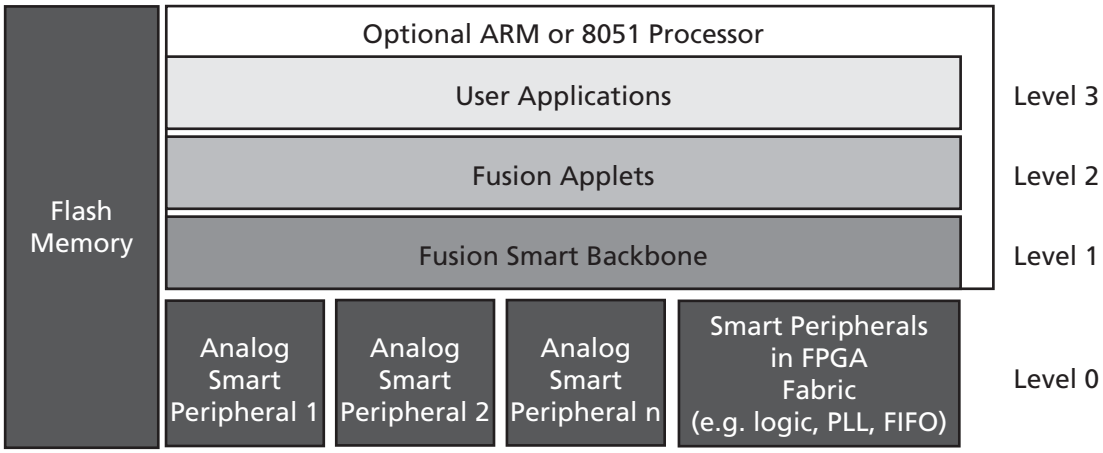
Fusion Stack Architecture

To manage the unprecedented level of integration in Fusion devices, Actel developed the Fusion technology stack (Figure 2-1). This layered model offers a flexible design environment, enabling design at very high and very low levels of abstraction. Fusion peripherals include hard analog IP and hard and soft digital IP. Peripherals will communicate across the FPGA fabric via a layer of soft gates—the Fusion backbone. Much more than a common bus interface, this Fusion backbone integrates a micro-sequencer within the FPGA fabric and will configure the individual peripherals and support low-level processing of peripheral data. Fusion applets are application building blocks that can control and respond to peripherals and other system signals. Applets can be rapidly combined to create large applications. The technology is scalable across devices, families, design types, and user expertise, and supports a well-defined interface for external IP and tool integration.

At the lowest level, Level 0, are Fusion peripherals. These are configurable functional blocks that can be hardwired structures such as a PLL or analog input channel, or soft (FPGA-gate) blocks such as a UART or two-wire serial interface. The Fusion peripherals are configurable and support a standard interface to facilitate communication and implementation.

Connecting and controlling access to the peripherals is the Fusion backbone, Level 1. The backbone is a soft-gate structure and is scalable to any number of peripherals. The backbone is a bus and much more; it manages peripheral configuration to ensure proper operation. Leveraging the common peripheral interface and a low-level state machine, the backbone efficiently offloads peripheral management from the system design. The backbone can set and clear flags based upon peripheral behavior and define performance criteria. The flexibility of the stack enables a designer to configure the silicon, directly bypassing the backbone if that level of control is desired.

One step up from the backbone is the Fusion applet, Level 2. The applet is an application building block that implements a specific function in FPGA gates. It can react to stimuli and board-level events coming through the backbone, or from other sources, and responds to these stimuli by accessing and manipulating peripherals via the backbone or initiating some other action. An applet controls or responds to the peripheral(s). Applets can be easily imported or exported from the design environment. The applet structure is open and well-defined, enabling users to import applets from Actel, system developers, third parties, and user groups.



Note: *Levels 1, 2, and 3 are implemented in FPGA logic gates.*

Figure 2-1 • **Fusion Architecture Stack**

The system application, Level 3, is the larger user application that utilizes one or more applets. Designing at the highest level of abstraction supported by the Actel Fusion technology stack, the application can be easily created in FPGA gates by importing and configuring multiple applets.

In fact, in some cases an entire FPGA system design can be created without any HDL coding.

An optional MCU enables a combination of software and HDL-based design methodologies. The MCU can be on-chip or off-chip as system requirements dictate. System portioning is very flexible, allowing the MCU to reside above the applets or to absorb applets, or applets and backbone, if desired.

The Actel Fusion technology stack enables a very flexible design environment. Users can engage in design across a continuum of abstraction from very low to very high.

Core Architecture

VersaTile

Based upon successful Actel ProASIC3/E logic architecture, Fusion devices provide granularity comparable to gate arrays. The Fusion device core consists of a sea-of-VersaTiles architecture.

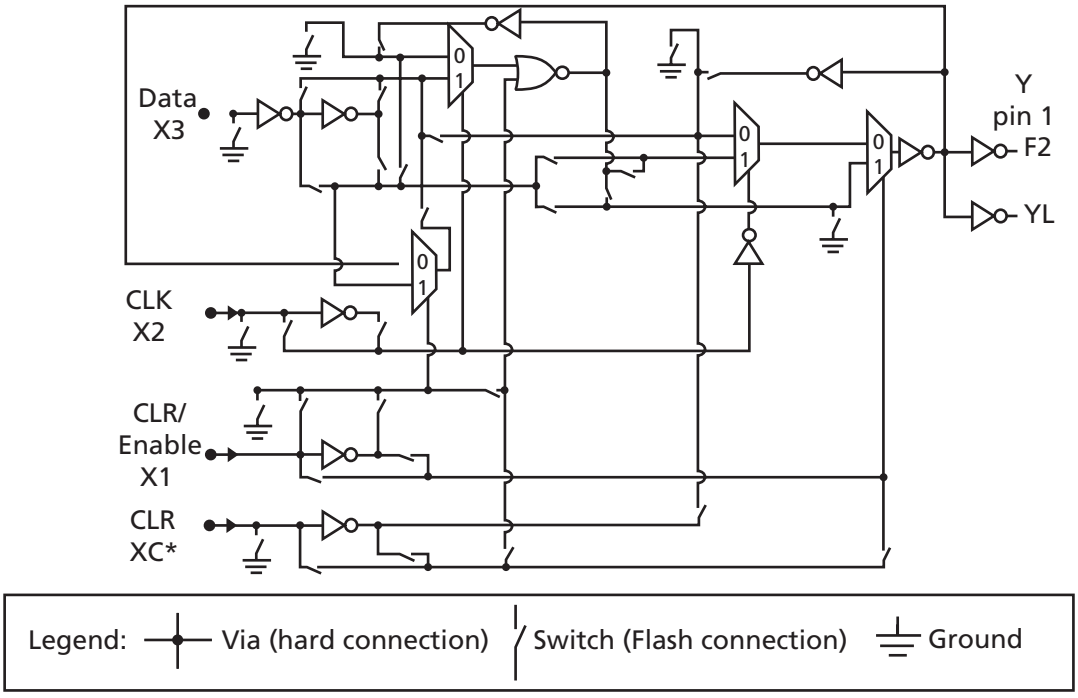
As illustrated in Figure 2-2, there are four inputs in a logic VersaTile cell, and each VersaTile can be configured using the appropriate Flash switch connections:

- Any three-input logic function
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set (on a fourth input)

VersaTiles can flexibly map the logic and sequential gates of a design. The inputs of the VersaTile can be inverted (allowing bubble pushing), and the output of the tile can connect to high-speed, very-long-line routing resources. VersaTiles and larger functions are connected with any of the four levels of routing hierarchy.

When the VersaTile is used as an enable D-flip-flop, the SET/CLR signal is supported by a fourth input, which can only be routed to the core cell over the VersaNet (global) network.

The output of the VersaTile is F2 when the connection is to the ultra-fast local lines, or YL when the connection is to the efficient long-line or very-long-line resources (Figure 2-2).



Note: **This input can only be connected to the global clock distribution network.*

Figure 2-2 • **Fusion Core VersaTile**

VersaTile Characteristics

Sample VersaTile Specifications—Combinatorial Module

The Fusion library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library (Figure 2-3). For more details, refer to the *Fusion and ProASIC3/E Macro Library Guide*.

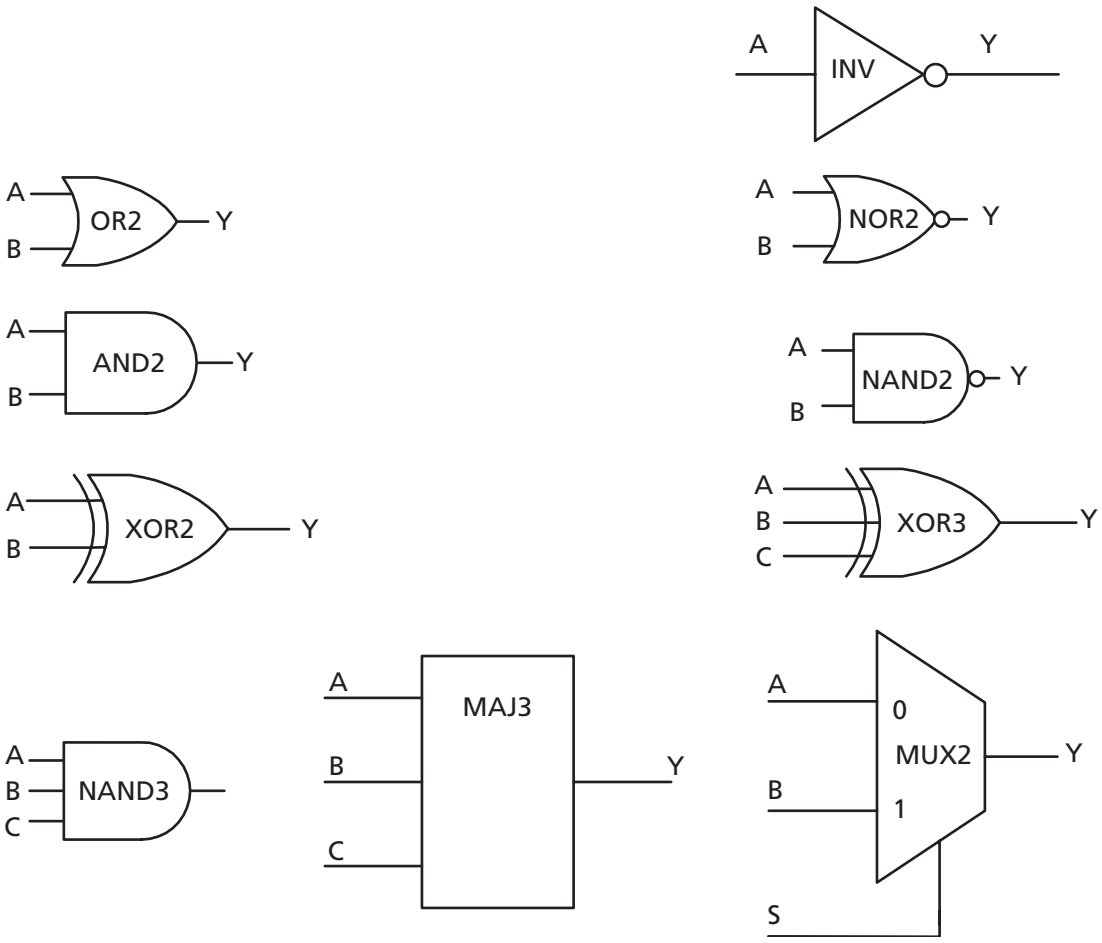
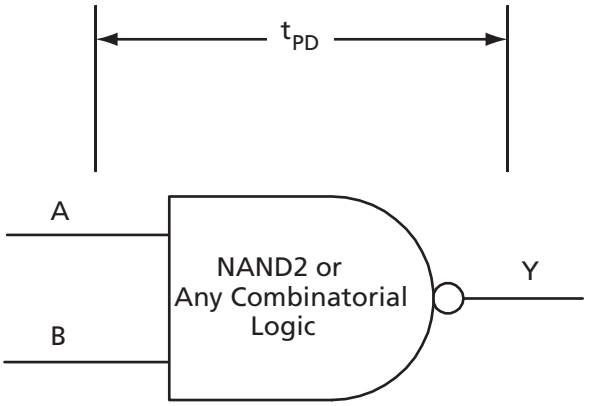


Figure 2-3 • **Sample of Combinatorial Cells**



$t_{PD} = MAX(t_{PD(RR)}, t_{PD(RF)}, t_{PD(FF)}, t_{PD9(FR)})$
where edges are applicable for the particular combinatorial cell

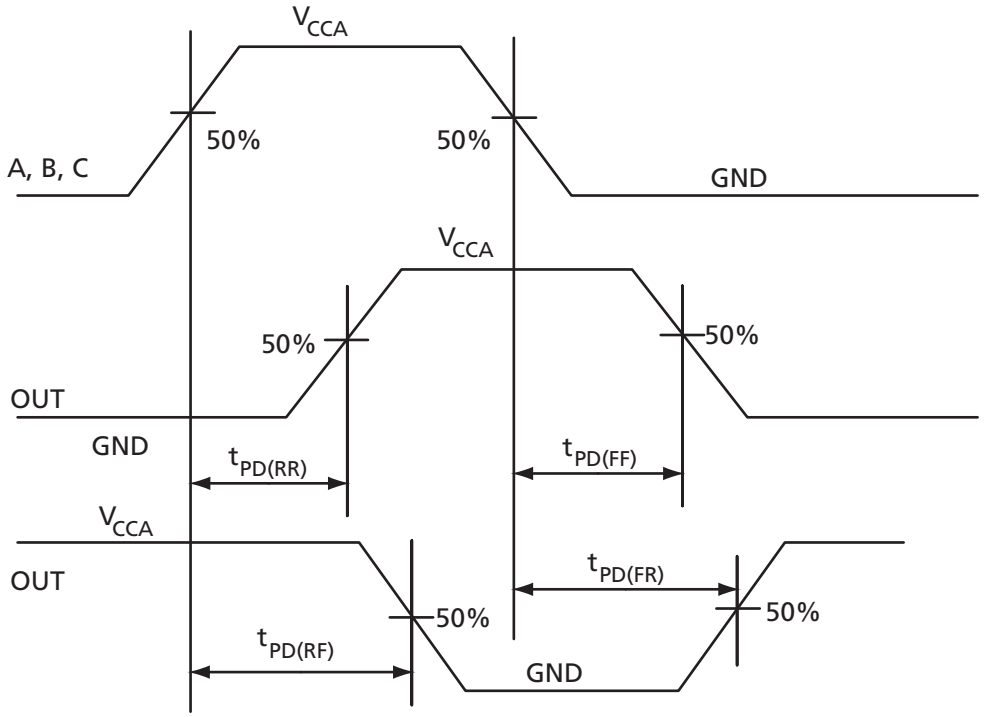


Figure 2-4 • **Combinatorial Timing Model and Waveforms**

Timing Characteristics

Table 2-1 • **Combinatorial Cell Propagation Delays**
Commercial Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V

Combinatorial Cell	Equation	Parameter	–2	–1	Std.	Units
INV	Y = !A	t_{PD}	0.40	0.46	0.54	ns
AND2	Y = A · B	t_{PD}	0.47	0.54	0.63	ns
NAND2	Y = !(A · B)	t_{PD}	0.47	0.54	0.63	ns
OR2	Y = A + B	t_{PD}	0.49	0.55	0.65	ns
NOR2	Y = !(A + B)	t_{PD}	0.49	0.55	0.65	ns
XOR2	Y = A ⊕ B	t_{PD}	0.74	0.84	0.99	ns
MAJ3	Y = MAJ (A, B, C)	t_{PD}	0.70	0.79	0.93	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	0.87	1.00	1.17	ns
MUX2	Y = A !S + B S	t_{PD}	0.51	0.58	0.68	ns
AND3	Y = A · B · C	t_{PD}	0.56	0.64	0.75	ns

Note: *For the derating values at specific junction-temperature and voltage-supply levels, refer to Table 3-6 on page 3-6.*

Sample VersaTile Specifications—Sequential Module

The Fusion library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library (Figure 2-5). For more details, refer to the *Fusion and ProASIC3/E Macro Library Guide*.

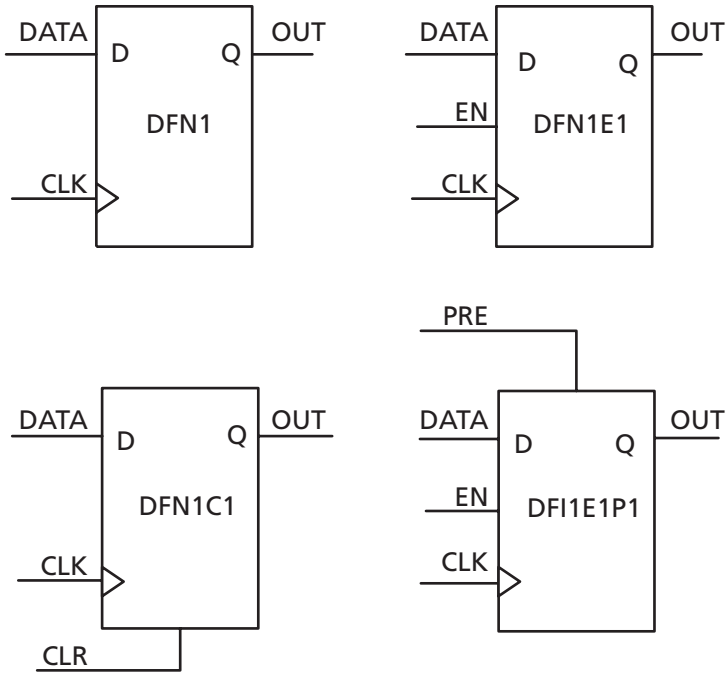


Figure 2-5 • **Sample of Sequential Cells**

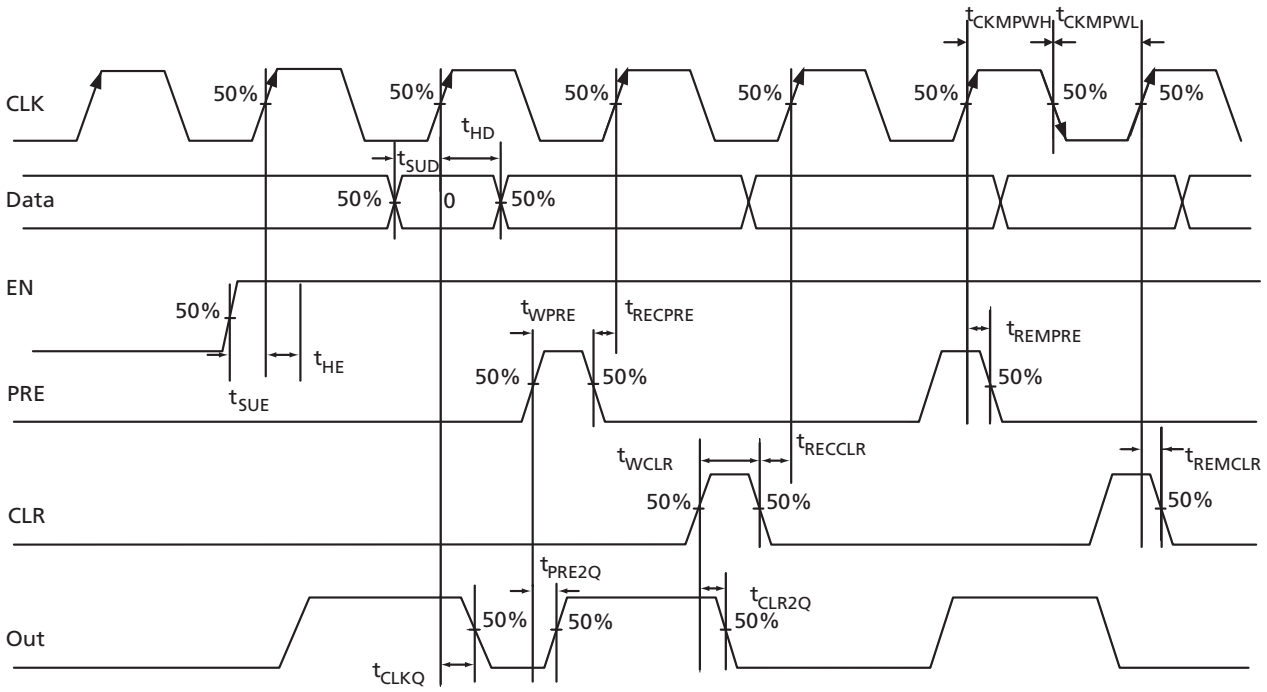


Figure 2-6 • **Sequential Timing Model and Waveforms**

Sequential Timing Characteristics

Table 2-2 • **Register Delays**
Commercial Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	0.55	0.63	0.74	ns
t_{SUD}	Data Setup time for the Core Register	0.43	0.49	0.57	ns
t_{HD}	Data Hold time for the Core Register	0.00	0.00	0.00	ns
t_{SUE}	Enable Setup time for the Core Register	0.45	0.52	0.61	ns
t_{HE}	Enable Hold time for the Core Register	0.00	0.00	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.40	0.45	0.53	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.40	0.45	0.53	ns
t_{REMCLR}	Asynchronous Clear Removal time for the Core Register	0.00	0.00	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery time for the Core Register	0.22	0.25	0.30	ns
t_{REMPRE}	Asynchronous Preset Removal time for the Core Register	0.00	0.00	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery time for the Core Register	0.22	0.25	0.30	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.25	0.28	0.33	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.25	0.28	0.33	ns
t_{CKMPWH}	Clock Minimum Pulse Width High for the Core Register	0.36	0.41	0.48	ns
t_{CKMPWL}	Clock Minimum Pulse Width Low for the Core Register	0.41	0.46	0.54	ns

Note: *For the derating values at specific junction-temperature and voltage-supply levels, refer to Table 3-6 on page 3-6.*

Array Coordinates

During many place-and-route operations in the Actel Designer software tool, it is possible to set constraints that require array coordinates. Table 2-3 is provided as a reference. The array coordinates are measured from the lower left (0, 0). They can be used in region constraints for specific logic groups/blocks, designated by a wildcard, and can contain core cells, memories, and I/Os.

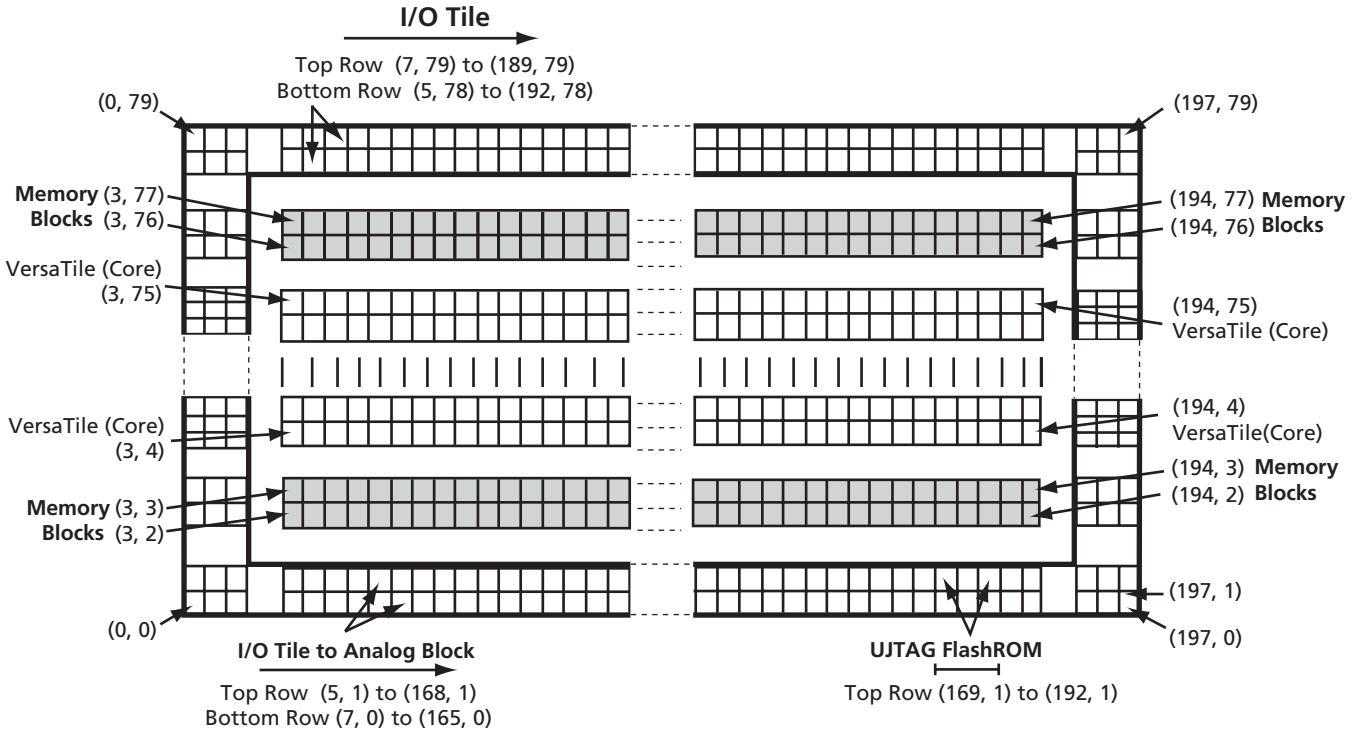
Table 2-3 provides array coordinates of core cells and memory blocks.

I/O and cell coordinates are used for placement constraints. Two coordinate systems are needed because there is not a one-to-one correspondence between I/O cells and edge core cells. In addition, the I/O coordinate system changes depending on the die/package combination. It is not listed in Table 2-3. The Designer ChipPlanner tool provides array coordinates of all I/O locations. I/O and cell coordinates are used for placement constraints. However, I/O placement is easier by package pin assignment.

Figure 2-7 illustrates the array coordinates of an AFS600 device. For more information on how to use array coordinates for region/placement constraints, see the *Designer User's Guide* or online help (available in the software) for Fusion software tools.

Table 2-3 • **Array Coordinates**

	VersaTiles				Memory Rows		All	
	Min.		Max.		Bottom	Top	Min.	Max.
Device	**x**	**y**	**x**	**y**	**(x, y)**	**(x, y)**	**(x, y)**	**(x, y)**
AFS090	3	2	66	25	None	(3, 26)	(0, 0)	(69, 29)
AFS250	3	2	130	49	None	(3, 50)	(0, 0)	(133, 53)
AFS600	3	4	194	75	(3, 2)	(3, 76)	(0, 0)	(197, 79)
AFS1500	3	4	258	99	(3, 2)	(3, 100)	(0, 0)	(261, 103)



Note: *The vertical I/O tile coordinates are not shown. West side coordinates are {(0, 2) to (2, 2)} to {(0, 77) to (2, 77)}; east side coordinates are {(195, 2) to (197, 2)} to {(195, 77) to (197, 77)}.*

Figure 2-7 • **Array Coordinates for AFS600**

Routing Architecture

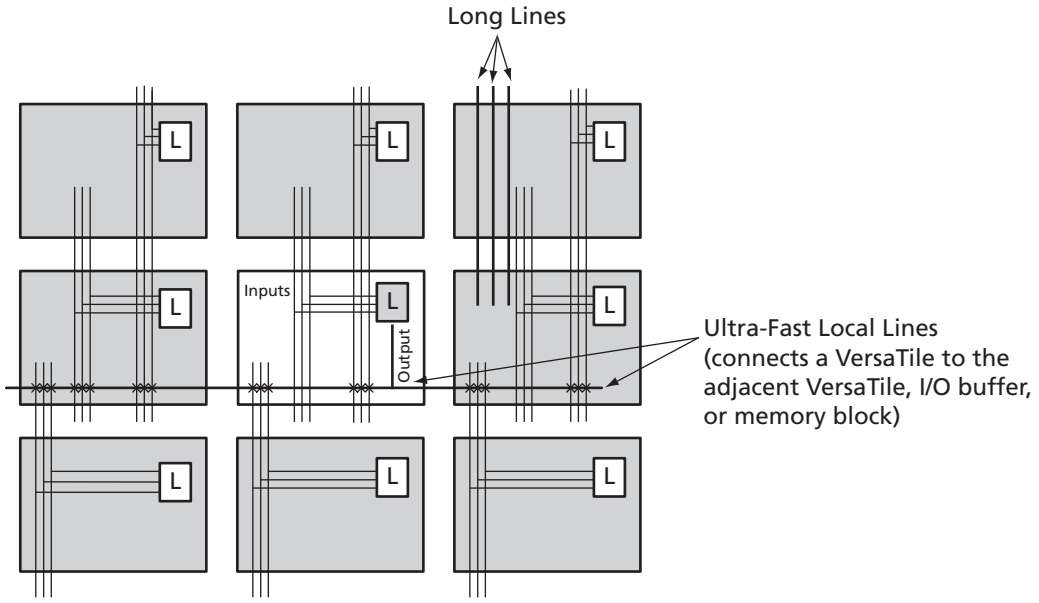
The routing structure of Fusion devices is designed to provide high performance through a flexible four-level hierarchy of routing resources: ultra-fast local resources; efficient long-line resources; high-speed, very-long-line resources; and the high-performance VersaNet networks.

The ultra-fast local resources are dedicated lines that allow the output of each VersaTile to connect directly to every input of the eight surrounding VersaTiles (Figure 2-8). The exception to this is that the SET/CLR input of a VersaTile configured as a D-flip-flop is driven only by the VersaNet global network.

The efficient, long-line resources provide routing for longer distances and higher fanout connections. These resources vary in length (spanning one, two, or four VersaTiles), run both vertically and horizontally, and cover the entire Fusion device (Figure 2-9 on page 2-9). Each VersaTile can drive signals onto the efficient long-line resources, which can access every input of every VersaTile. Active buffers are inserted automatically by routing software to limit the loading effects.

The high-speed, very-long-line resources, which span the entire device with minimal delay, are used to route very long or high-fanout nets: length +/–12 VersaTiles in the vertical direction and length +/–16 in the horizontal direction from a given core VersaTile (Figure 2-10 on page 2-10). Very long lines in Fusion devices, like those in ProASIC3, have been enhanced. This provides a significant performance boost for long-reach signals.

The high-performance VersaNet global networks are low-skew, high-fanout nets that are accessible from external pins or from internal logic (Figure 2-11 on page 2-11). These nets are typically used to distribute clocks, reset signals, and other high-fanout nets requiring minimum skew. The VersaNet networks are implemented as clock trees, and signals can be introduced at any junction. These can be employed hierarchically with signals accessing every input on all VersaTiles.



Note: *Input to the core cell for the D-flip-flop set and reset is only available via the VersaNet global network connection.*

Figure 2-8 • **Ultra-Fast Local Lines Connected to the Eight Nearest Neighbors**

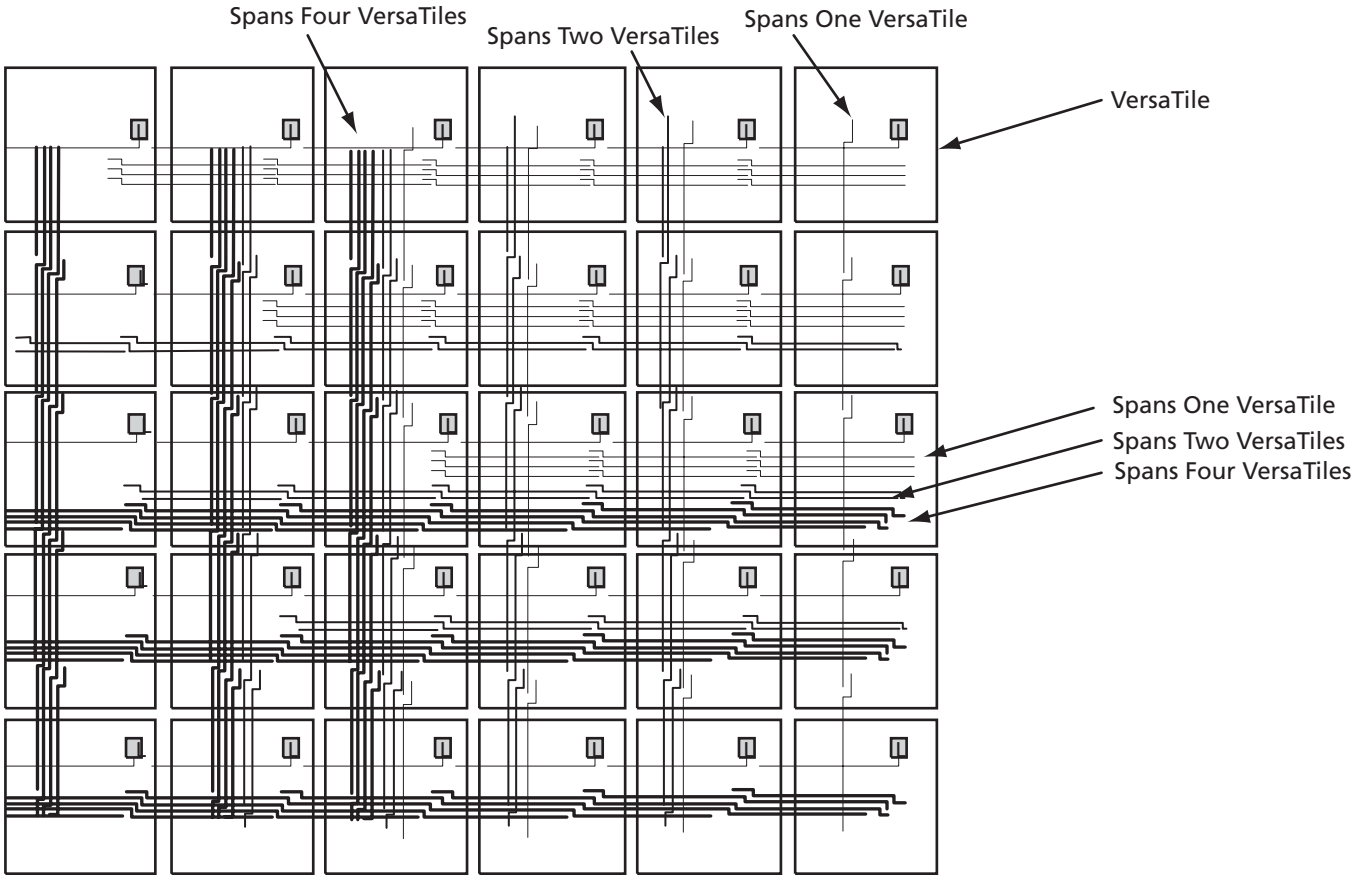


Figure 2-9 • **Efficient Long-Line Resources**

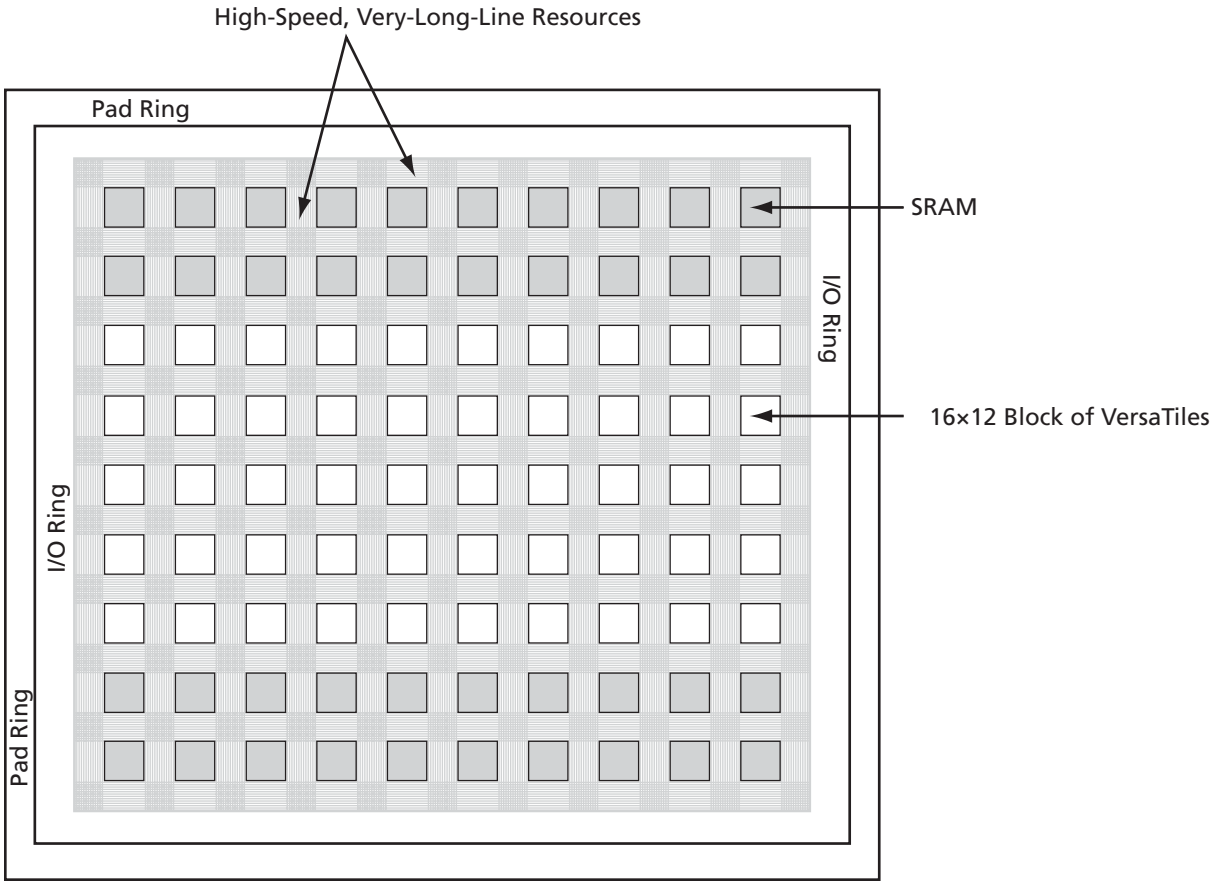


Figure 2-10 • **Very-Long-Line Resources**

Global Resources (VersaNets)

Fusion devices offer powerful and flexible control of circuit timing through the use of analog circuitry. Each chip has six clock conditioning circuits (CCCs). The west CCC also contains a phase-locked loop (PLL) core. In the two larger devices (AFS600 and AFS1500), both the west and the east CCC contain a PLL. The PLLs include delay lines, a phase shifter (0°, 90°, 180°, 270°), and clock multipliers/dividers. Each CCC has all the circuitry needed for the selection and interconnection of inputs to the VersaNet global network. The east and west CCCs each have access to three VersaNet global lines on each side of the chip (six lines total). The CCCs at the four corners each have access to three quadrant global lines on each quadrant of the chip.

Advantages of the VersaNet Approach

One of the architectural benefits of Fusion is the set of powerful and low-delay VersaNet global networks. Fusion offers six chip (main) global networks that are distributed from the center of the FPGA array (Figure 2-11). In addition, Fusion devices have three regional globals (quadrant globals) in each of the four chip quadrants. Each core VersaTile has access to nine global network resources: three quadrant and six chip (main) global networks. There are a total of 18 global networks on the device. Each of these networks contains spines and ribs that reach all VersaTiles in all quadrants (Figure 2-12 on page 2-12). This flexible VersaNet global network architecture allows users to map up to 180 different internal/external clocks in a Fusion device. Details on the VersaNet networks are given in Table 2-4 on page 2-12. The flexibility of the Fusion VersaNet global network allows the designer to address several design requirements. User applications that are clock-resource-intensive can easily route external or gated internal clocks using VersaNet global routing networks. Designers can also drastically reduce delay penalties and minimize resource usage by mapping critical, high-fanout nets to the VersaNet global network.

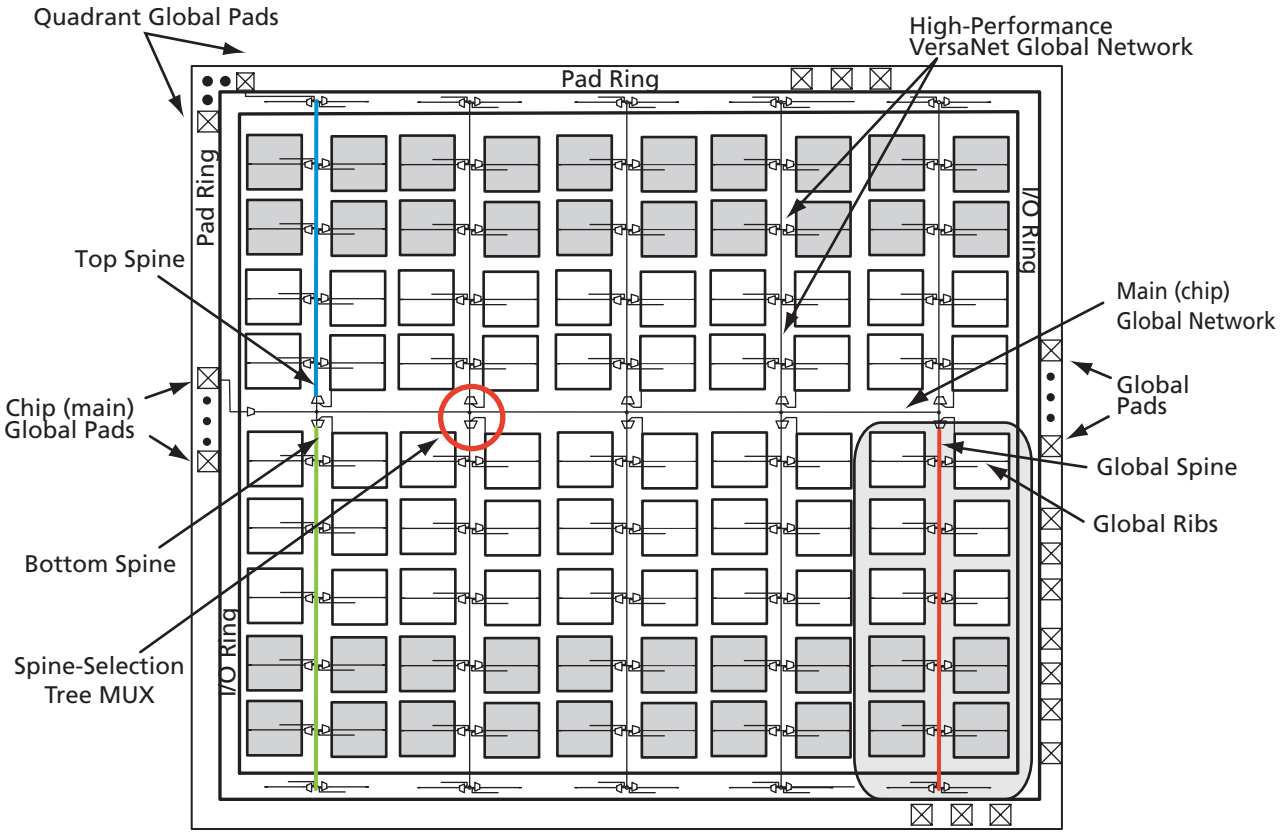


Figure 2-11 • **Overview of Fusion VersaNet Global Network**

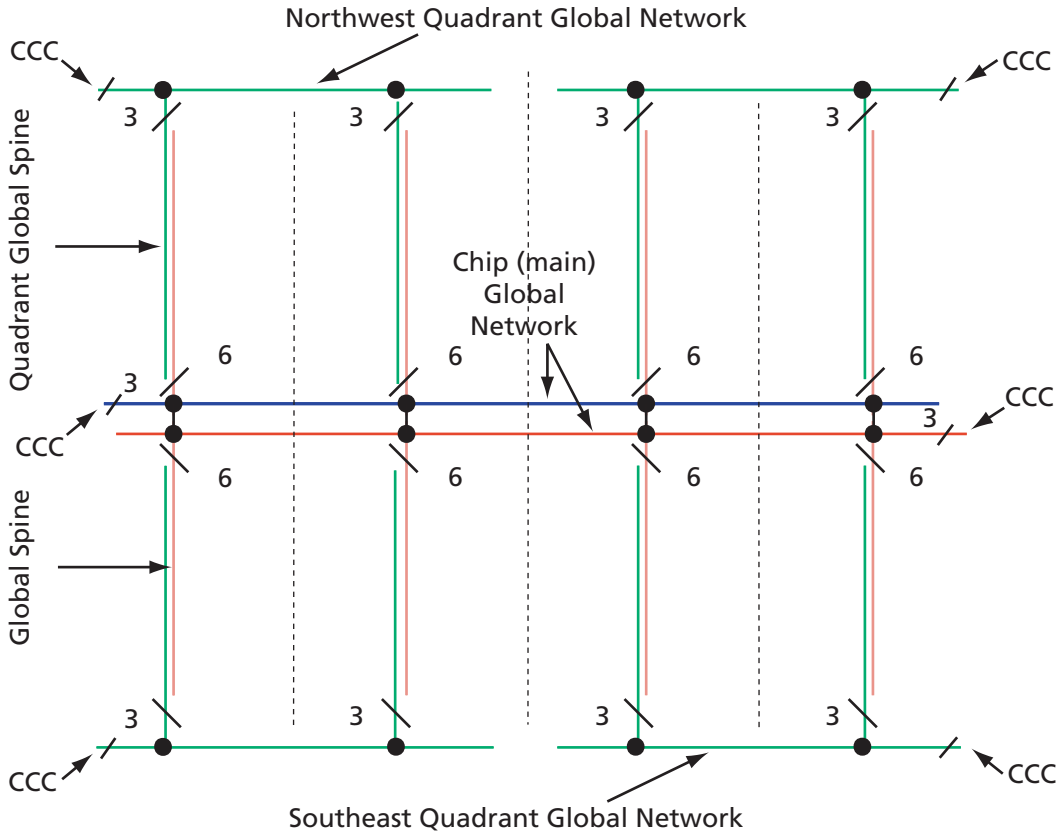


Figure 2-12 • **Global Network Architecture**

Table 2-4 • **Globals/Spines/Rows by Device**

	AFS090	AFS250	AFS600	AFS1500
Global VersaNets (Trees)*	9	9	9	9
VersaNet Spines/Tree	4	8	12	20
Total Spines	36	72	108	180
VersaTiles in Each Top or Bottom Spine	384	768	1,152	1,920
Total VersaTiles	2,304	6,144	13,824	38,400

Note: **There are six chip (main) globals and three globals per quadrant.*

VersaNet Global Networks and Spine Access

The Fusion architecture contains a total of 18 segmented global networks that can access the VersaTiles, SRAM memory, and I/O tiles on the Fusion device. There are 6 chip (main) global networks that access the entire device and 12 quadrant networks (3 in each quadrant). Each device has a total of 18 globals. These VersaNet global networks offer fast, low-skew routing resources for high-fanout nets, including clock signals. In addition, these highly segmented global networks offer users the flexibility to create low-skew local networks using spines for up to 180 internal/external clocks (in an AFS1500 device) or other high-fanout nets in Fusion devices. Optimal usage of these low-skew networks can result in significant improvement in design performance on Fusion devices.

The nine spines available in a vertical column reside in global networks with two separate regions of scope: the quadrant global network, which has three spines, and the chip (main) global network, which has six spines. Note that there are three quadrant spines in each quadrant of the device. There are four quadrant global network regions per device (Figure 2-12 on page 2-12).

The spines are the vertical branches of the global network tree, shown in Figure 2-11 on page 2-11. Each spine in a vertical column of a chip (main) global network is further divided into two equal-length spine segments: one in the top and one in the bottom half of the die.

Each spine and its associated ribs cover a certain area of the Fusion device (the "scope" of the spine; see Figure 2-11 on page 2-11). Each spine is accessed by the dedicated global network MUX tree architecture, which defines how a particular spine is driven—either by the signal on the global network from a CCC, for example, or another net defined by the user (Figure 2-13). Quadrant spines can be driven from user I/Os on the north and south sides of the die, via analog I/Os configured as direct digital inputs. The ability to drive spines in the quadrant global networks can have a significant effect on system performance for high-fanout inputs to a design.

Details of the chip (main) global network spine-selection MUX are presented in Figure 2-13. The spine drivers for each spine are located in the middle of the die.

Quadrant spines are driven from a north or south rib. Access to the top and bottom ribs is from the corner CCC or from the I/Os on the north and south sides of the device.

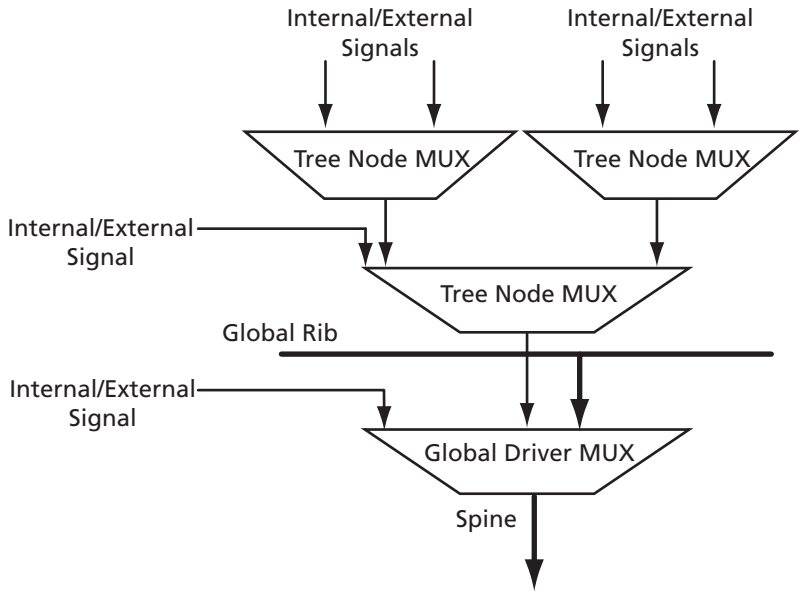


Figure 2-13 • **Spine-Selection MUX of Global Tree**

Clock Aggregation

Clock aggregation allows for multi-spine clock domains. A MUX tree provides the necessary flexibility to allow long-lines or I/Os to access domains of one, two, or four global spines. Signal access to the clock aggregation system is achieved through long-line resources in the central rib, and also through local resources in the north and south ribs, allowing I/Os to feed directly into the clock system. As Figure 2-14 indicates, this access system is contiguous.

There is no break in the middle of the chip for the north and south I/O VersaNet access. This is different from the quadrant clocks, located in these ribs, which only reach the middle of the rib.

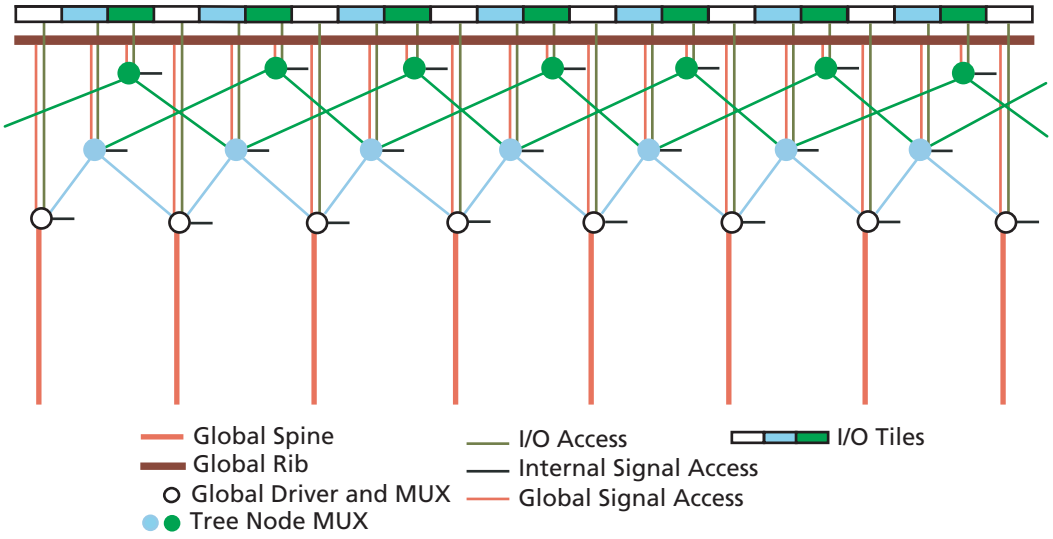


Figure 2-14 • **Clock Aggregation Tree Architecture**

Global Resource Characteristics

AFS600 VersaNet Topology

Clock delays are device-specific. Figure 2-15 is an example of a global tree used for clock routing. The global tree presented in Figure 2-15 is driven by a CCC located on the west side of the AFS600 device. It is used to drive all D-flip-flops in the device.

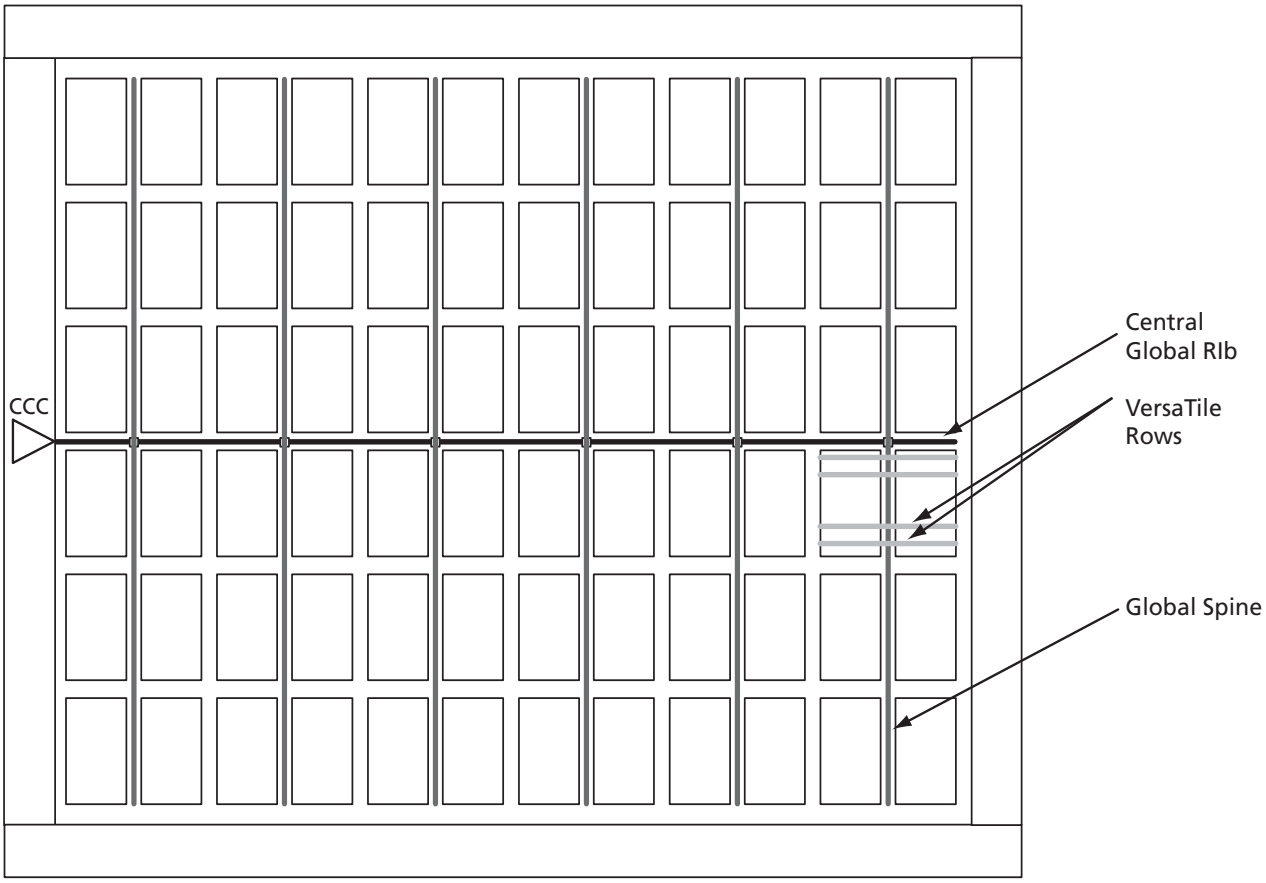


Figure 2-15 • **Example of Global Tree Use in an AFS600 Device for Clock Routing**

VersaNet Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are dependent upon I/O standard, and the clock may be driven and conditioned internally by the CCC module. Table 2-5, Table 2-6, and Table 2-7 present minimum and maximum global clock delays within the device. Minimum and maximum delays are measured with minimum and maximum loading, respectively.

Timing Characteristics

Table 2-5 • **AFS600 Global Resource Timing**
Commercial Case Conditions: T_J = 70°C, V_{CC} = 1.425 V

Parameter	Description	–2		–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.28	1.51	1.46	1.72	1.71	2.02	ns
t_{RCKH}	Input High Delay for Global Clock	1.28	1.55	1.45	1.77	1.71	2.08	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock							ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock							ns
t_{RCKSW}	Maximum Skew for Global Clock		0.27		0.31		0.37	ns
F_{RMAX}	Maximum Frequency for Global Clock							MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For the derating values at specific junction-temperature and voltage-supply levels, refer to Table 3-6 on page 3-6.*

Table 2-6 • **AFS250 Global Resource Timing**
Commercial Case Conditions: T_J = 70°C, V_{CC} = 1.425 V

Parameter	Description	–2		–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.19	1.42	1.36	1.62	1.59	1.91	ns
t_{RCKH}	Input High Delay for Global Clock	1.19	1.46	1.35	1.66	1.59	1.96	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock							ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock							ns
t_{RCKSW}	Maximum Skew for Global Clock		0.27		0.31		0.37	ns
F_{RMAX}	Maximum Frequency for Global Clock							MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For the derating values at specific junction-temperature and voltage-supply levels, refer to Table 3-6 on page 3-6.*

Table 2-7 • **AFS090 Global Resource Timing**
Commercial Case Conditions: T_J = 70°C, V_{CC} = 1.425 V

Parameter	Description	–2		–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.18	1.41	1.34	1.60	1.58	1.89	ns
t_{RCKH}	Input High Delay for Global Clock	1.17	1.44	1.33	1.64	1.57	1.93	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock							ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock							ns
t_{RCKSW}	Maximum Skew for Global Clock		0.27		0.31		0.37	ns
F_{RMAX}	Maximum Frequency for Global Clock							MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For the derating values at specific junction-temperature and voltage-supply levels, refer to Table 3-6 on page 3-6.*

Clocking Resources

The Fusion family has a robust collection of clocking peripherals, as shown in the block diagram in Figure 2-16. These on-chip resources enable the creation, manipulation, and distribution of many clock signals. The Fusion integrated RC oscillator produces a 100 MHz clock source with no external components. For systems requiring more precise clock signals, the Actel Fusion family supports an on-chip crystal oscillator circuit. The integrated PLLs in each Fusion device can use the RC oscillator, crystal oscillator, or another on-chip clock signal as a source. These PLLs offer a variety of capabilities to modify the clock source (multiply, divide, synchronize, advance, or delay). Utilizing the CCC found in the popular Actel ProASIC3 family, Fusion incorporates six CCC blocks. The CCCs allow access to Fusion global and local clock distribution nets, as described in the "Global Resources (VersaNets)" section on page 2-11.

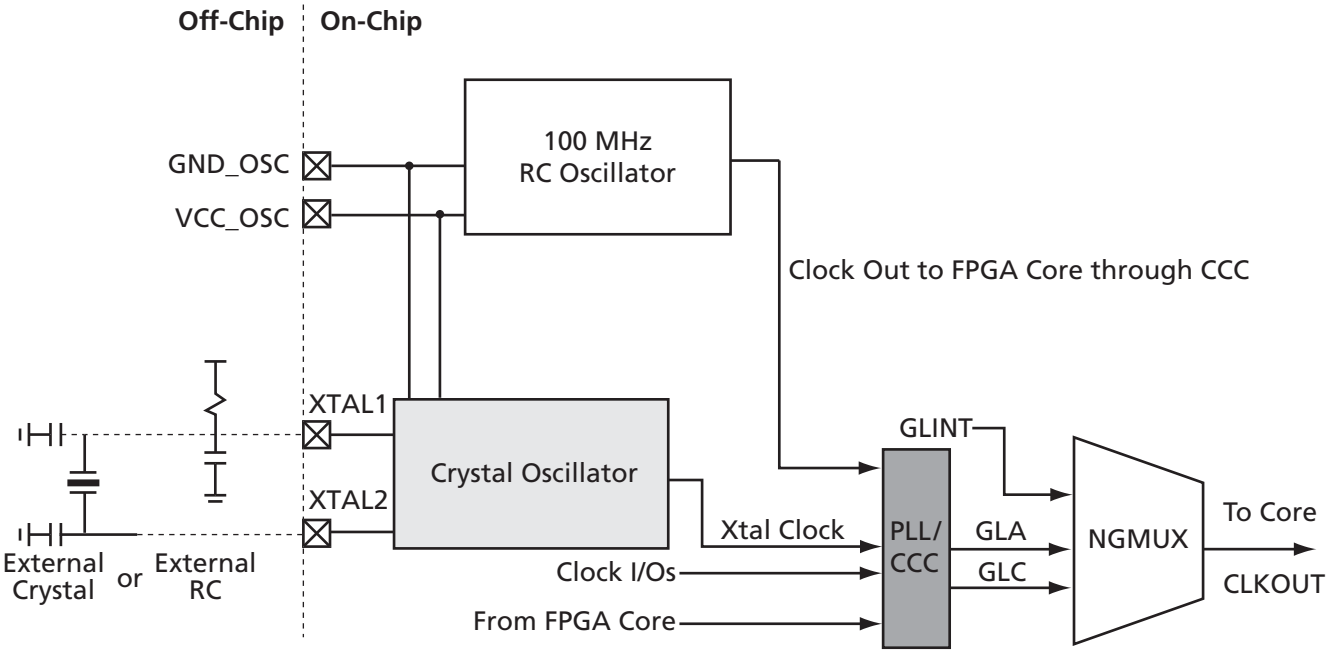


Figure 2-16 • **Fusion Clocking Options**

RC Oscillator

The RC oscillator is an on-chip free running clock source generating a 100 MHz clock. It can be used as a source clock for both on-chip and off-chip resources. When used in conjunction with the Fusion PLL and CCC circuits, the RC oscillator clock source can be used to generate clocks of varying frequency and phase.

The Fusion RC oscillator is very accurate at ±1% over commercial and industrial temperature ranges. It is an automated clock, requiring no setup or configuration by the user. It requires only that the power and GND_OSC pins be connected; no external components are required. The RC oscillator can be used to drive either a PLL or another internal signal.

RC Oscillator Characteristics

Table 2-8 • **Electrical Characteristics of RC Oscillator**

Parameter	Description	Condition	Min.	Typ.	Max.	Units
F_{RC}	Operating Frequency			100		MHz
	Accuracy	Temperature: 0°C to 85°C Voltage: 3.3 V +/– 5%		1		%
		Temperature: –40°C to 125°C Voltage: 3.3 V +/– 5%		3		%
	Output Jitter	Period Jitter (at 5 k cycles)		100		ps
		Cycle–Cycle Jitter (at 5 k cycles)		100		ps
		Period Jitter (at 5 k cycles) with 1 kHz / 300 mV peak-to-peak noise on power supply		150		ps
		Cycle–Cycle Jitter (at 5 k cycles) with 1 kHz / 300 mV peak-to-peak noise on power supply		150		ps
	Output Duty Cycle			50		%
I_{DYNRC}	Operating Current			1		mA

Crystal Oscillator

The on-chip crystal oscillator circuit works with an off-chip crystal to generate a high precision clock. It has an accuracy of 100 ppm (0.01%) and is capable of providing system clocks for Fusion peripherals and other system clock networks, both on-chip and off-chip. When combined with the on-chip CCC/PLL blocks, a wide range of clock frequencies can be created to support various design requirements.

The on-chip circuitry is designed to work with an external crystal, ceramic resonator, or a resistor-capacitor (RC) network. It can only support one of these configurations at a time. Typical design practices dictate that the desired mode for the crystal oscillator be determined and the board designed for a single configuration. The crystal oscillator supports four modes of operation, defined in Table 2-9.

In Mode 0, the oscillator is configured to work with an external RC network. The RC components are connected to the XTAL1 pin, with XTAL2 left floating. The frequency generated by the circuit in Mode 0 is determined by the RC time constant of the selected components (Figure 2-18).

Table 2-9 • **Crystal Oscillator Mode Definition**

Mode	RTCMODE/MODE[1:0]	Recommended Capacitor	Frequency Range (MHz)
RC network (Mode 0)	00	N/A	N/A
Low gain (Mode 1)	01	100 pF	0.032 to 0.20
Medium gain (Mode 2)	10	100 pF	0.20 to 2.0
High gain (Mode 3)	11	15 pF	2.0 to 20.0

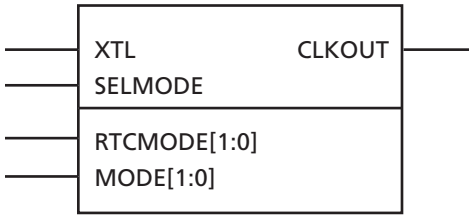


Figure 2-17 • **Crystal Oscillator Macro**

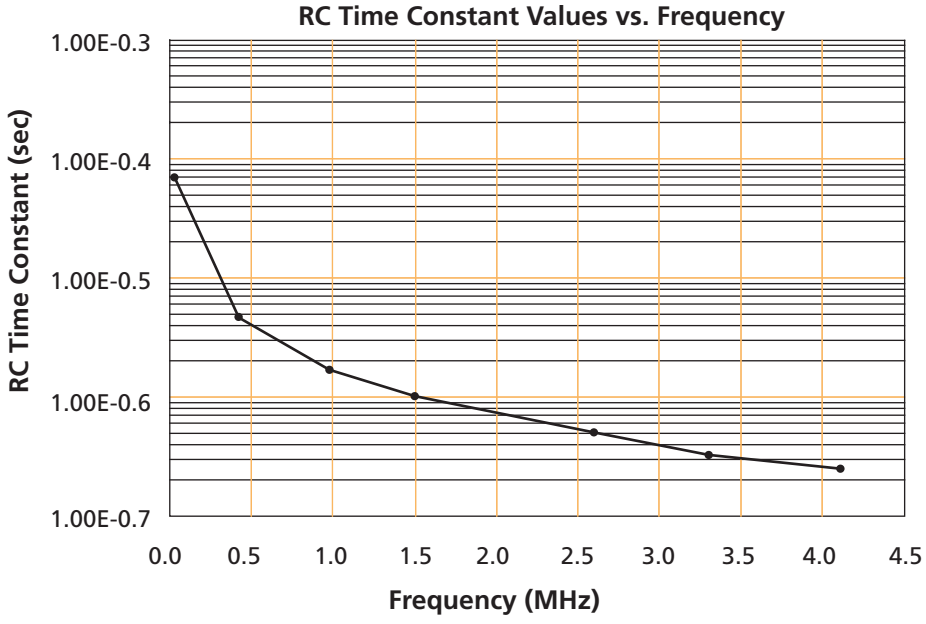


Figure 2-18 • **Crystal Oscillator: RC Time Constant Values vs. Frequency (typical)**

In Modes 1 to 3, the crystal oscillator is configured to support an external crystal or ceramic resonator. These modes correspond to low, medium, and high gain. They differ in the frequency of crystal or resonator that is supported. The crystal or resonator is connected to the XTAL1 and XTAL2 pins. Additionally, a capacitor is required on both XTAL1 and XTAL2 pins to ground (Figure 2-16 on page 2-18). Table 2-9 on page 2-20 details each crystal oscillator mode, supported frequency range, and recommended capacitor value.

A use model supported by the Fusion device involves powering down the core while the real-time counter (RTC) continues to run, clocked by the crystal oscillator. When powered down, the core cannot control crystal oscillator mode pins. Also, some designers may wish to avoid the RTC altogether. To support both situations, the crystal oscillator can be controlled by either the RTC or the FGPA core. If the RTC is instantiated in the design, it will by default use RTCMODE[1:0] to set the crystal oscillator control pins (the default). If the RTC is not used in the design, the FPGA core will set the crystal oscillator control pins with MODE[1:0].

Crystal Oscillator Characteristics

Table 2-10 • **Electrical Characteristics of the Crystal Oscillator**

Parameter	Description	Condition	Min.	Typ.	Max.	Units
F_{XTAL}	Operating Frequency	Using External Crystal	0.032		20	MHz
		Using Ceramic Resonator	0.5		8	MHz
		Using RC Network	0.032		4	MHz
	Output Duty Cycle			50		%
	Output Jitter	With 10 MHz Crystal		50		ps RMS
$I_{DYNXTAL}$	Operating Current	RC		0.6		mA
		0.032–0.2 MHz		0.6		mA
		0.2–2.0 MHz		0.6		mA
		2.0–20.0 MHz		0.6		mA
$I_{STBXTAL}$	Standby Current			10		µA
$PSRR_{XTAL}$	Power Supply Noise Tolerance			0.5		Vp–p
V_{IHXTAL}	Input Logic Level High		90% of V_{CC}			V
V_{ILXTAL}	Input Logic Level Low				10% of V_{CC}	V

Clock Conditioning Circuits

In Fusion devices, the CCCs are used to implement frequency division, frequency multiplication, phase shifting, and delay operations.

The CCCs are available in six chip locations—each of the four chip corners and in the middle of the east and west chip sides.

Each CCC can implement up to three independent global buffers (with or without programmable delay), or a PLL function (programmable frequency division/multiplication, phase shift, and delays) with up to three global outputs. Unused global outputs of a PLL can be used to implement independent global buffers, up to a maximum of three global outputs for a given CCC.

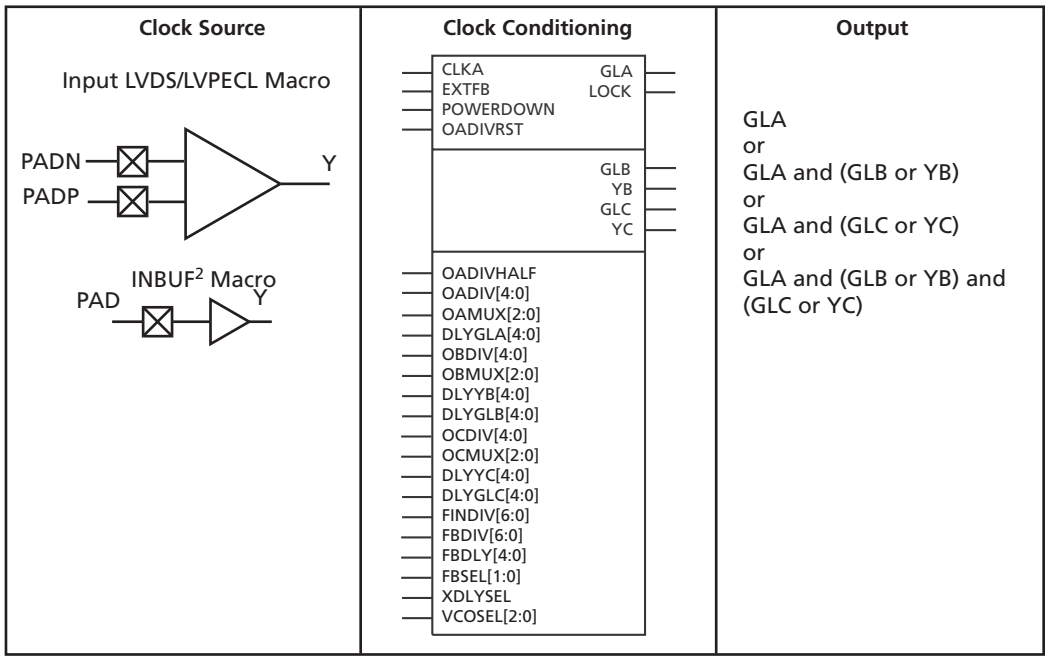
A global buffer can be placed in any of the three global locations (CLKA-GLA, CLKB-GLB, and CLKC-GLC) of a given CCC.

A PLL macro uses the CLKA CCC input to drive its reference clock. It uses the GLA and, optionally, the GLB and GLC global outputs to drive the global networks. A PLL macro can also drive the YB and YC regular core outputs. The GLB (or GLC) global output cannot be reused if the YB (or YC) output is used (Figure 2-19). Refer to the "PLL Macro" section on page 2-27 for more information.

Each global buffer, as well as the PLL reference clock, can be driven from one of the following:

- Three dedicated single-ended I/Os using a hardwired connection
- Two dedicated differential I/Os using a hardwired connection
- The FPGA core

The CCC block is fully configurable, either via Flash configuration bits set in the programming bitstream or through an asynchronous interface. This asynchronous interface is dynamically accessible from inside the Fusion device to permit parameter changes (such as divide ratios) during device operation. To increase the versatility and flexibility of the clock conditioning system, the CCC configuration is determined either by the user during the design process, with configuration data being stored in Flash memory as part of the device programming procedure, or by writing data into a dedicated shift register during normal device operation. This latter mode allows the user to dynamically reconfigure the CCC without the need for core programming. The shift register is accessed through a simple serial interface. Refer to the "CCC and PLL Characteristics" section on page 2-28 for more information.



Notes:

1. *Visit the Actel website for future application notes concerning dynamic PLL reconfiguration. Refer to the "PLL Macro" section on page 2-27 for signal descriptions.*
2. *Many specific INBUF macros support the wide variety of single-ended and differential I/O standards for the Fusion family.*

Figure 2-19 • **Fusion CCC Options: Global Buffers with the PLL Macro**

Table 2-11 • **Available Selections of I/O Standards within CLKBUF and CLKBUF_LVDS/LVPECL Macros**

CLKBUF Macros
CLKBUF_LVCMOS5
CLKBUF_LVCMOS33 [1]
CLKBUF_LVCMOS18
CLKBUF_LVCMOS15
CLKBUF_PCI
CLKBUF_LVDS [2]
CLKBUF_LVPECL

Notes:

1. *This is the default macro. For more details refer to the* Fusion and ProASIC3/E Macro Library Guide.
2. *BLVDS and M-LVDS standards are supported with CLKBUF_LVDS.*

Global Buffers with No Programmable Delays

The CLKBUF and CLKBUF_LVPECL/LVDS macros are composite macros that include an I/O macro driving a global buffer, which are hardwired together (Figure 2-20).

The CLKINT macro provides a global buffer function driven by the FPGA core.

The CLKBUF, CLKBUF_LVPECL/LVDS, and CLKINT macros are pass-through clock sources and do not use the PLL or provide any programmable delay functionality.

Many specific CLKBUF macros support the wide variety of single-ended and differential I/O standards supported by Fusion devices. The available CLKBUF macros are described in the *Fusion and ProASIC3/E Macro Library Guide.*

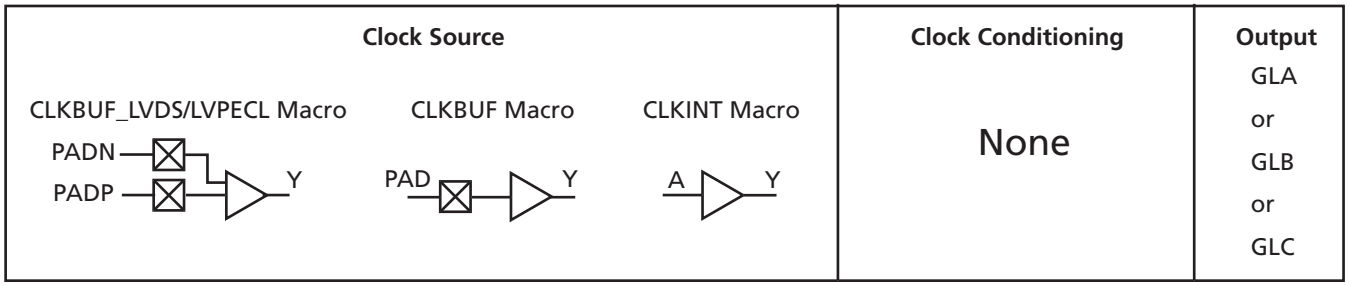


Figure 2-20 • **Global Buffers with No Programmable Delay**

Global Buffers with Programmable Delay

The CLKDLY macro is a pass-through clock source that does not use the PLL, but provides the ability to delay the clock input using a programmable delay (Figure 2-21). The CLKDLY macro takes the selected clock input and adds a user-defined delay element. This macro generates an output clock phase shift from the input clock.

The CLKDLY macro can be driven by an INBUF macro to create a composite macro, where the I/O macro drives the global buffer (with programmable delay) using a hardwired connection. In this case, the I/O must be placed in one of the dedicated global I/O locations.

Many specific INBUF macros support the wide variety of single-ended and differential I/O standards supported by the Fusion family. The available INBUF macros are described in the *Fusion and ProASIC3/E Macro Library Guide.*

The CLKDLY macro can be driven directly from the FPGA core.

The CLKDLY macro can also be driven from an I/O that is routed through the FPGA regular routing fabric. In this case, users must instantiate a special macro, PLLINT, to differentiate from the hardwired I/O connection described earlier.

The visual CLKDLY configuration in the SmartGen part of the Libero IDE and Designer tools allows the user to select the desired amount of delay, and configures the delay elements appropriately. SmartGen also allows the user to select the input clock source. SmartGen will automatically instantiate the special macro, PLLINT, when needed.

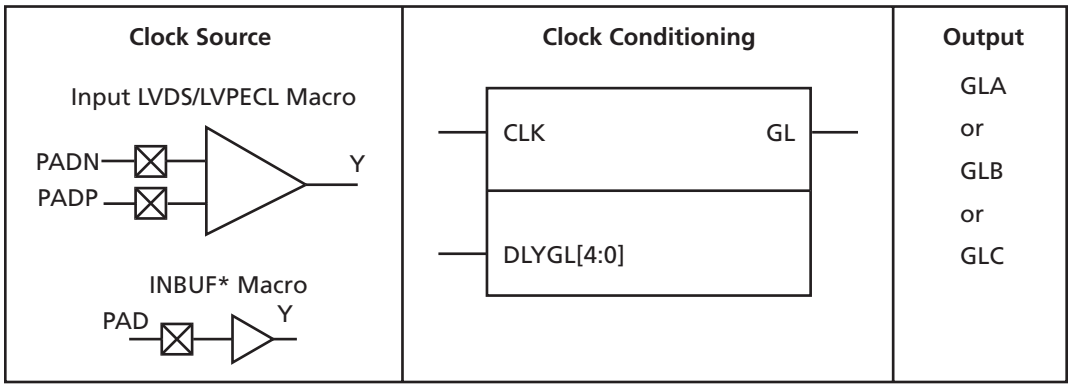
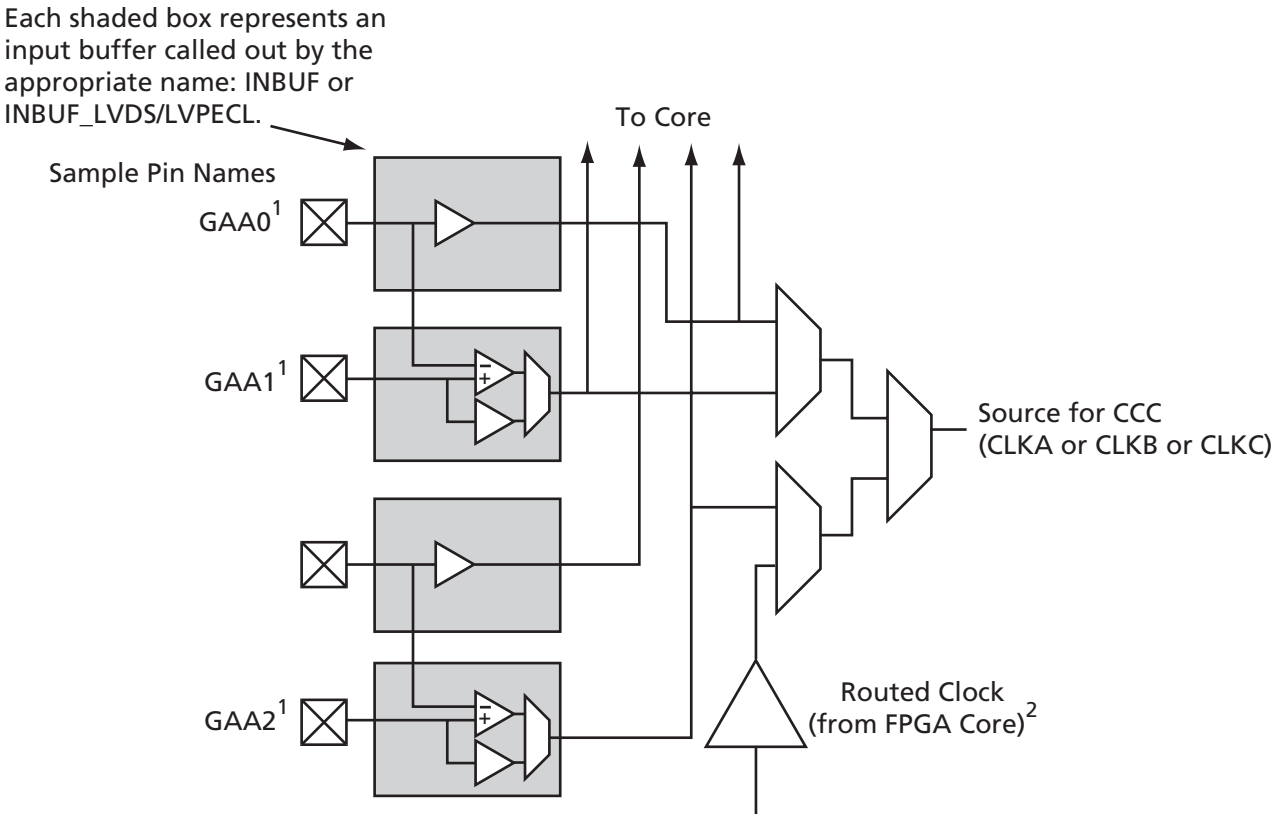


Figure 2-21 • **Fusion CCC Options: Global Buffers with Programmable Delay**

Global Input Selections

Each global buffer, as well as the PLL reference clock, can be driven from one of the following (Figure 2-22):

- Three dedicated single-ended I/Os using a hardwired connection
- Two dedicated differential I/Os using a hardwired connection
- The FPGA core



Notes:

1. *Represents the global input pins. Globals have direct access to the clock conditioning block and are not routed via the FPGA fabric. Refer to the "User I/O Naming Convention" section on page 2-118 for more information.*
2. *Instantiate the routed clock source input as follows:*
   a) Connect the output of a logic element to the clock input of the PLL, CLKDLY, or CLKINT macro.
   b) Do not place a clock source I/O (INBUF or INBUF_LVPECL/LVDS) in a relevant global pin location.
3. *LVDS-based clock sources are available in the east and west banks on all Fusion devices.*

Figure 2-22 • **Clock Input Sources Including CLKBUF, CLKBUF_LVDS/LVPECL, and CLKINT**

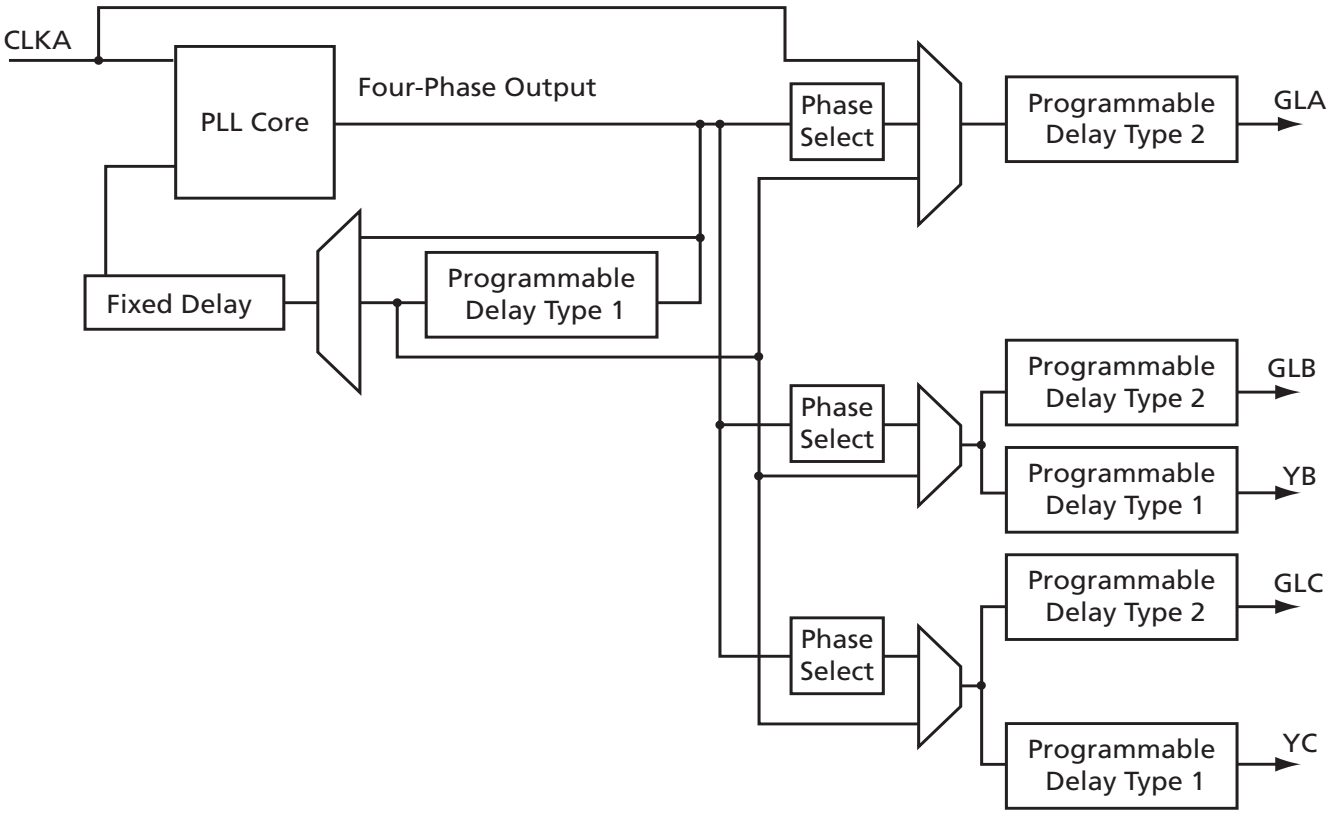
CCC Physical Implementation

The CCC circuit is composed of the following (Figure 2-23):

- PLL core
- Three phase selectors
- Six programmable delays and one fixed delay
- Five programmable frequency dividers that provide frequency multiplication/division (not shown in Figure 2-23 because they are automatically configured based on the user's required frequencies)
- One dynamic shift register that provides CCC dynamic reconfiguration capability (not shown).

CCC Programming

The CCC block is fully configurable. It is configured via static Flash configuration bits in the array, set by the user in the programming bitstream, or configured through an asynchronous dedicated shift register dynamically accessible from inside the Fusion device. The dedicated shift register permits parameter changes such as PLL divide ratios and delays during device operation. This latter mode allows the user to dynamically reconfigure the PLL without the need for core programming. The register file is accessed through a simple serial interface.



Note: *Clock divider and multiplier blocks are not shown in this figure or in SmartGen. They are automatically configured based on the user's required frequencies.*

Figure 2-23 • **PLL Block**

PLL Macro

The PLL functionality of the clock conditioning block is supported by the PLL macro. Note that the PLL macro reference clock uses the CLKA input of the CCC block, which is only accessible from the global A[0:2] package pins. Refer to Figure 2-22 on page 2-25 for more information.

The PLL macro provides five derived clocks (three independent) from a single reference clock. The PLL feedback loop can be driven either internally or externally. The PLL macro also provides power-down input and lock output signals. See Figure 2-19 on page 2-22 for more information.

Inputs:

- CLKA: selected clock input
- POWERDOWN (active low): disables PLLs. The default state is power-down on (active low).

Outputs:

- LOCK (active high): indicates that PLL output has locked on the input reference signal
- GLA, GLB, GLC: outputs to respective global networks
- YB, YC: allows output from the CCC to be routed back to the FPGA core

As previously described, the PLL allows up to five flexible and independently configurable clock outputs. Figure 2-23 on page 2-26 illustrates the various clock output options and delay elements.

As illustrated, the PLL supports three distinct output frequencies from a given input clock. Two of these (GLB and GLC) can be routed to the B and C global networks, respectively, and/or routed to the device core (YB and YC).

There are five delay elements to support phase control on all five outputs (GLA, GLB, GLC, YB, and YC).

There is also a delay element in the feedback loop that can be used to advance the clock relative to the reference clock.

The PLL macro reference clock can be driven by an INBUF macro to create a composite macro, where the I/O macro drives the global buffer (with programmable delay) using a hardwired connection. In this case, the I/O must be placed in one of the dedicated global I/O locations.

The PLL macro reference clock can be driven directly from the FPGA core.

The PLL macro reference clock can also be driven from an I/O that is routed through the FPGA regular routing fabric. In this case, users must instantiate a special macro, PLLINT, to differentiate it from the hardwired I/O connection described earlier.

The visual PLL configuration in SmartGen, available with the Libero IDE and Designer tools, will derive the necessary internal divider ratios based on the input frequency and desired output frequencies selected by the user. SmartGen allows the user to select the various delays and phase shift values necessary to adjust the phases between the reference clock (CLKA) and the derived clocks (GLA, GLB, GLC, YB, and YC). SmartGen also allows the user to select where the input clock is coming from. SmartGen automatically instantiates the special macro, PLLINT, when needed.

CCC and PLL Characteristics

Timing Characteristics

Table 2-12 • **Fusion CCC/PLL Specification**

Parameter	Min.	Typ.	Max.	Unit
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}	1.5		350	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}	0.75		350	MHz
Delay Increments in Programmable Delay Blocks[1, 2]		200		ps
Number of Programmable Values in Each Programmable Delay Block			32	
Input Period Jitter			1.5	ns
CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT}	Max Peak-to-Peak Period Jitter			
	1 Global Network Used		3 Global Networks Used	
0.75 MHz to 24 MHz	0.50%		0.70%	
24 MHz to 100 MHz	1.00%		1.20%	
100 MHz to 250 MHz	1.75%		2.00%	
250 MHz to 350 MHz	2.50%		5.60%	
Acquisition Time			150	µs
Output Duty Cycle	48.5		51.5	%
Delay Range in Block: Programmable Delay 1 [1, 2]	0.6		5.56	ns
Delay Range in Block: Programmable Delay 2 [1, 2]	0.025		5.56	ns
Delay Range in Block: Fixed Delay [1, 2]		2.2		ns

Notes:

1. *This delay is a function of voltage and temperature. See Table 3-6 on page 3-6 for deratings.*
2. *T_J = 25°C, V_{CC} = 1.5 V*

No Glitch MUX (NGMUX)

Positioned downstream from the PLL/CCC blocks, the NGMUX provides a special switching sequence between two asynchronous clock domains that prevents generating any unwanted narrow clock pulses. The NGMUX is used to switch the source of a global between three different clock sources. Allowable inputs are either two PLL/CCC outputs or a PLL/CCC output and a regular net, as shown in Figure 2-24. The GLMUXCFG[1:0] configuration bits determine the source of the CLK inputs (i.e., internal signal, GLA, or GLC). These are set by SmartGen during design, but can also be changed by dynamically reconfiguring the PLL. The GLMUXSEL[1:0] bits control which clock source is passed through the NGMUX to the global network (GL). See Table 2-13.

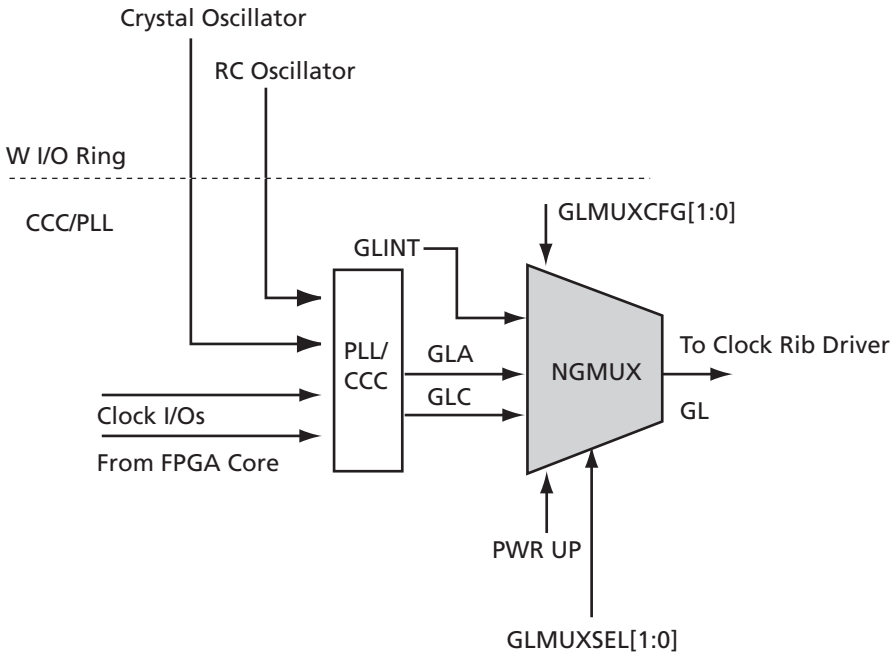


Figure 2-24 • **NGMUX**

Table 2-13 • **NGMUX Configuration and Selection Table**

GLMUXCFG[1:0]	GLMUXSEL[1:0]		Selected Input Signal	MUX Type
00	X	0	GLA	2-to-1 GLMUX
	X	1	GLC	
01	X	0	GLA	2-to-1 GLMUX
	X	1	GLINT	
10	X	0	GLC	2-to-1 GLMUX
	X	1	GLINT	
11	0	0	GLA	3-to-1 GLMUX
	0	1	GLC	
	1	0	GLINT	
	1	1	GND	

The NGMUX macro is simplified to show the two clock options that have been selected by the GLMUXCFG[1:0] bits. Figure 2-25 illustrates the NGMUX macro. During design, the two clock sources are connected to CLK0 and CLK1 and are controlled by GLMUXSEL[1:0] to determine which signal is to be passed through the MUX.

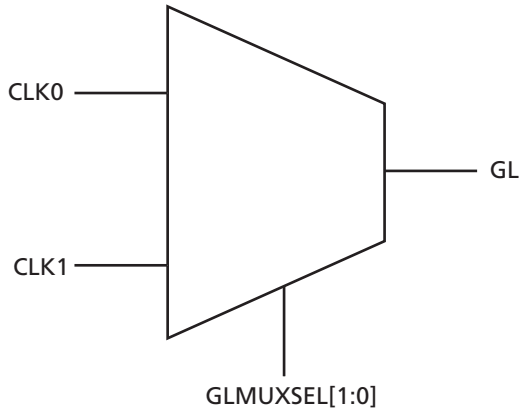


Figure 2-25 • **NGMUX Macro**

The sequence of switching between two clock sources (from CLK0 to CLK1) is as follows (Figure 2-26):

- GLMUXSEL[1:0] transitions to initiate a switch.
- GL drives one last complete CLK0 positive pulse (i.e., one rising edge followed by one falling edge).
- From that point, GL stays low until the second rising edge of CLK1 occurs.
- At the second CLK1 rising edge, GL will begin to continuously deliver CLK1 signal.
  Minimum t_{sw} = 0.05 ns at 25°C (typical conditions).

For examples of NGMUX operation, refer to the *Peripherals User's Guide*.

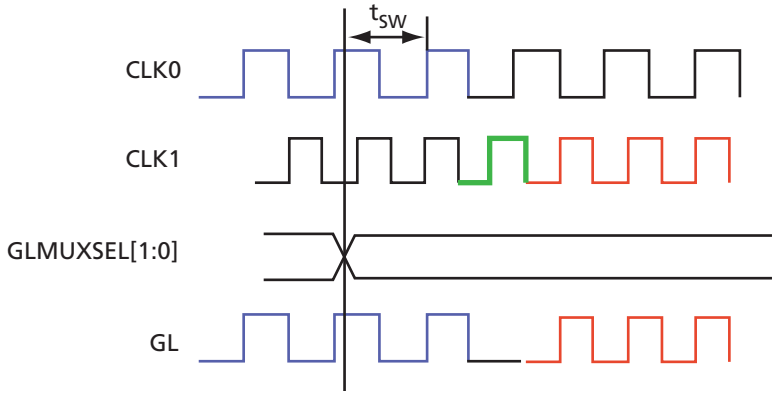


Figure 2-26 • **NGMUX Waveform**

Real-Time Counter System

The addition of the RTC system enables Fusion devices to support both standby and sleep modes of operation, greatly reducing power consumption in many applications.

The RTC system comprises six blocks that work together to provide this increased functionality and reduced power consumption. Figure 2-27 shows these blocks and how they are connected.

- RTC (Figure 2-28)
- Crystal oscillator
- V_{CC33UP} detector
- Voltage regulator initialization
- Voltage regulator logic
- 1.5 V voltage regulator

The RTC provides a counter as well as a MATCH output signal that may be used in the FPGA and, optionally, to power-up the on-chip 1.5 V voltage regulator and provide a 1.5 V power source (in conjunction with an external pass transistor) to the FPGA fabric portion of the Fusion silicon device. The FPGA fabric can then be used to power-down the 1.5 V voltage regulator.

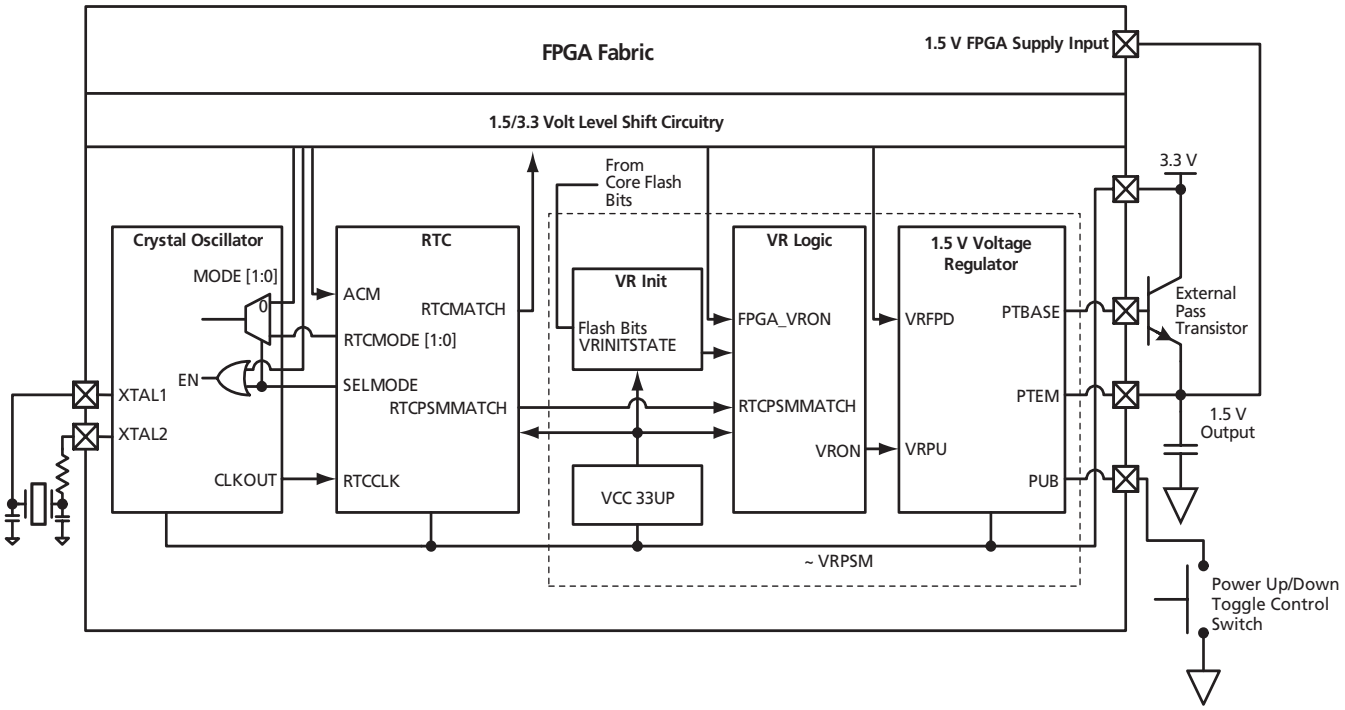


Figure 2-27 • **Real-Time Counter System**

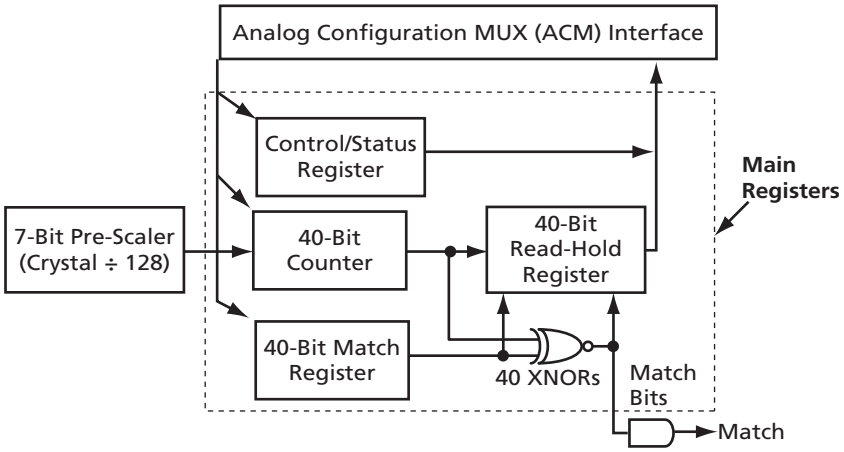


Figure 2-28 • **RTC Block Diagram**

Real-Time Counter

The RTC can be configured to power up the FPGA fabric at a specific time or periodically. Custom user logic or a soft microcontroller within the FPGA fabric portion of the Fusion device can be programmed to read and modify the registers in the RTC. Based on this information or other internal or external conditions, the FPGA may decide to power down the voltage regulator and thereby shut off the FPGA fabric.

The 3.3 V supply must be valid and the crystal oscillator (nominally 32.768 kHz) enabled for self-time wake-up/restart operation. When operating from the 3.3 V supply and the 1.5 V core voltage is disabled, the ACM interface to the FPGA is disabled.

A 40-bit loadable counter is used as the primary timekeeping element within the RTC. This counter can be configured to reset itself when a count value is reached that matches the value set within a 40-bit match register. Note that the only exception to this self-clearing mechanism occurs when the 40-bit counter is equal to 0 (0x0000000000), since the counter would never increment from zero. When the device is first powered up (i.e., when the 3.3 V supply becomes valid) the 40-bit counter and 40-bit match register are cleared to logic 0, and the MATCH output signal is active (logic 1). At any time when the 40-bit counter value does not match the value in the 40-bit match register, the MATCH output signal will become inactive (logic 0).

Both the counter and match registers are addressable (read/write) from the FPGA and through a JTAG instruction. The RTC is considered part of the analog system and is accessed via ACM. Refer to the "Analog Configuration MUX" section on page 2-88 for detailed instructions on writing to the RTC via the ACM. The counter action can be suspended/resumed by clearing/setting the Cntr_En bit in the Control/Status Register.

If a 32.768 kHz external crystal is connected to the crystal oscillator pad, the 40-bit counter will have a maximum count of 4,294,967,296 seconds, which equates to just over 136 years of elapsed timekeeping with a minimum period of 1/256 second, which will be the toggle rate of the LSB bit of the 40-bit counter.

Frequencies other than 32.768 kHz can be used as a clock source, with the appropriate scaling of the LSB time interval. Maximum input clock frequency is 20 MHz (the crystal oscillator limit).

The RTC signals are included in the Analog Block macro. The signal functions and descriptions are listed in Table 2-14.

A Fusion use model includes the RTC controlling the power-up state of the FPGA core via the 1.5 V regulator. To support this model, the crystal oscillator must be running and configured when the FPGA is powered off. Hence, when the RTC is enabled in the system design, it will configure the crystal oscillator via the RTCXTLMODE[1:0] and RTCXTLSEL pins.

A 7-bit pre-scaler block is used to divide the source clock (from the external crystal) by 128. This pre-scaled 50%-duty-cycle clock signal is then used by the counter logic as its reference clock. Given an external crystal frequency of 32.768 kHz, the pre-scaler output clock will toggle at a rate of 32.768 kHz / 128 = 256 Hz.

The RTC is built from and controlled by a set of registers, denoted "Main Registers" in Figure 2-27 on page 2-31. These registers are accessed via the ACM.

The FPGA fabric portion of the Fusion device must be powered up and active at least once to write to the various registers within the RTC to initialize them for the user's application. Users set up the RTC by configuring it from the Actel SmartGen tool implementing custom logic, or programming a soft microcontroller.

The 40-bit counter and match register are each divided into five bytes. Each byte is directly addressable by the ACM. The address map of registers accessed through the ACM and used by the RTC is shown in Table 2-15 on page 2-33.

Table 2-14 • **RTC Macro Signal Description**

Signal Name	Number of Bits	Direction	Function
RTCMATCH	1	Out	Match between 40-bit counter and match register
RTCPSMMATCH	1	Out	RTCMATCH connected to voltage regulator power supply monitor (VRPSM) (Figure 2-30 on page 2-36)
RTCXTLMODE[1:0]	2	Out	Drives XTLOSC RTCMODE[1:0] pins
RTCXTLSEL	1	Out	Drives XTLOSC SELMODE pin
RTCCLK	1	In	RTC clock input from XTLOSC CLKOUT pin

Table 2-15 • **RTC ACM Memory Map**

ACM_ADDR[7:0]	Decimal	Register Name	Description	Use
0x40	64	COUNTER0	Counter bits 7:0	Used to preload the counter to a specified start point. Default setting is all zeroes.
0x41	65	COUNTER1	Counter bits 15:8	
0x42	66	COUNTER2	Counter bits 23:16	
0x43	67	COUNTER3	Counter bits 31:24	
0x44	68	COUNTER4	Counter bits 39:32	
0x48	72	MATCHREG0	Match register bits 7:0	The RTC uses a 40-bit register to compare against the 40-bit counter value to determine when a match occurs. This 40-bit match register, like the counter, is broken into 5 bytes (MATCHREG0–4).
0x49	73	MATCHREG1	Match register bits 15:8	
0x4a	74	MATCHREG2	Match register bits 23:16	
0x4b	75	MATCHREG3	Match register bits 31:24	
0x4c	76	MATCHREG4	Match register bits 39:32	
0x50	80	MATCHBITS0	Individual Match bits 7:0	Each bit of the 40-bit counter is compared to each bit of the 40-bit match register via XNOR gates. These 40 match bits are partitioned into 5 bytes.
0x51	81	MATCHBITS1	Individual Match bits 15:8	
0x52	82	MATCHBITS2	Individual Match bits 23:16	
0x53	83	MATCHBITS3	Individual Match bits 31:24	
0x54	84	MATCHBITS4	Individual Match bits 39:32	
0x58	88	CTRL_STAT	Control (write) / Status (read) register bits 7:0	Control (write) / Status (read) register bits 7:0
0x59	89	TEST_REG	Test register(s)	Test register(s)

The control/status register (CTRL_STAT) is an 8-bit register that defines the operation of the RTC. The control register can reset the RTC, enabling operation to begin with all zeroes in the counter. The RTC can be configured to clear upon a match with the Match register, or it can continue to count while still setting the match signal. To enable the Fusion device to power up at a specific time or at periodic intervals, the RTC can be configured to turn on the 1.5 V voltage regulator. Table 2-16 details the CTRL_STAT settings.

Table 2-16 • **RTC Control/Status Register**

Bit	Name	Description
7	rtc_rst	RTC Reset: Writing a logic 1 to this bit causes an RTC reset.[2] Writing a logic 0 to this bit will allow synchronous deassertion of reset after 2 ACM_CLK cycles if V_{CC33UP} = 1.[3]
6	cntr_en	Counter Enable: A logic 1 in this bit will enable the counter if the RTC is not in reset. It takes 64 RTCCLK positive edges (1/2 of the pre-scaler division factor), after reset is removed and cntr_en = 1, before the counter is incremented.[4] A logic 0 in this bit resets the pre-scaler and therefore suspends incrementing the counter, but the counter is not reset. Before writing to the counter registers, the counter must be disabled.
5	vr_en_mat	Voltage Regulator Enable on Match: Writing a logic 1 to this bit will allow the RTCMATCH output port to go to logic 1 when a match occurs between the 40-bit counter and the 40-bit match register. Logic 0 forces RTCMATCH to logic 0, to prevent enabling the voltage regulator from the RTC.
4:3	xt_mode[1:0]	Crystal Oscillator Mode: These bits control the RTCXTLMODE[1:0] output ports that are connected to the RTCMODE[1:0] input pins of the crystal oscillator pad. For 32 kHz crystal operation, this should be set to '01'. (See the "Crystal Oscillator" section on page 2-20.)
2	rst_cnt_omat	Reset Counter on Match: A logic 1 written to this bit allows the counter to clear itself when a match occurs. In this situation, the 40-bit counter clears on the next rising edge of the pre-scaled clock, approximately 4 ms after the match occurs (the pre-scaled clock toggles at a rate of 256 Hz, given a 32.768 kHz external crystal). A logic 0 written to this bit allows the counter to increment indefinitely, while still allowing match events to occur.
1	rstb_cnt	Counter Reset: A logic 0 resets the 40-bit counter value to 0. A logic 1 allows the counter to count.[4]
0	xtal_en	Crystal Oscillator Enable: This bit controls the RTCXTLSEL output port that is connected to the SELMODE input pin of the crystal oscillator. If a logic 0 is written to this bit, only the FPGA fabric can be used to control the crystal oscillator EN and MODE[1:0] inputs. If a logic 1 is written to this bit, only the RTC can be used to control the RTCXTLSEL and RTCMODE[1:0] inputs of the crystal oscillator. This bit must be set to 1 to allow the RTC counter to function if the 1.5 V supply is off.

Notes:

1. *Default state (set when V_{CC33UP} = 0) for bits 0–7 is logic 0.*
2. *Reset of all RTC states (except this Control/Status register) occurs asynchronously if V_{CC33UP} = 0 or CTRL_STAT bit 7 (rtc_rst) is set to 1.*
3. *Reset is removed synchronously after 2 rising edges of ACM_CLK, following both V_{CC33UP} = 1 and rtc_rst = 0.*
4. *Counter will first increment on the 64th rising edge of RTCCLK after all of the following are true:*
   a. reset is removed
   b. rstb_cnt (CTRL_STAT bit 1) is set to 1
   c. cntr_en (CTRL_STAT bit 6) is set to 1

   and will then increment every 128 RTCCLK cycles.

Crystal Oscillator (Xtal Osc)

When used as the clock source for the RTC, the crystal oscillator will be configured by the RTC with the RTCXTLMODE[1:0] RTC macro pins. Refer to the "Crystal Oscillator" section on page 2-20 for specific details on crystal oscillator operation.

The crystal oscillator input to the RTC is divided by 128, so bit 0 of the RTC toggles at the frequency of the crystal oscillator divided by 128. The frequencies of the RTC are gated by those of the crystal oscillator; from 32.768 kHz to 20 MHz. When used with a 32.768 kHz crystal, bit 0 of the of RTC has a period of ~3.9 ms (1/(32,768/128), or 1/256 seconds), and bit 7 has a period of 1 second.

Voltage Regulator Initialization (VR Init)

The VR Init block determines voltage regulator behavior when the 3.3 V supply is valid. The Fusion devices support different use models. Some of these require the 1.5 V voltage regulator to turn on when the 3.3 V supply is stable. Other use models require additional conditions to be met before the 1.5 V VR turns on. Since the FPGA is not operating when the 3.3 V supply is off, the VR Init lets the user define VR behavior at design time. Two bits can be set within the core, which the VR Init will read as it comes out of reset and either turn on the VR or leave it in an off state.

Voltage Regulator (VR) Logic

The Voltage Regulator Logic block, along with the VR, combines commands from the FPGA, RTC, VR Init block, V_{CC33UP} detector, and PUB pad, to determine whether or not the VR is enabled.

The VR can be enabled from several sources: the PUB pin, the RTC_MATCH signal from the RTC block, or triggered by the VR Init block. Once triggered, the VR will remain on. Only the FPGA fabric can disable the VR, unless the V_{CC33A} supply falls below the V_{CC33UP} threshold and a reset occurs.

1.5 V Voltage Regulator

The VR generates a 1.5 V power supply from the 3.3 V power supply. The 1.5 V output is intended to supply all 1.5 V needs of the Fusion device. This regulator requires an external bipolar pass transistor(Figure 2-29). The VR can drive up to 20 mA of current through the PTBASE pad. The amount of 1.5 V current available is dependent upon the gain of the external pass transistor used. Enable for this block is generated in the VR Logic block or from the PUB pin.

The 1.5 V is not supplied internally to the Fusion device. It must be routed externally to the V_{CC} pins on the device. Therefore the user is not required to use the VR and can use an off-chip 1.5 V supply if desired.

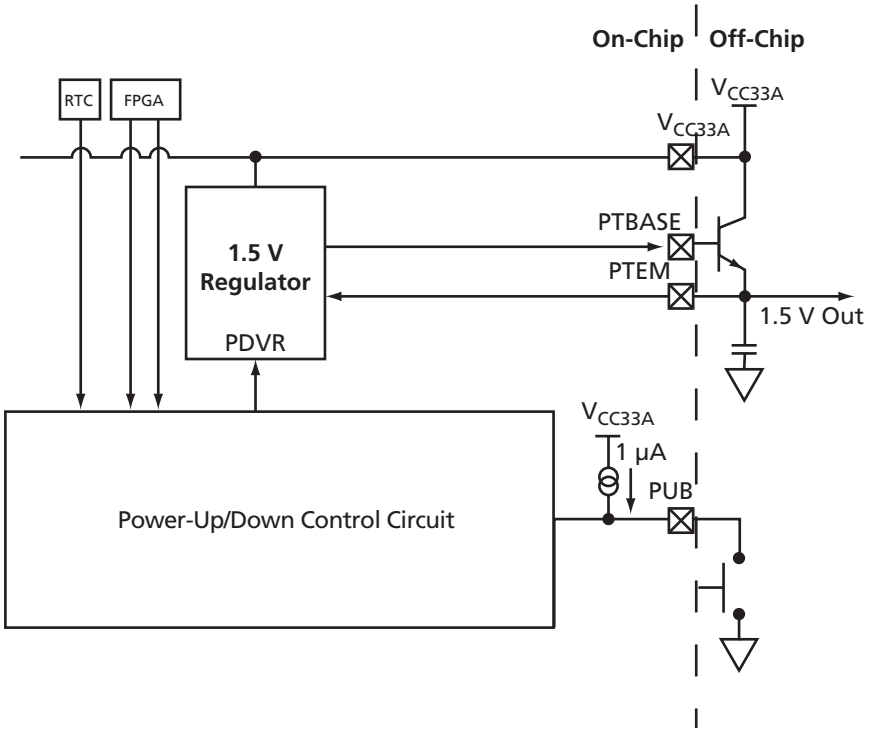


Figure 2-29 • **Voltage Regulator**

Voltage Regulator Power Supply Monitor (VRPSM)

As the functions of the VR Logic and Power System Monitor work closely together to control the power-up state of the FPGA core, these functions were combined into a single VRPSM macro (Figure 2-30).

The signals for the VRPSM macro are listed in Table 2-17. The PUB input comes from the PUB pin on the device and can be pulled high by a signal external to the Fusion device. This can be used to wake up from a standby condition. The inputs VRINITSTATE and RTCPSMMTACH come from the VR Init and RTC blocks, respectively, and either can initiate a VR power-up.

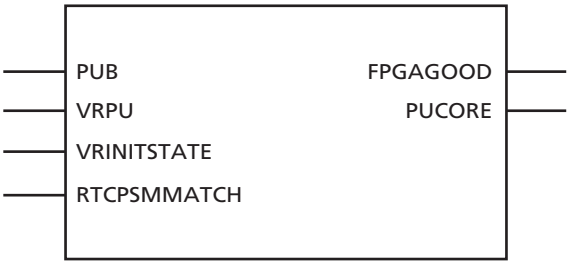


Figure 2-30 • **VRPSM Macro**

Table 2-17 • **Signals for VRPSM Macro**

Signal Name	Number of Bits	Direction	Function
PUB	1	Input	Active low power-up
VRPU	1	Input	Voltage regulator power-up
VRINITSTATE	1	Input	FPGAGOOD initial value (set by 2 Flash bits in FPGA)
RTCPSMMATCH	1	Input	Connected to RTCPSMMATCH signal from RTC
FPGAGOOD	1	Output	Indicates that FPGA is logically functional
PUCORE	1	Output	Power-up to core

Embedded Memories

Fusion devices include four types of embedded memory: Flash block, FlashROM, SRAM, and FIFO.

Flash Memory Block

Fusion is the first FPGA that offers a Flash memory block (FB). Each FB block stores 2 Mbits of data. The Flash memory block macro is illustrated in Figure 2-31. The port pin name and descriptions are detailed on Table 2-18 on page 2-38. All Flash memory block signals are active high, except for CLK and active low RESET. All Flash memory operations are synchronous to the rising edge of CLK.

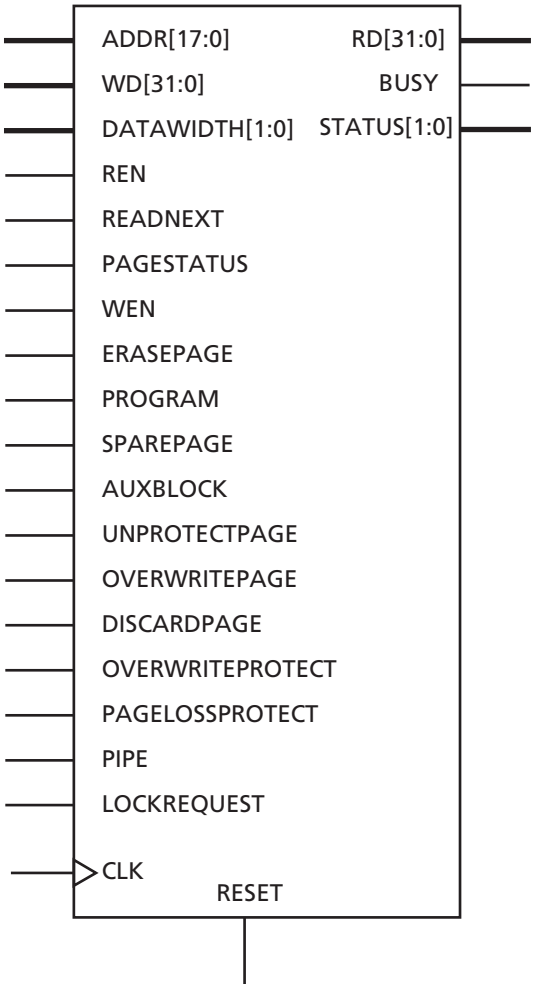


Figure 2-31 • **Flash Memory Block**

Flash Memory Block Pin Names

Table 2-18 • **Flash Memory Block Pin Names**

Interface Name	Width	Direction	Description
ADDR[17:0]	18	In	Byte offset into the FB. Byte based address.
AUXBLOCK	1	In	When asserted, the page addressed is used to access the auxiliary block within that page.
BUSY	1	Out	When asserted, indicates that the FB is performing an operation.
CLK	1	In	User interface clock. All operations and status are synchronous to the rising edge of this clock.
DATAWIDTH[1:0]	2	In	Data width 00 = 1 byte in RD/WD[7:0] 01 = 2 bytes in RD/WD[15:0] 1x = 4 bytes in RD/WD[31:0]
DISCARDPAGE	1	In	When asserted, the contents of the Page Buffer are discarded so that a new page write can be started.
ERASEPAGE	1	In	When asserted, the contents of the Page Buffer are discarded so that a new page write can be started.
LOCKREQUEST	1	In	When asserted, indicates to the JTAG controller that the fpga interface is accessing the FB.
OVERWRITEPAGE	1	In	When asserted, the page addressed is overwritten with the contents of the Page Buffer if the page is writable.
OVERWRITEPROTECT	1	In	When asserted, all program operations will set the overwrite protect bit of the page being programmed.
PAGESTATUS	1	In	When asserted with REN, initiates a read page status operation.
PAGELOSSPROTECT	1	In	When asserted, a modified Page Buffer must be programmed or discarded before accessing a new page.
PIPE	1	In	Adds a pipeline stage to the output for operation above 50 MHz.
PROGRAM	1	In	When asserted, writes the contents of the Page Buffer into the FB page addressed.
RD[31:0]	32	Out	Read data
READNEXT	1	In	When asserted with REN, initiates a read-next operation.
REN	1	In	When asserted, initiates a read operation.
RESET	1	In	When asserted, resets the state of the FB (active low).
SPAREPAGE	1	In	When asserted, the sector addressed is used to access the spare page within that sector.
STATUS[1:0]	2	Out	Status of the last operation completed: 00: Successful completion 01: Read/Unprotect-Page: single error detected and corrected Write: operation addressed a write-protected page Erase-Page: protection violation Program: Page Buffer is unmodified Protection violation 10: Read/Unprotect-Page: two or more errors detected 11: Write: attempt to write to another page before programming current page Erase-Page/Program: page write count has exceeded the 10-year retention threshold
UNPROTECTPAGE	1	In	When asserted, the page addressed is copied into the Page Buffer and the Page Buffer is made writable.
WD[31:0]	32	In	Write data
WEN	1	In	When asserted, store WD in the page buffer.

All Flash memory block input signals are active high, except for RESET.

Flash Memory Block Diagram

A simplified diagram of the Flash memory block is shown in Figure 2-32.

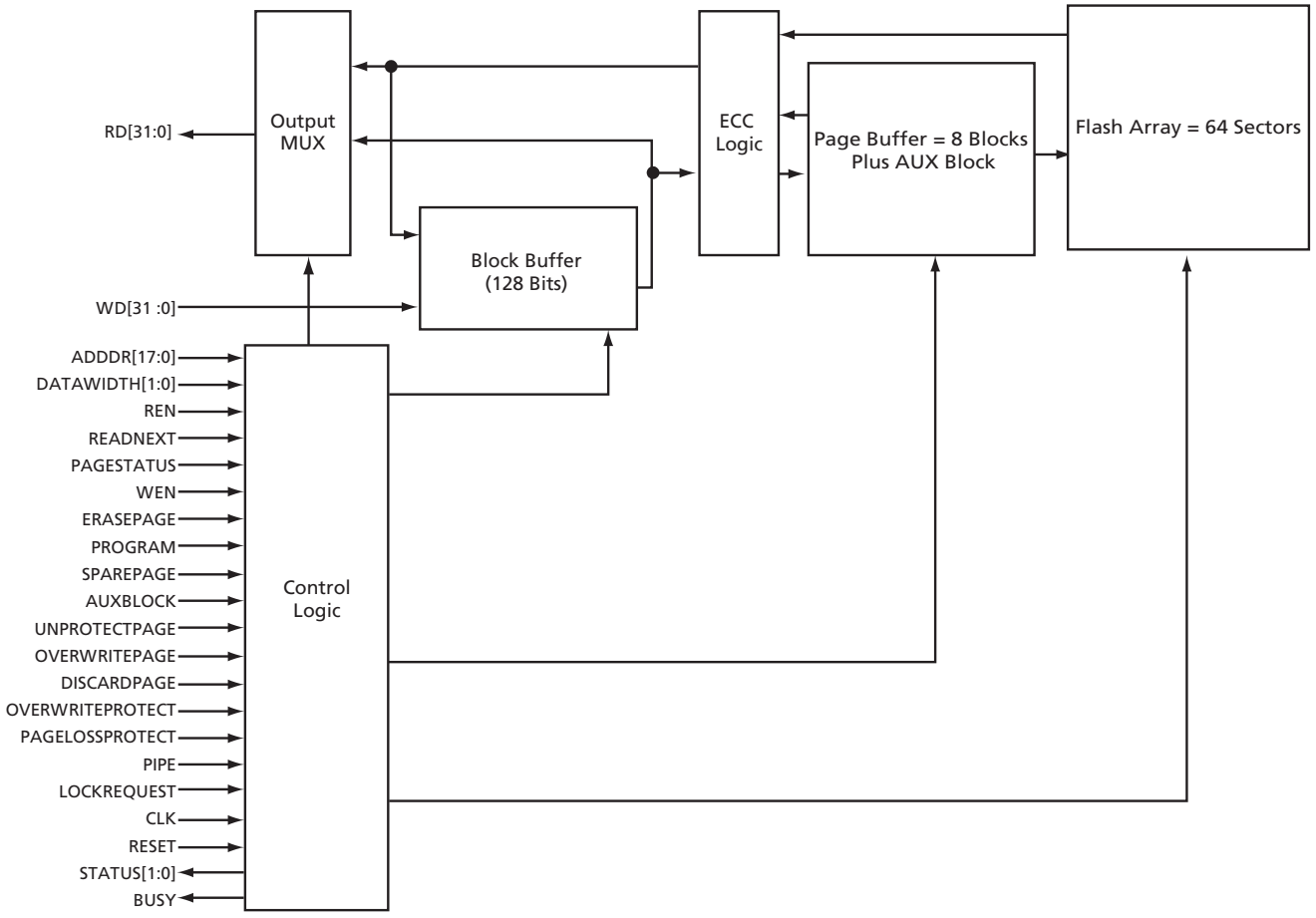


Figure 2-32 • **Flash Memory Block Diagram**

The logic consists of the following sub-blocks:

- Flash Array

  Contains all stored data. The Flash array contains 64 sectors, and each sector contains 33 pages of data.
- Page Buffer

  Is a page-wide volatile register. A page contains 8 blocks of data and an AUX block.
- Block Buffer

  Contains the contents of the last block accessed. A block contains 128 data bits.
- ECC Logic

  The FB stores error correction information with each block to perform single-bit error correction and double-bit error detection on all data blocks.

Flash Memory Block Addressing

Figure 2-33 shows a graphical representation of the Flash memory block.

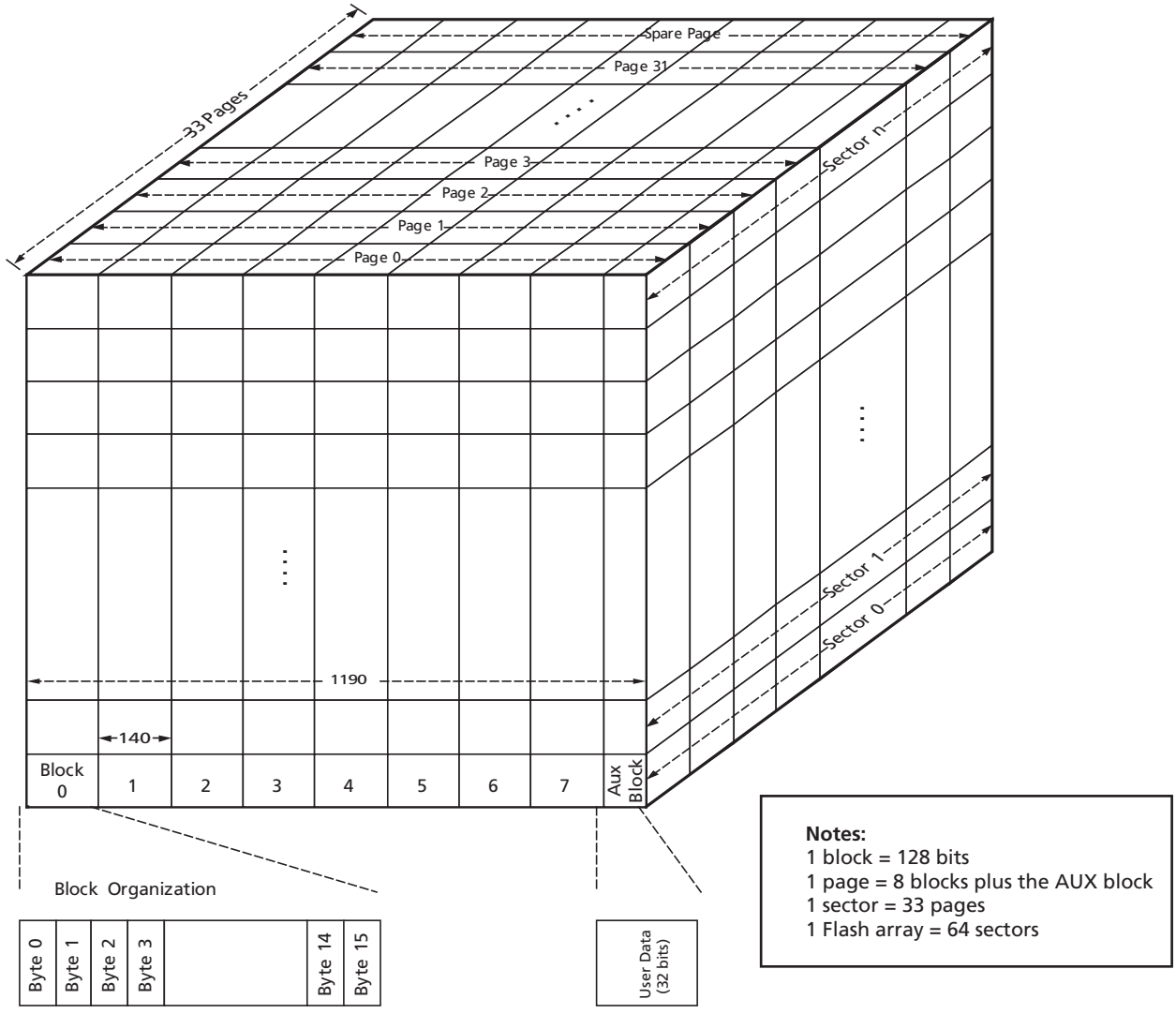


Figure 2-33 • **Flash Memory Block Organization**

Each FB is partitioned into sectors, pages, blocks, and bytes. There are 64 sectors in an FB, and each sector contains 32 pages and 1 spare page. Each page contains 8 data blocks and 1 auxiliary block. Each data block contains 16 bytes of user data, and the auxiliary block contains 4 bytes of user data.

Addressing for the FB is shown in Table 2-19.

Table 2-19 • **FB Address Bit Allocation ADDR[17:0]**

17	12	11	7	6	4	3	0
Sector		Page		Block		Byte	

When the spare page of a sector is addressed (SPAREPAGE active), ADDR[11:7] are ignored.

When the Auxiliary block is addressed (AUXBLOCK active), ADDR[6:2] are ignored.

Note: The spare page of sector 0 is unavailable for any user data. Writes to this page will return an error, and reads will return all zeroes.

Data operations are performed in widths of 1 to 4 bytes. A write to a location in a page that is not already in the Page Buffer will cause the page to be read from the FB Array and stored in the Page Buffer. The block that was addressed during the write will be put into the Block Buffer and the data written by WD will overwrite the data in the Block Buffer. After the data is written to the Block Buffer, the Block Buffer is then written to the Page Buffer to keep both buffers in sync. Subsequent writes to the same block will overwrite the Block Buffer and the Page Buffer. A write to another block in the page will cause the addressed block to be loaded from the Page Buffer, and the write will be performed as described previously.

The data width can be selected dynamically via the DATAWIDTH input bus. The truth table for the data width settings is detailed in Table 2-20. The minimum resolvable address is one 8-bit byte. For data widths greater than 8 bits, the corresponding address bits are ignored (when DATAWIDTH = 0 (2 bytes), ADDR[0] is ignored and when DATAWIDTH = 10 or 11 (4 bytes), ADDR[1:0] is ignored). Data pins are LSB-oriented and unused WD data pins must be grounded.

Table 2-20 • **Data Width Settings**

DATAWIDTH[1:0]	Data Width
00	1 byte [7:0]
01	2 byte [15:0]
10, 11	4 bytes [31:0]

Flash Memory Block Protection

Page Loss Protection

When the PAGELOSSPROTECT pin is set to logic 1, it prevents writes to any other page except the current page in the Page Buffer, until the page is either discarded or programmed.

A write to another page while the current page is page loss protected will return a STATUS of '11'.

Overwrite Protection

Any page that is overwrite protected will result in the STATUS being set to '01' when an attempt is made to either write, program, or erase it. To set the Overwrite Protection state for a page, set the OVERWRITEPROTECT pin when a program operation is undertaken. To clear the Overwrite Protect state for a given page, an Unprotect Page operation must be performed on the page, and then the page must be programmed with the OVERWRITEPROTECT pin cleared to save the new page.

LOCKREQUEST

The LOCKREQUEST signal is used to give the user interface control over simultaneous access of the FB from both the User and JTAG interfaces. When LOCKREQUEST is asserted, the JTAG interface will hold off any access attempts until LOCKREQUEST is deasserted.

Flash Memory Block Operations

FB Operation Priority

The FB provides for priority of operations when multiple actions are requested simultaneously. Table 2-21 shows the priority order (priority 0 is the highest).

Table 2-21 • **FB Operation Priority**

Operation	Priority
System initialization	0
FB reset	1
Read	2
Write	3
Erase page	4
Program	5
Unprotect page	6
Discard page	7

Access to the FB is controlled by the BUSY signal. The BUSY output is synchronous to the CLK signal. FB operations are only accepted in cycles where BUSY is logic 0.

Write Operation

Write operations are initiated with the assertion of the WEN signal. Figure 2-34 on page 2-42 illustrates the multiple write operations.

When a write operation is initiated to a page that is currently not in the Page Buffer, the FB control logic will issue a BUSY signal to the user interface while the page is loaded from the FB Array into the Page Buffer. (Note: The number of clock cycles that the BUSY output is asserted during the load of the Page Buffer is variable.) After loading the page to the Page Buffer, the addressed data block is loaded from the Page Buffer into the Block Buffer. Subsequent writes to the same block of the page will incur no busy cycles. A write to another block in the page will assert BUSY for four cycles (five cycles when PIPE is asserted), to allow the data to be written to the Page Buffer and have the current block loaded into the Block Buffer.

Write operations are considered successful as long as the STATUS output is '00'. A non-zero STATUS indicates an error was detected during the operation and the write was not performed. Note that the STATUS output is "sticky;" it is unchanged until another operation is started.

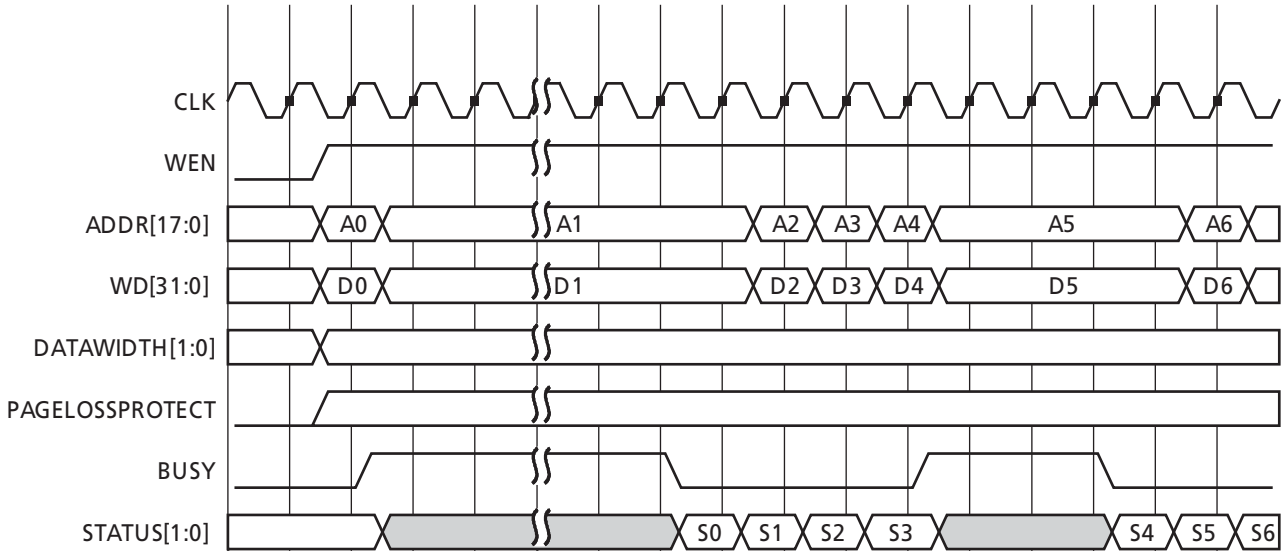


Figure 2-34 • **FB Write Waveform**

Only one word can be written at a time. Write word width is controlled by the DATAWIDTH bus. Users are responsible for keeping track of the contents of the Page Buffer and when to program it to the array. Just like a regular RAM, writing to random addresses is possible. Users can write into the Page Buffer in any order, but will incur additional BUSY cycles. It is not necessary to modify the entire Page Buffer before saving it to nonvolatile memory.

Write errors include the following:

1. Attempting to write a page that is Overwrite Protected (STATUS = 01). The write is not performed.
2. Attempting to write to a page that is not in the Page Buffer when Page Loss Protection is enabled (STATUS = 11). The write is not performed.

Program Operation

A program operation is initiated by asserting the PROGRAM signal on the interface. Program operations save the contents of the Page Buffer to the FB Array. Due to the technologies inherent in the FB, a program operation is a time consuming operation (~8 ms). While the FB is writing the data to the array, the BUSY signal will be asserted.

During a Program operation, the sector and page addresses on ADDR are compared with the stored address for the page (and sector) in the Page Buffer. If there is a mismatch between the two addresses, the program operation will be aborted and an error will be reported on the STATUS output.

It is possible to write the Page Buffer to a different page in memory. When asserting the PROGRAM pin, if OVERWRITEPAGE is asserted as well, the FB will write the contents of the Page Buffer to the sector and page designated on the ADDR inputs, if the destination page is not overwrite protected.

A program operation may be utilized to either modify the contents of the page in the Flash memory block or change the protections for the page. Setting the OVERWRITEPROTECT bit on the interface while asserting the PROGRAM pin will put the page addressed into Overwrite Protect Mode. Overwrite Protect Mode safeguards a page from being inadvertently overwritten during subsequent program or erase operations.

Program operations that result in a STATUS value of '01' do not modify the addressed page. For all other values of STATUS, the addressed page is modified.

Program errors include the following:

1. Attempting to program a page that is Overwrite Protected (STATUS = 01)
2. Attempting to program to a page that is not in the Page Buffer when the Page Buffer has entered Page Loss Protection mode (STATUS = 01)
3. Attempting to perform a program with OVERWRITEPAGE set when the page addressed has been Overwrite Protected (STATUS = 01)
4. The Write Count of the page programmed exceeding the Write Threshold defined in the part specification (STATUS = 11)
5. The ECC Logic determining that there is an uncorrectable error within the programmed page (STATUS = 10)
6. Attempting to program to a page that is **not** in the Page Buffer when OVERWRITEPAGE is not set and the page in the Page Buffer is modified (STATUS = 01)
7. Attempting to program the page that is in the Page Buffer when the Page Buffer is **not** modified.

The waveform for a program operation is shown in Figure 2-35.

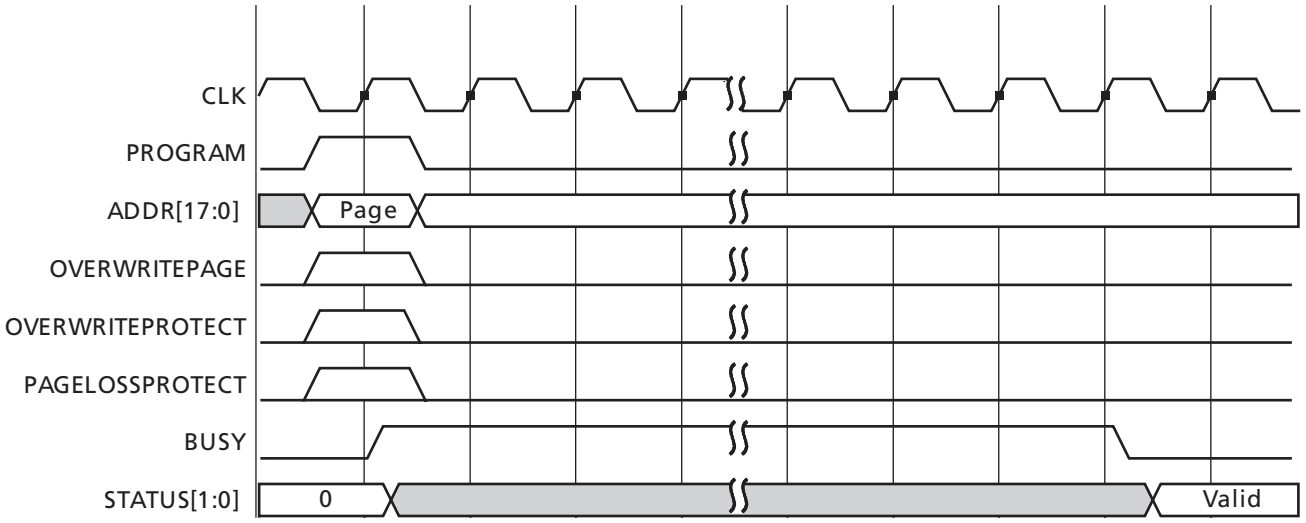


Figure 2-35 • **FB Program Waveform**

Note: OVERWRITEPAGE is only sampled when the PROGRAM or ERASEPAGE pins are asserted. OVERWRITEPAGE is ignored in all other operations.

Erase Page Operation

The Erase Page operation is initiated when the ERASEPAGE pin is asserted. The Erase Page operation allows the user to erase (set user data to '0') any page within the FB.

The use of the OVERWRITEPAGE and PAGELOSSPROTECT pins is the same for erase as for a Program Page operation.

As with the Program Page operation, a STATUS of '01' indicates that the addressed page is not erased.

A waveform for an Erase Page operation is shown in Figure 2-36.

Erase errors include the following:

1. Attempting to erase a page that is Overwrite Protected (STATUS = 01)
2. Attempting to erase a page that is not in the Page Buffer when the Page Buffer has entered Page Loss Protection mode (STATUS = 01)
3. The Write Count of the erased page exceeding the Write Threshold defined in the part specification (STATUS = 11)
4. The ECC Logic determining that there is an uncorrectable error within the erased page (STATUS = 10)

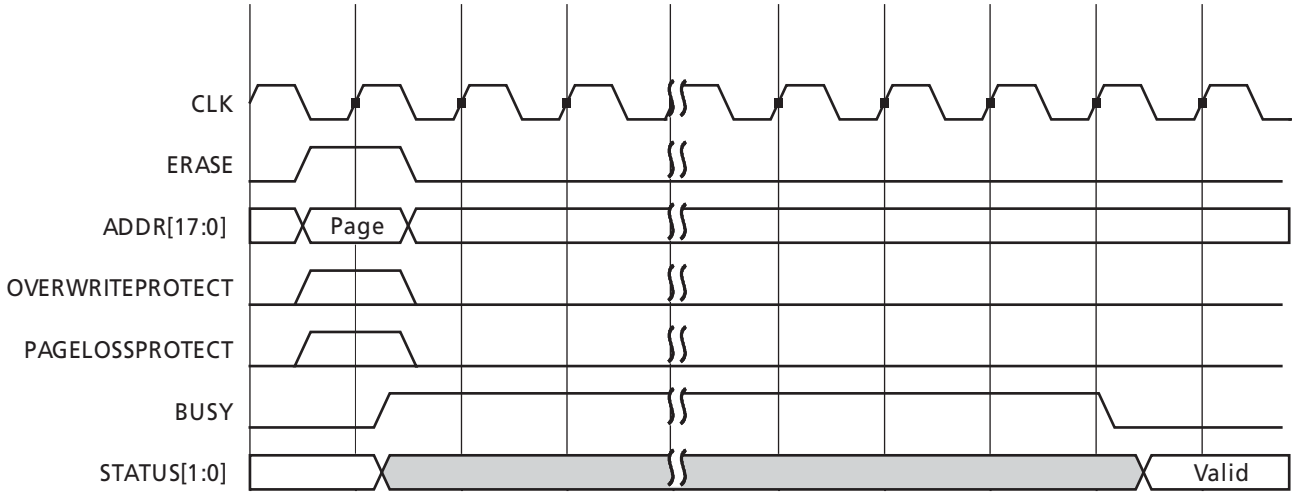


Figure 2-36 • **FB Erase Page Waveform**

Read Operation

Read operations are designed to read data from the FB Array, Page Buffer, Block Buffer or status registers. Read operations support a normal read and a read-ahead mode (done by asserting READNEXT). Also, the timing for Read operations is dependent on the setting of PIPE.

The following diagrams illustrate representative timing for Non-Pipe Mode (Figure 2-37) and Pipe Mode (Figure 2-38) reads of the Flash memory block interface.

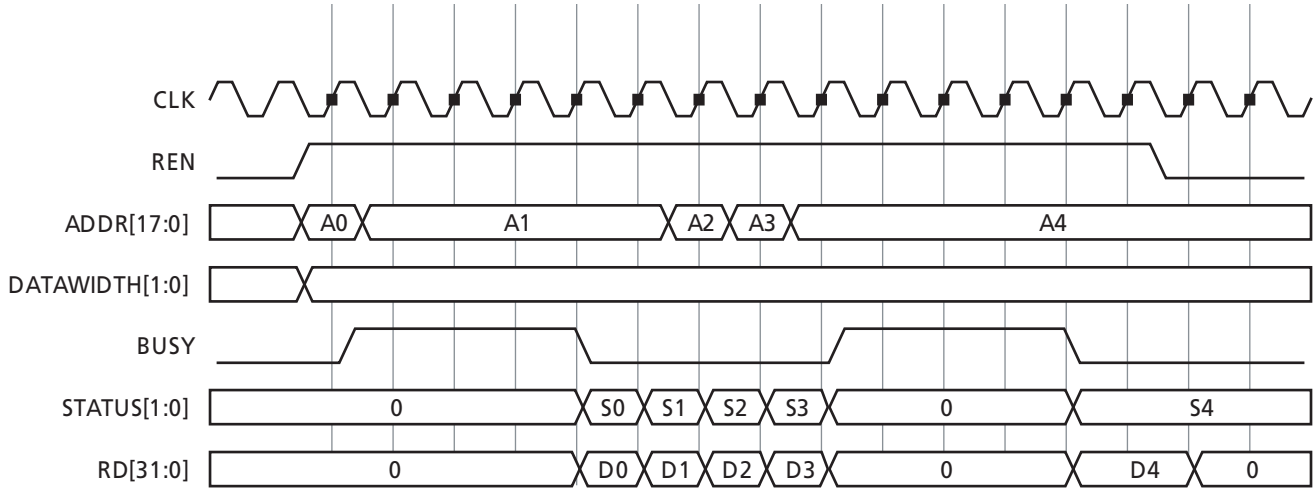


Figure 2-37 • **Read Waveform (Non-Pipe Mode, 32-Bit Access)**

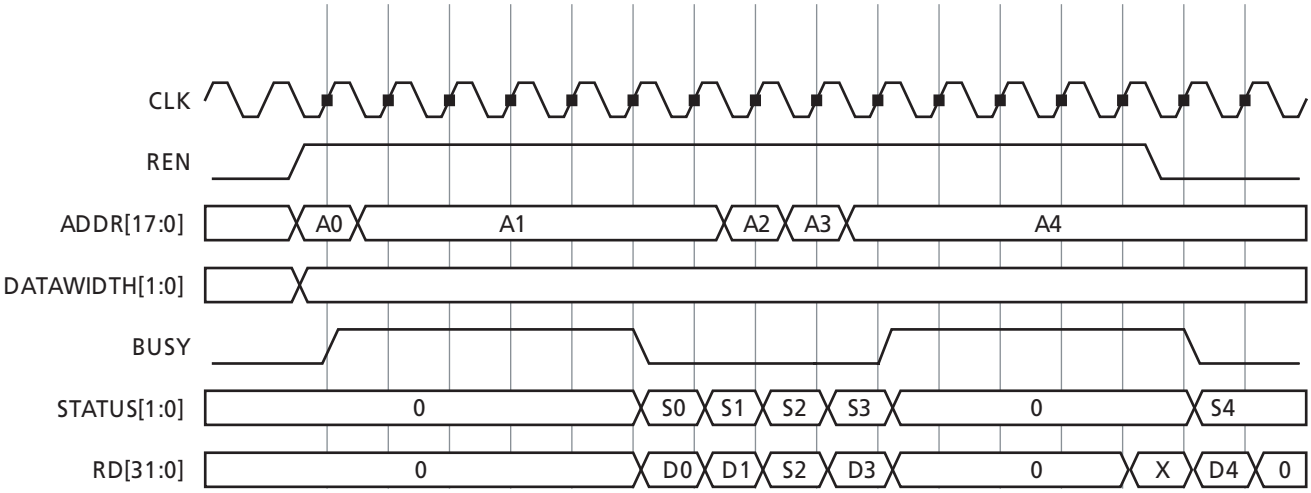


Figure 2-38 • **Read Waveform (Pipe Mode, 32-Bit Access)**

The following error indications are possible for Read operations:

1. STATUS = 01 when a single-bit data error was detected and corrected within the block addressed.
2. STATUS = 10 when a double-bit error was detected in the block addressed (note that the error is uncorrected).

In addition to data reads, users can read the status of any page in the FB by asserting PAGESTATUS along with REN. The format of the data returned by a page status read is shown in Table 2-22, and the definition of the page status bits is shown in Table 2-23.

Table 2-22 • **Page Status Read Data Format**

31	8	7	4	3	2	1	0
Write Count		Reserved		Over Threshold	Read Protected	Write Protected	Overwrite Protected

Table 2-23 • **Page Status Bit Definition**

Page Status Bits	Bit Definition
31–8	The number of times the page addressed has been programmed/erased
7–4	Reserved; read as 0
3	Over threshold indicator (see the "Program Operation" section on page 2-42)
2	Read protected; read protect bit for page which is set via the JTAG interface
1	Write protected; write protect bit for page which is set via the JTAG interface
0	Overwrite protected; designates that the user has set the OVERWRITEPROTECT bit on the interface while doing a program operation. The page cannot be written without first performing an Unprotect Page operation.

Read Next Operation

The Read Next operation is a feature by which the next block relative to the block in the Block Buffer is read from the FB Array while performing reads from the Block Buffer. The goal is to minimize wait states during consecutive sequential read operations.

The Read Next operation is performed in a predetermined manner because it does look-ahead reads. The general look-ahead function is as follows:

- Within a page, the next block fetched will be the next in the linear address.
- When reading the last data block of a page, it will fetch the first block of the next page.
- When reading spare pages, it will read the first block of the next sector's spare page.
- Reads of the last sector will wrap around to sector 0.
- Reads of Auxiliary blocks will read the next linear page's Auxiliary block.

When an address on the ADDR input does not agree with the predetermined look-ahead address, there is a time penalty for this access. The FB will be busy finishing the current look-ahead read before it can start the next read. The worst case is a total of nine BUSY cycles before data is delivered.

The Non-Pipe Mode and Pipe Mode waveforms for Read Next operations are illustrated in Figure 2-39 and Figure 2-40.

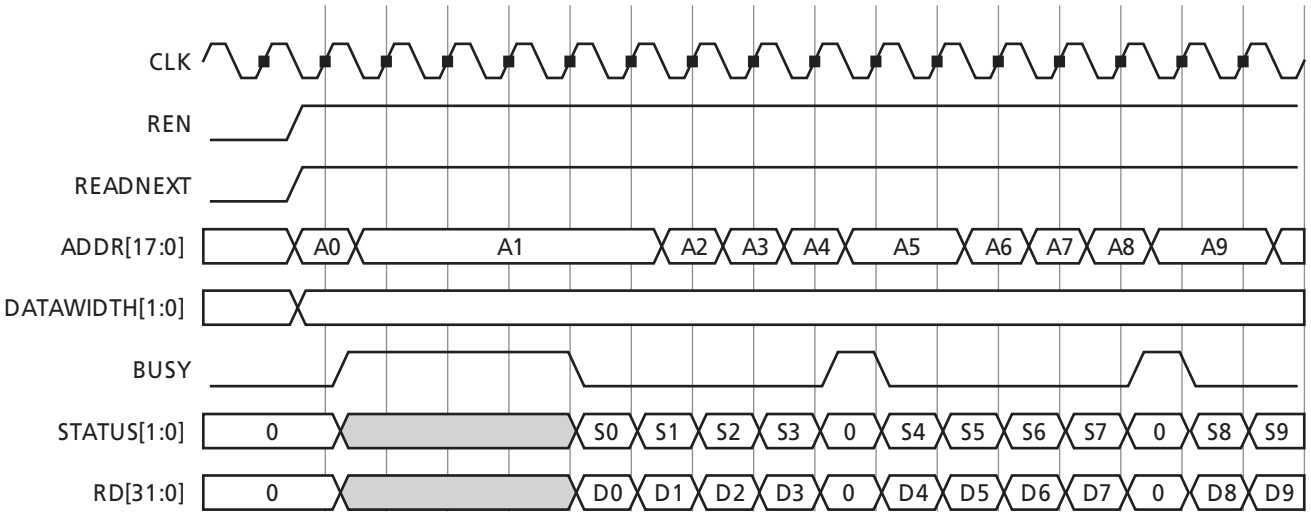


Figure 2-39 • **Read Next Waveform (Non-Pipe Mode, 32-Bit Access)**

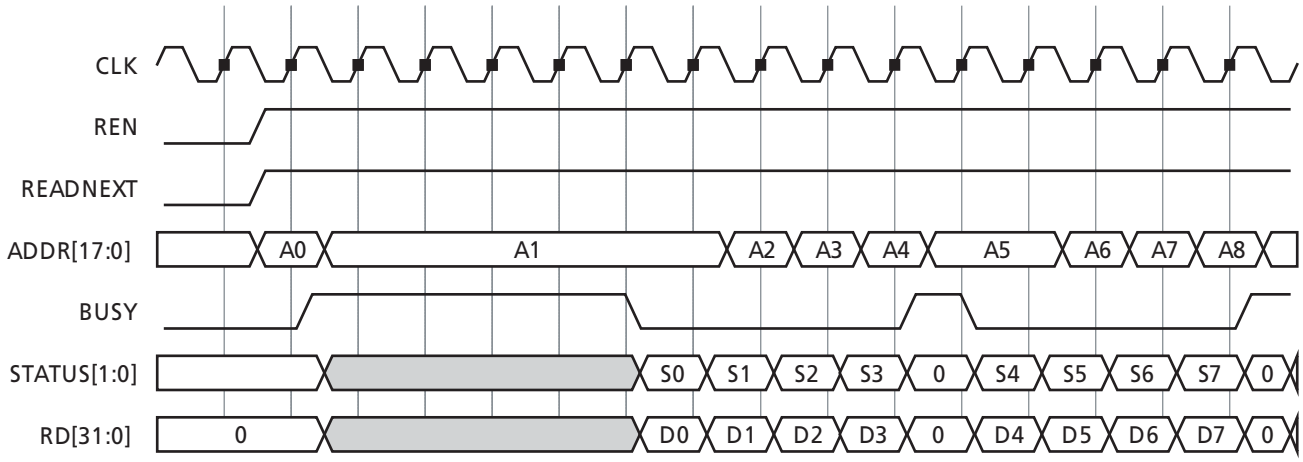


Figure 2-40 • **Read Next WaveForm (Pipe Mode, 32-Bit Access)**

Unprotect Page Operation

An Unprotect Page operation will clear the protection for a page addressed on the ADDR input. It is initiated by setting the UNPROTECTPAGE signal on the interface along with the page address on ADDR.

If the page is not in the Page Buffer, the Unprotect Page operation will copy the page into the Page Buffer. The copy page operation occurs only if the current page in the Page Buffer is not Page Loss Protected.

The waveform for an Unprotect Page operation is shown in Figure 2-41.

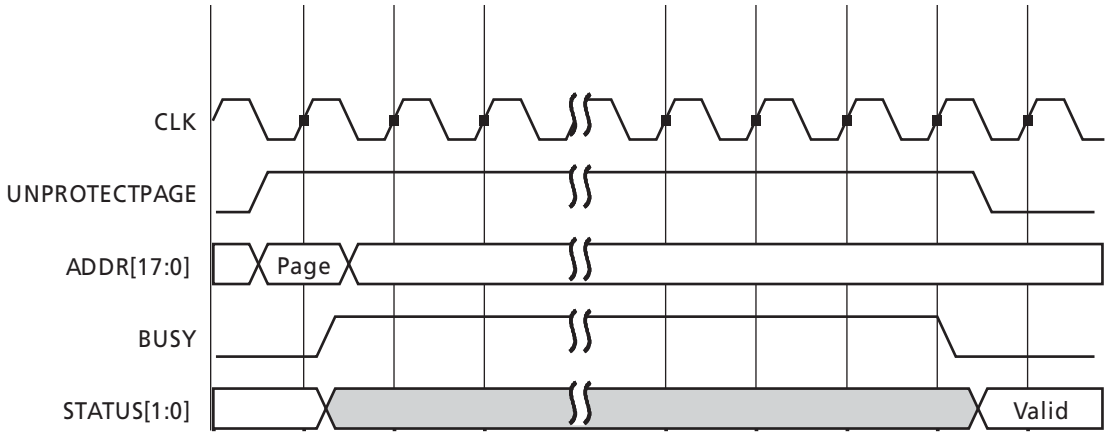


Figure 2-41 • **FB Unprotected Page Waveform**

The Unprotect Page operation can incur the following error conditions:

1. If the copy of the page to the Page Buffer determines that the page has a single-bit correctable error in the data, it will report a STATUS = 01.
2. If the address on ADDR does not match the address of the Page Buffer, PAGELOSSPROTECT is asserted, and the Page Buffer has been modified, then the STATUS = 11 and the addressed page is not loaded into the Page Buffer.
3. If the copy of the page to the Page Buffer determines that at least one block in the page has a double-bit uncorrectable error, then STATUS = 10 and the Page Buffer will contain the corrupted data.

Discard Page Operation

If the contents of the modified Page Buffer have to be discarded, the DISCARDPAGE signal should be asserted. This command results in the Page Buffer being marked as unmodified.

The timing for the operation is shown in Figure 2-42. The BUSY signal will remain asserted until the operation has completed.

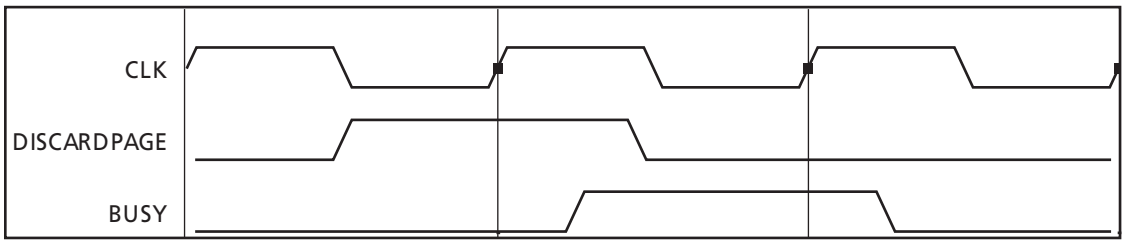


Figure 2-42 • **FB Discard Page Waveform**

Flash Memory Block Characteristics

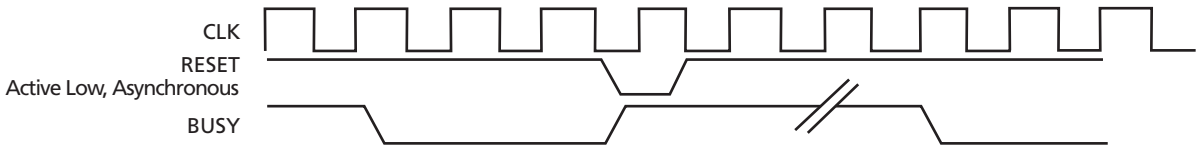


Figure 2-43 • **Reset Timing Diagram**

Table 2-24 • **Flash Memory Block Timing**
Commercial-Case Conditions: T_J = 25°C, Typical Case, V_{CC} = 1.5 V

Parameter	Description	Min.	Typ.	Max.	Units
$t_{CLKQ5CYC}$	Clock-to-Q in 5-cycle read mode of the Control Logic		7.5		ns
$t_{CLKQ6CYC}$	Clock-to-Q in 6-cycle read mode of the Control Logic		2.3		ns
t_{DSUNVM}	Data Input Setup time for the Control Logic	1.5			ns
t_{DHNVM}	Data Input Hold time for the Control Logic	0			ns
t_{ASUNVM}	Address Input Setup time for the Control Logic	4.9			ns
t_{AHNVM}	Address Input Hold time for the Control Logic	0			ns
$t_{MPWARNVM}$	Asynchronous Reset Minimum Pulse Width for the Control Logic	10			ns
$t_{MPWCLKNVM}$	Clock Minimum Pulse Width for the Control Logic	5			ns

FlashROM

Fusion devices have 1 kbit of on-chip nonvolatile Flash memory that can be read from the FPGA core fabric. The FlashROM is arranged in 8 banks of 128 bits during programming. The 128 bits in each bank are addressable as 16 bytes during the read back of the FlashROM from the FPGA core (Figure 2-44).

The FlashROM can only be programmed via the IEEE 1532 JTAG port. It cannot be programmed directly from the FPGA core. When programming, each of the 8 128-bit banks can be selectively reprogrammed. The FlashROM can only be reprogrammed on a bank boundary. Programming involves an automatic, on-chip bank erase prior to reprogramming the bank. The FlashROM supports a synchronous read and can be read on byte boundaries. The upper 3 bits of the FlashROM address from the FPGA core define the bank that is being accessed. The lower 4 bits of the FlashROM address from the FPGA core define which of the 16 bytes in the bank is being accessed.

		Byte Number in Bank 4 LSB of ADDR (READ)															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bank Number 3 MSB of ADDR (READ)	7																
	6																
	5																
	4																
	3																
	2																
	1																
	0																

Figure 2-44 • **FlashROM Architecture**

FlashROM Characteristics

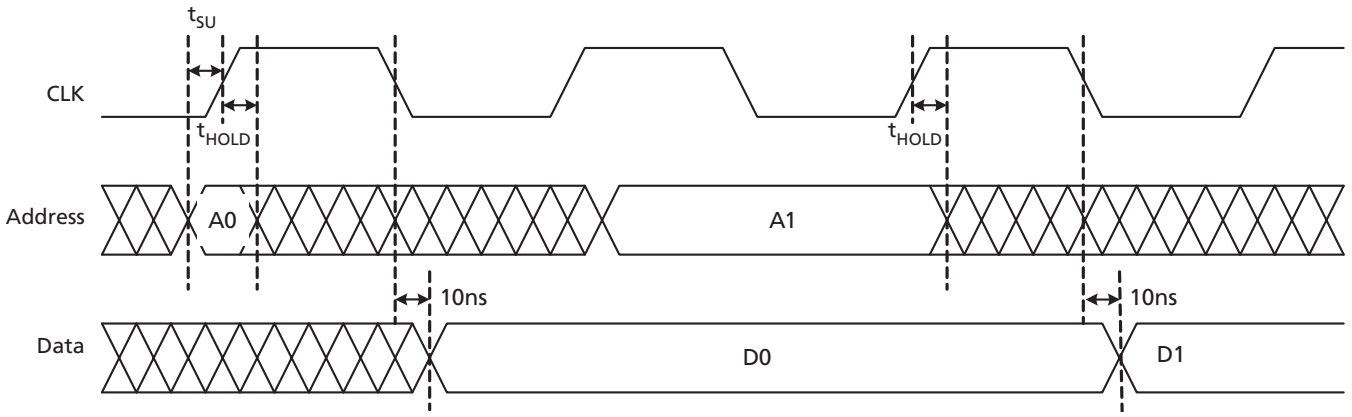


Figure 2-45 • **FlashROM Timing Diagram**

SRAM and FIFO

All Fusion devices have SRAM blocks along the north side of the device. Additionally, AFS600 and AFS1500 devices have an SRAM block on the south side of the device. To meet the needs of high-performance designs, the memory blocks operate strictly in synchronous mode for both read and write operations. The read and write clocks are completely independent, and each may operate at any desired frequency less than or equal to 350 MHz.

- 4k×1, 2k×2, 1k×4, 512×9 (dual-port RAM—two read, two write or one read, one write)
- 512×9, 256×18 (two-port RAM—one read and one write)
- Sync write, sync pipelined/nonpipelined read

The Fusion SRAM memory block includes dedicated FIFO control logic to generate internal addresses and external flag logic (Full, Empty, AFULL, AEMPTY).

During RAM operation, addresses are sourced by the user logic and the FIFO controller is ignored. In FIFO mode, the internal addresses are generated by the FIFO controller and routed to the RAM array by internal MUXes. Refer to Figure 2-46 for more information about the implementation of the embedded FIFO controller.

The Fusion architecture enables the read and write sizes of RAMs to be organized independently, allowing for bus conversion. This is done with the WW (write width) and RW (read width) pins. The different D×W configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1. For example, the write size can be set to 256×18 and the read size to 512×9.

Both the write and read widths for the RAM blocks can be specified independently with the WW (write width) and RW (read width) pins. The different DxW configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1.

Refer to the allowable RW and WW values supported for each of the RAM macro types in Table 2-25 on page 2-53.

When widths of one, two, or four are selected, the ninth bit is unused. For example, when writing nine-bit values and reading four-bit values, only the first four bits and the second four bits of each nine-bit value are addressable for read operations. The ninth bit is not accessible.

Conversely, when writing four-bit values and reading nine-bit values, the ninth bit of a read operation will be undefined. The RAM blocks employ Little Endian byte order for read and write operations.

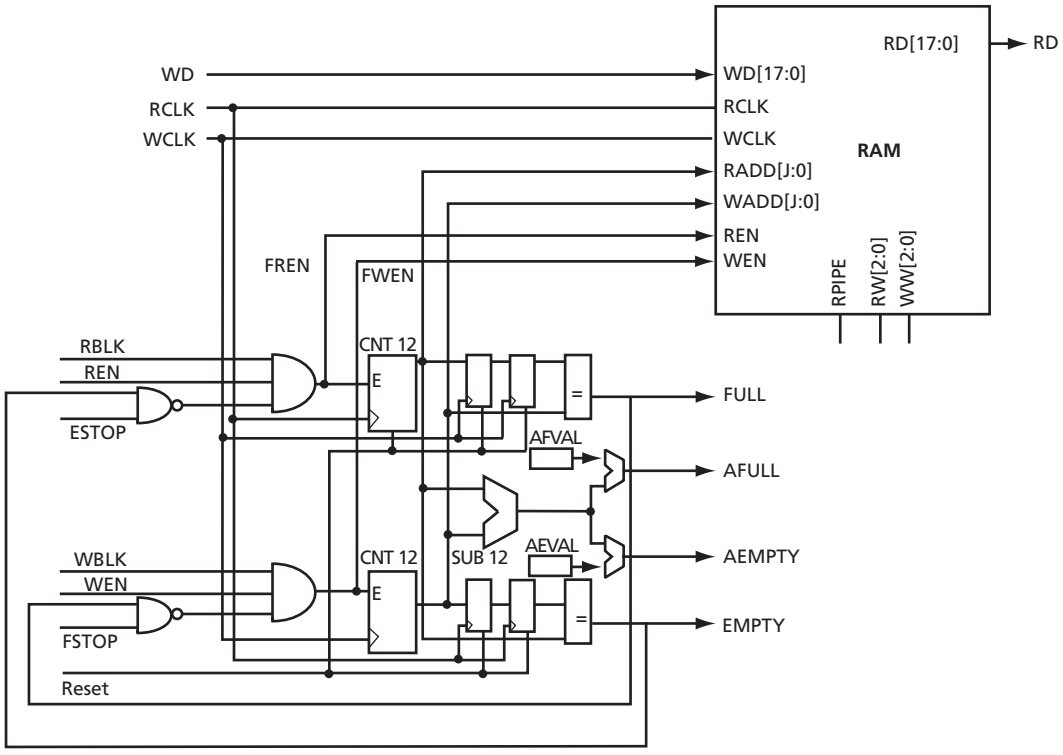


Figure 2-46 • **Fusion RAM Block with Embedded FIFO Controller**

RAM4K9 Description

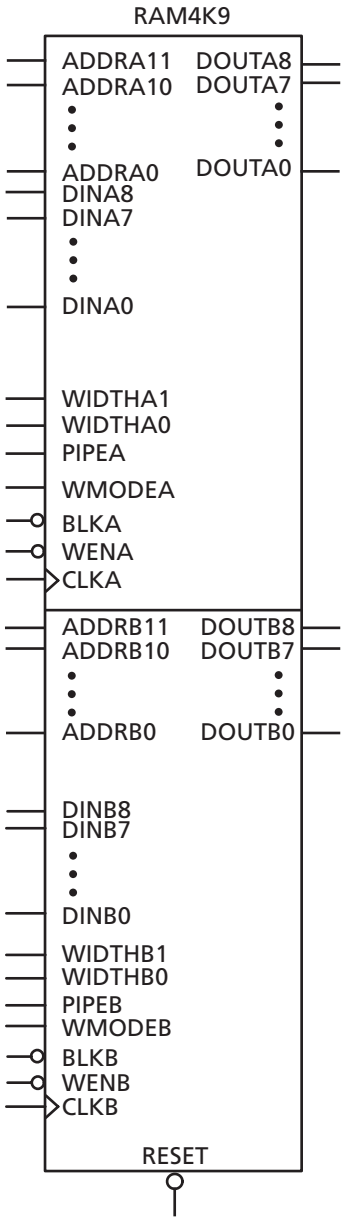


Figure 2-47 • **RAM4K9**

The following signals are used to configure the RAM4K9 memory element:

WIDTHA and WIDTHB

These signals enable the RAM to be configured in one of four allowable aspect ratios (Table 2-25).

Table 2-25 • **Allowable Aspect Ratio Settings for WIDTHA[1:0]**

WIDTHA1, WIDTHA0	WIDTHB1, WIDTHB0	D×W
00	00	4k×1
01	01	2k×2
10	10	1k×4
11	11	512×9

Note: *The aspect ratio settings are constant and cannot be changed on the fly.*

BLKA and BLKB

These signals are active low and will enable the respective ports when asserted. When a BLKx signal is deasserted, the corresponding port's outputs hold the previous value.

WENA and WENB

These signals switch the RAM between read and write modes for the respective ports. A low on these signals indicates a write operation, and a high indicates a read.

CLKA and CLKB

These are the clock signals for the synchronous read and write operations. These can be driven independently or with the same driver.

PIPEA and PIPEB

These signals are used to specify pipelined read on the output. A low on PIPEA or PIPEB indicates a nonpipelined read and the data appears on the corresponding output in the same clock cycle. A high indicates a pipelined read and data appears on the corresponding output in the next clock cycle.

WMODEA and WMODEB

These signals are used to configure the behavior of the output when RAM is in write mode. A low on these signals makes the output retain data from the previous read. A high indicates pass-through behavior, wherein the data being written will appear immediately on the output. This signal is overridden when the RAM is being read.

RESET

This active low signal resets the output to zero when asserted. It does not reset the contents of the memory.

ADDRA and ADDRB

These are used as read or write addresses, and they are 12 bits wide. When a depth of less than 4 k is specified, the unused high-order bits must be grounded (Table 2-26).

Table 2-26 • **Address Pins Unused/Used for Various Supported Bus Widths**

	ADDRx	
DxW	**Unused**	**Used**
4k×1	None	[11:0]
2k×2	[11]	[10:0]
1k×4	[11:10]	[9:0]
512×9	[11:9]	[8:0]

Note: *The "x" in ADDRx implies A or B.*

DINA and DINB

These are the input data signals, and they are nine bits wide. Not all nine bits are valid in all configurations. When a data width less than nine is specified, unused high-order signals must be grounded (Table 2-27).

DOUTA and DOUTB

These are the nine-bit output data signals. Not all nine bits are valid in all configurations. As with DINA and DINB, high-order bits may not be used (Table 2-27). The output data on unused pins is undefined.

Table 2-27 • **Unused/Used Input and Output Data Pins for Various Supported Bus Widths**

	DINx/DOUTx	
DxW	**Unused**	**Used**
4k×1	[8:1]	[0]
2k×2	[8:2]	[1:0]
1k×4	[8:4]	[3:0]
512×9	None	[8:0]

Note: *The "x" in DINx and DOUTx implies A or B.*

RAM512X18 Description

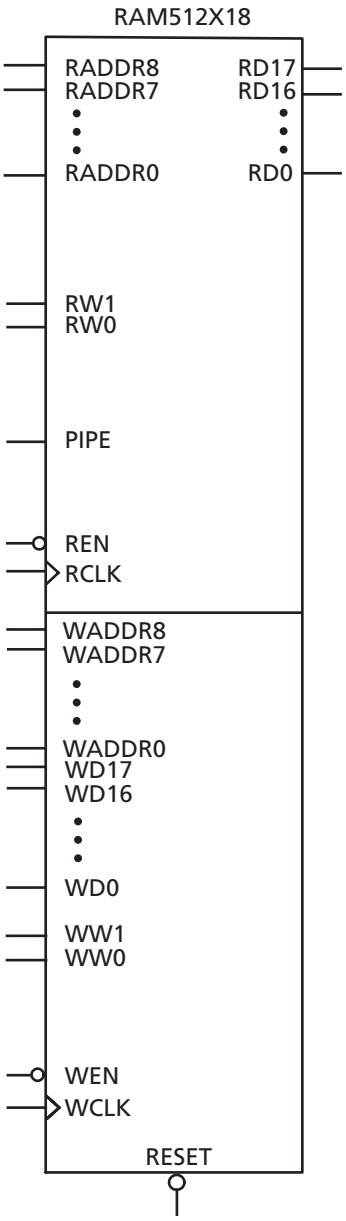


Figure 2-48 • **RAM512X18**

RAM512X18 exhibits slightly different behavior from the RAM4K9, as it has dedicated read and write ports.

WW and RW

These signals enable the RAM to be configured in one of the two allowable aspect ratios (Table 2-28).

Table 2-28 • **Aspect Ratio Settings for WW[1:0]**

WW[1:0]	RW[1:0]	D×W
01	01	512×9
10	10	256×18
00, 11	00, 11	Reserved

WD and RD

These are the input and output data signals, and they are 18 bits wide. When a 512×9 aspect ratio is used for write, WD[17:9] are unused and must be grounded. If this aspect ratio is used for read, then RD[17:9] are undefined.

WADDR and RADDR

These are read and write addresses, and they are nine bits wide. When the 256×18 aspect ratio is used for write or read, WADDR[8] or RADDR[8] are unused and must be grounded.

WCLK and RCLK

These signals are the write and read clocks, respectively. They are both active high.

WEN and REN

These signals are the write and read enables, respectively. They are both active low by default. These signals can be configured as active high.

RESET

This active low signal resets the output to zero when asserted. It does not reset the contents of the memory.

PIPE

This signal is used to specify pipelined read on the output. A low on PIPE indicates a nonpipelined read and the data appears on the output in the same clock cycle. A high indicates a pipelined read and data appears on the output in the next clock cycle.

Clocking

The dual-port SRAM blocks are only clocked on the rising edge. SmartGen allows falling-edge triggered clocks by adding inverters to the netlist, hence achieving dual-port SRAM blocks that are clocked on either edge (rising or falling). For dual-port SRAM, each port can be clocked on either edge or by separate clocks, by port.

Fusion devices support inversion (bubble pushing) throughout the FPGA architecture, including the clock input to the SRAM modules. Inversions added to the SRAM clock pin on the design schematic or in the HDL code will be automatically accounted for during design compile without incurring additional delay in the clock path.

The two-port SRAM can be clocked on the rising edge or falling edge of WCLK and RCLK.

If negative-edge RAM and FIFO clocking is selected for memory macros, clock edge inversion management (bubble pushing) is automatically used within the Fusion development tools, without performance penalty.

Modes of Operation

There are two read modes and one write mode:

- Read Nonpipelined (synchronous—one clock edge): In the standard read mode, new data is driven onto the RD bus in the same clock cycle following RA and REN valid. The read address is registered on the read port clock active edge and data appears at RD after the RAM access time. Setting PIPE to OFF enables this mode.
- Read Pipelined (synchronous—two clock edges): The pipelined mode incurs an additional clock delay from the address to the data but enables operation at a much higher frequency. The read address is registered on the read port active clock edge, and the read data is registered and appears at RD after the second read clock edge. Setting PIPE to ON enables this mode.
- Write (synchronous—one clock edge): On the write clock active edge, the write data is written into the SRAM at the write address when WEN is high. The setup times of the write address, write enables, and write data are minimal with respect to the write clock. Write and read transfers are described with timing requirements in the "SRAM Characteristics" section on page 2-56 and "FIFO Characteristics" section on page 2-63.

RAM Initialization

Each SRAM block can be individually initialized on power-up by means of the JTAG port using the UJTAG mechanism (refer to the "JTAG IEEE 1532" section on page 2-170 and the *Fusion SRAM/FIFO Blocks* application note). The shift register for a target block can be selected and loaded with the proper bit configuration to enable serial loading. The 4,608 bits of data can be loaded in a single operation.

SRAM Characteristics
Timing Waveforms

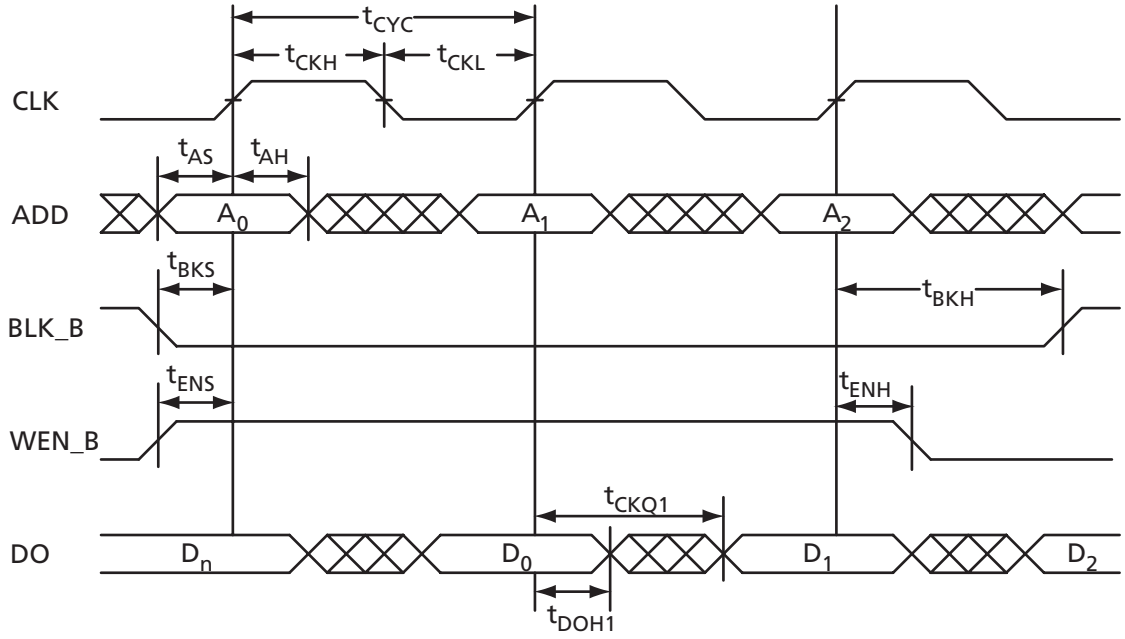


Figure 2-49 • **RAM Read for Flow-Through Output**

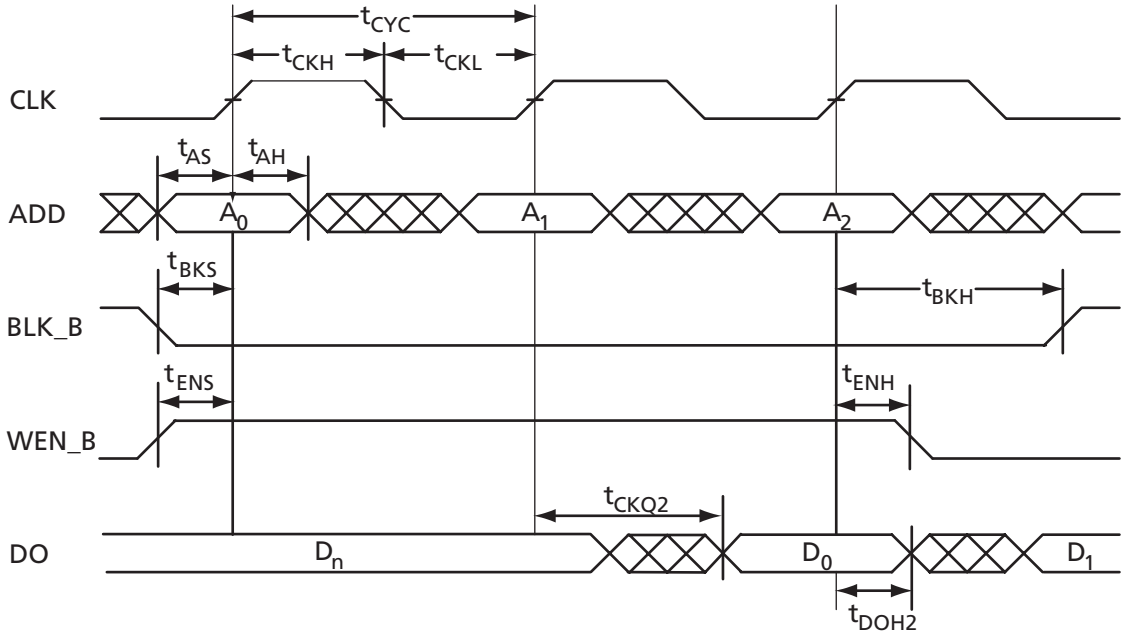


Figure 2-50 • **RAM Read for Pipelined Output**

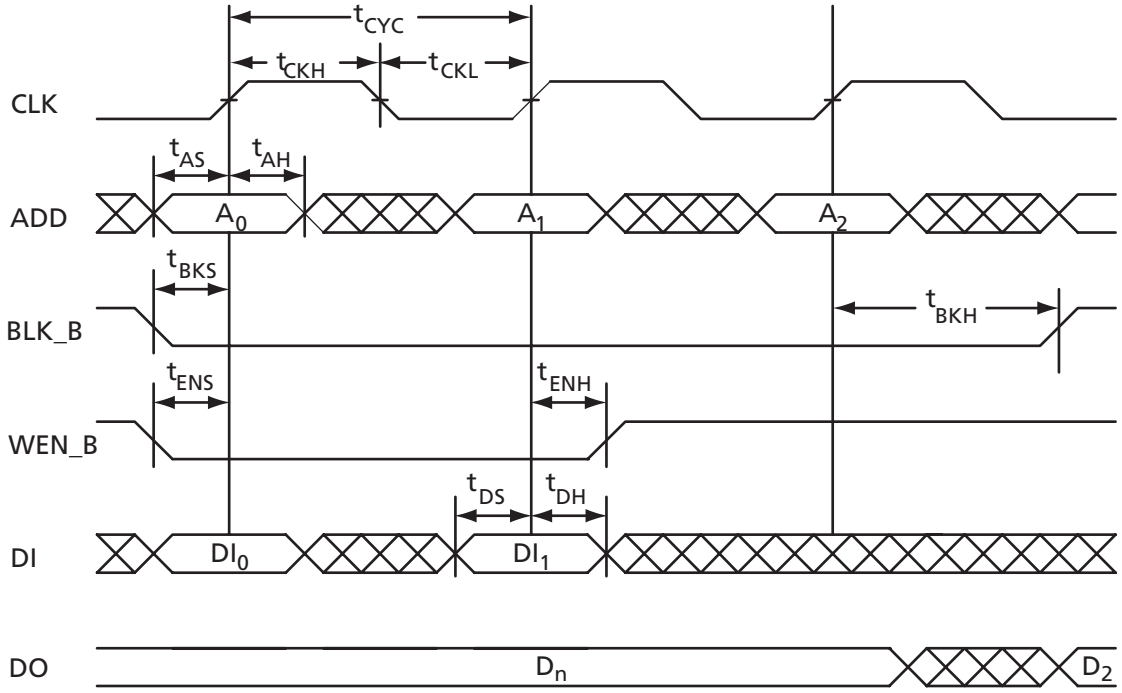


Figure 2-51 • **RAM Write, Output Retained (WMODE = 0)**

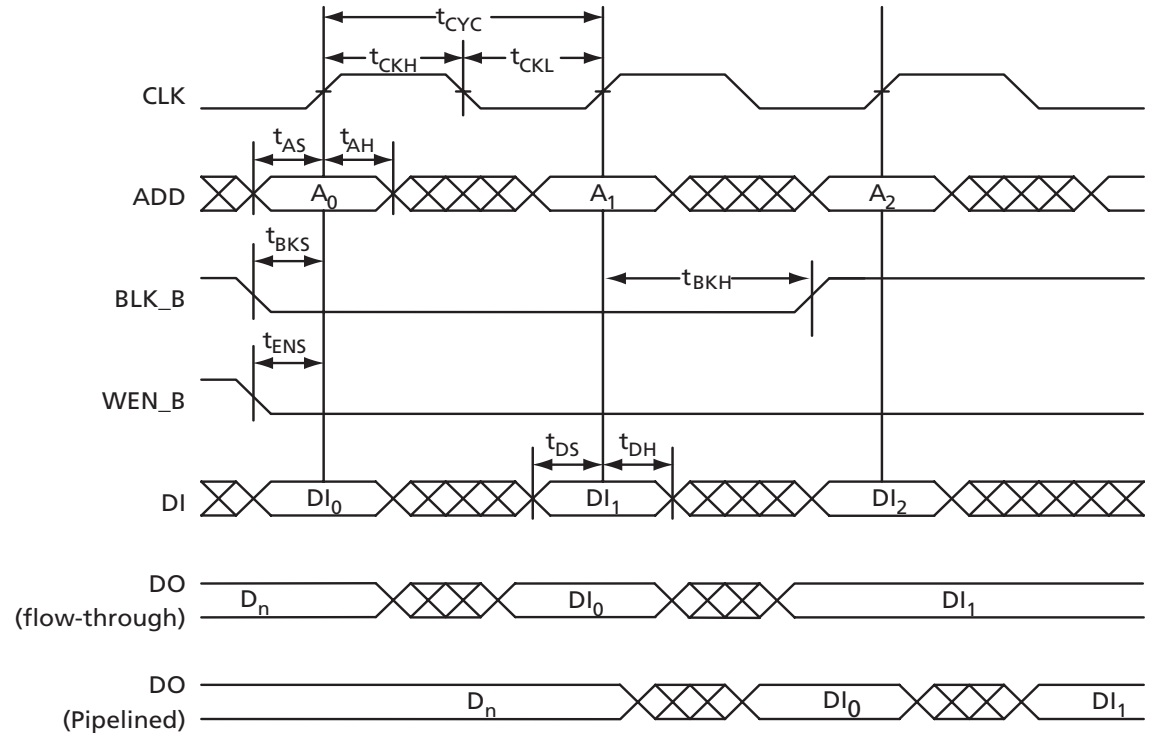


Figure 2-52 • **RAM Write, Output as Write Data (WMODE = 1)**

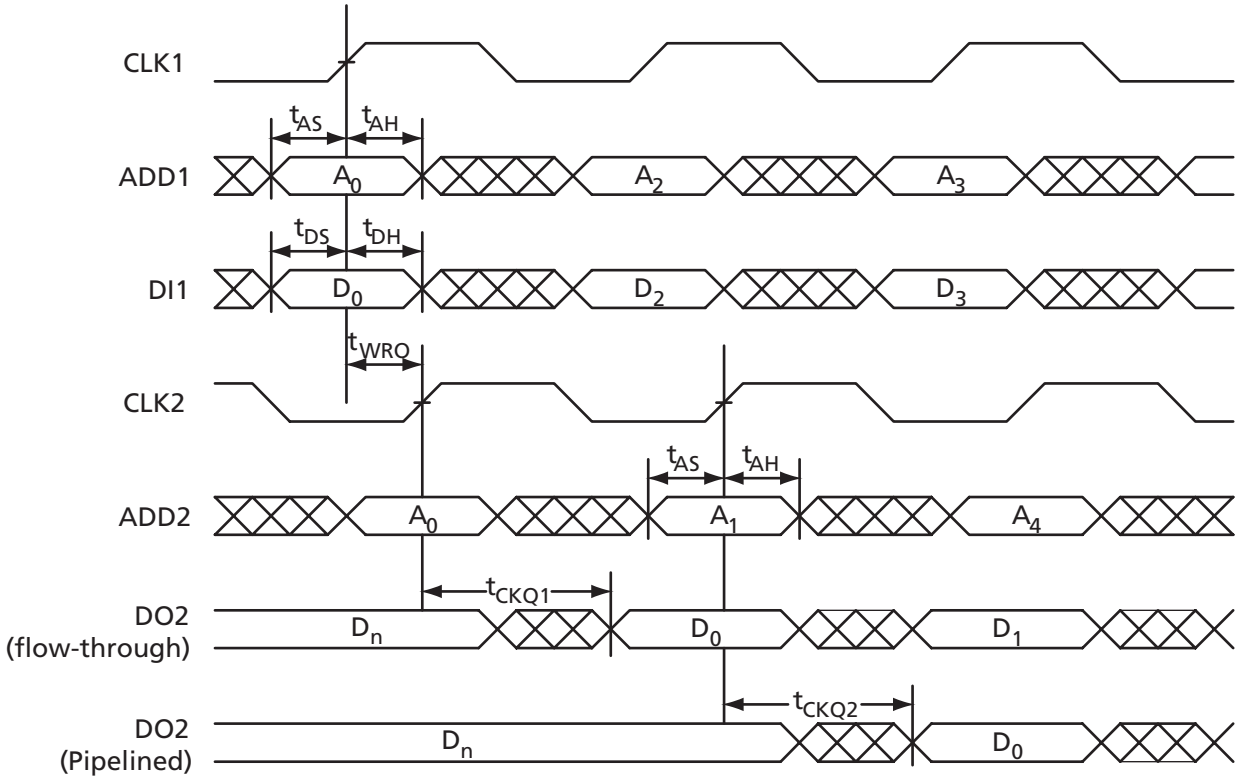


Figure 2-53 • **One Port Write/Other Port Read Same**

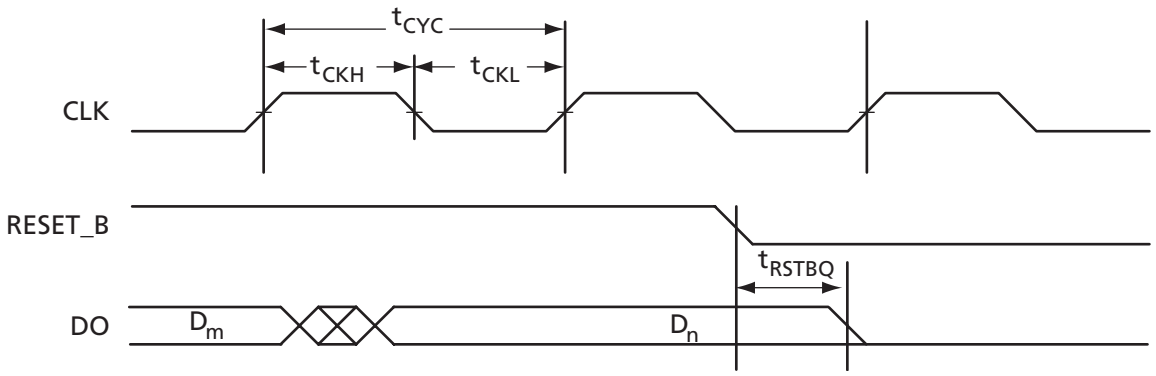


Figure 2-54 • **RAM Reset**

Timing Characteristics

Table 2-29 • **RAM4K9**
Commercial Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{AS}	Address Setup time	0.25	0.28	0.33	ns
t_{AH}	Address Hold time	0.00	0.00	0.00	ns
t_{ENS}	REN_B,WEN_B Setup time	0.14	0.16	0.19	ns
t_{ENH}	REN_B, WEN_B Hold time	0.10	0.11	0.13	ns
t_{BKS}	BLK_B Setup time	0.23	0.27	0.31	ns
t_{BKH}	BLK_B Hold time	0.02	0.02	0.02	ns
t_{DS}	Input data (DI) Setup time	0.18	0.21	0.25	ns
t_{DH}	Input data (DI) Hold time	0.00	0.00	0.00	ns
t_{CKQ1}	Clock High to New Data Valid on DO (output retained, WMODE = 0)	1.79	2.03	2.39	ns
	Clock High to New Data Valid on DO (flow-through, WMODE = 1)	2.36	2.68	3.15	ns
t_{CKQ2}	Clock HIGH to New Data Valid on DO (pipelined)	0.89	1.02	1.20	ns
t_{RSTBQ}	RESET_B Low to Data Out Low on DO (flow through)	0.92	1.05	1.23	ns
	RESET_B Low to Data Out Low on DO (pipelined)	0.92	1.05	1.23	ns
$t_{REMRSTB}$	RESET_B Removal	0.25	0.28	0.33	ns
$t_{RECRSTB}$	RESET_B Recovery	1.49	1.68	1.98	ns
$t_{MPWRSTB}$	RESET_B Minimum Pulse Width	0.22	0.25	0.29	ns
t_{CYC}	Clock Cycle time	1.99	2.26	2.66	ns

Note: *For the derating values at specific junction-temperature and voltage-supply levels, refer to Table 3-6 on page 3-6.*

Table 2-30 • **RAM512X18**
Commercial Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{AS}	Address Setup time	0.25	0.28	0.33	ns
t_{AH}	Address Hold time	0.00	0.00	0.00	ns
t_{ENS}	REN_B,WEN_B Setup time	0.18	0.20	0.24	ns
t_{ENH}	REB_B, WEN_B Hold time	0.06	0.07	0.08	ns
t_{DS}	Input data (DI) Setup time	0.18	0.21	0.25	ns
t_{DH}	Input data (DI) Hold time	0.00	0.00	0.00	ns
t_{CKQ1}	Clock High to New Data Valid on DO (output retained, WMODE = 0)	2.16	2.46	2.89	ns
t_{CKQ2}	Clock High to New Data Valid on DO (pipelined)	0.90	1.02	1.20	ns
t_{RSTBQ}	RESET_B Low to Data Out Low on DO (flow through)	0.92	1.05	1.23	ns
	RESET_B Low to Data Out Low on DO (pipelined)	0.92	1.05	1.23	ns
$t_{REMRSTB}$	RESET_B Removal	0.25	0.28	0.33	ns
$t_{RECRSTB}$	RESET_B Recovery	1.49	1.68	1.98	ns
$t_{MPWRSTB}$	RESET_B Minimum Pulse Width	0.22	0.25	0.29	ns
t_{CYC}	Clock Cycle time	1.99	2.26	2.66	ns

Note: *For the derating values at specific junction-temperature and voltage-supply levels, refer to Table 3-6 on page 3-6.*

FIFO4K18 Description

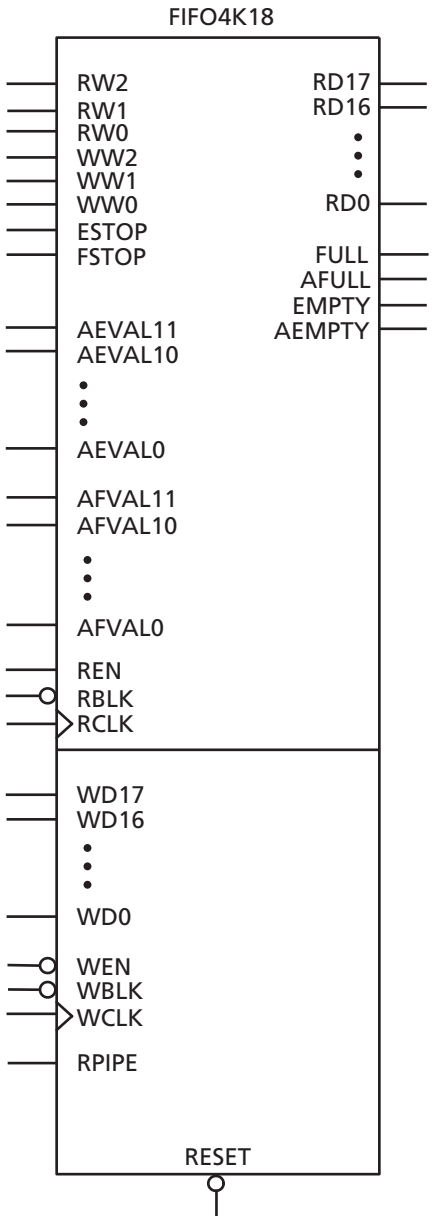


Figure 2-55 • **FIFO4KX18**

The following signals are used to configure the FIFO4K18 memory element:

WW and RW

These signals enable the FIFO to be configured in one of the five allowable aspect ratios (Table 2-31).

Table 2-31 • **Aspect Ratio Settings for WW[2:0]**

WW2, WW1, WW0	RW2, RW1, RW0	D×W
000	000	4k×1
001	001	2k×2
010	010	1k×4
011	011	512×9
100	100	256×18
101, 110, 111	101, 110, 111	Reserved

WBLK and RBLK

These signals are active low and will enable the respective ports when low. When the RBLK signal is high, the corresponding port's outputs hold the previous value.

WEN and REN

Read and write enables. WEN is active low and REN is active high by default. These signals can be configured as active high or low.

WCLK and RCLK

These are the clock signals for the synchronous read and write operations. These can be driven independently or with the same driver.

RPIPE

This signal is used to specify pipelined read on the output. A low on RPIPE indicates a nonpipelined read and the data appears on the output in the same clock cycle. A high indicates a pipelined read and data appears on the output in the next clock cycle.

RESET

This active low signal resets the output to zero when asserted. It resets the FIFO counters. It also sets all the RD pins low, the Full and AFULL pins low, and the Empty and AEMPTY pins high (Table 2-32).

Table 2-32 • **Input Data Signal Usage for Different Aspect Ratios**

DxW	WD/RD Unused
4k×1	WD[17:1], RD[17:1]
2k×2	WD[17:2], RD[17:2]
1k×4	WD[17:4], RD[17:4]
512×9	WD[17:9], RD[17:9]
256×18	–

WD

This is the input data bus and is 18 bits wide. Not all 18 bits are valid in all configurations. When a data width less than 18 is specified, unused higher-order signals must be grounded (Table 2-32).

RD

This is the output data bus and is 18 bits wide. Not all 18 bits are valid in all configurations. Like the WD bus, high-order bits become unusable if the data width is less than 18. The output data on unused pins is undefined (Table 2-32).

ESTOP, FSTOP

ESTOP is used to stop the FIFO read counter from further counting once the FIFO is empty (i.e., the Empty flag goes high). A high on this signal inhibits the counting.

FSTOP is used to stop the FIFO write counter from further counting once the FIFO is full (i.e., the Full flag goes high). A high on this signal inhibits the counting.

For more information on these signals, refer to the "ESTOP and FSTOP Usage" section on page 2-62.

FULL, EMPTY

When the FIFO is full and no more data can be written, the Full flag asserts high. The Full flag is synchronous to WCLK to inhibit writing immediately upon detection of a full condition and to prevent overflows. Since the write address is compared to a resynchronized (and thus time-delayed) version of the read address, the Full flag will remain asserted until two WCLK active edges after a read operation eliminates the full condition.

When the FIFO is empty and no more data can be read, the Empty flag asserts high. The Empty flag is synchronous to RCLK to inhibit reading immediately upon detection of an empty condition and to prevent underflows. Since the read address is compared to a resynchronized (and thus time delayed) version of the write address, the Empty flag will remain asserted until two RCLK active edges, after a write operation, removes the empty condition.

For more information on these signals, refer to the "FIFO Flag Usage Considerations" section on page 2-62.

AFULL, AEMPTY

These are programmable flags and will be asserted on the threshold specified by AFVAL and AEVAL, respectively.

When the number of words stored in the FIFO reaches the amount specified by AEVAL while reading, the AEMPTY output will go high. Likewise, when the number of words stored in the FIFO reaches the amount specified by AFVAL while writing, the AFULL output will go high.

AFVAL, AEVAL

The AEVAL and AFVAL pins are used to specify the almost-empty and almost-full threshold values, respectively. They are 12-bit signals. For more information on these signals, refer to the "FIFO Flag Usage Considerations" section on page 2-62.

ESTOP and FSTOP Usage

The ESTOP pin is used to stop the read counter from counting any further once the FIFO is empty (i.e., the EMPTY flag goes high). Likewise, the FSTOP pin is used to stop the write counter from counting any further once the FIFO is full (i.e., the Full flag goes high).

The FIFO counters in the Fusion device start the count at 0, reach the maximum depth for the configuration (e.g., 511 for a 512×9 configuration), and then restart at 0. An example application for the ESTOP, where the read counter keeps counting, would be writing to the FIFO once and reading the same content over and over without doing another write.

FIFO Flag Usage Considerations

The AEVAL and AFVAL pins are used to specify the 12-bit AEMPTY and AFULL threshold values, respectively. The FIFO contains separate 12-bit write address (WADDR) and read address (RADDR) counters. WADDR is incremented every time a write operation is performed, and RADDR is incremented every time a read operation is performed. Whenever the difference between WADDR and RADDR is greater than or equal to AFVAL, the AFULL output is asserted. Likewise, whenever the difference between WADDR and RADDR is less than or equal to AEVAL, the AEMPTY output is asserted. To handle different read and write aspect ratios, AFVAL and AEVAL are expressed in terms of total data bits instead of total data words. When users specify AFVAL and AEVAL in terms of read or write words, the SmartGen tool translates them into bit addresses and configures these signals automatically. SmartGen configures the AFULL flag, AFULL, to assert when the write address exceeds the read address by at least a predefined value. In a 2k×8 FIFO, for example, a value of 1,500 for AFVAL means that the AFULL flag will be asserted after a write when the difference between the write address and the read address reaches 1,500 (there have been at least 1500 more writes than reads). It will stay asserted until the difference between the write and read addresses drops below 1,500.

The AEMPTY flag is asserted when the difference between the write address and the read address is less than a predefined value. In the example above, a value of 200 for AEVAL means that the AEMPTY flag will be asserted when a read causes the difference between the write address and the read address to drop to 200. It will stay asserted until that difference rises above 200. Note that the FIFO can be configured with different read and write widths; in this case the AFVAL setting is based on the number of write data entries and the AEVAL setting is based on the number of read data entries. For aspect ratios of 512×9 and 256×18, only 4,096 bits can be addressed by the 12 bits of AFVAL and AEVAL. The number of words must be multiplied by 8 and 16, instead of 9 and 18. The SmartGen tool automatically uses the proper values. To avoid half-words being written or read, which could happen if different read and write aspect ratios are specified, the FIFO will assert Full or Empty as soon as at least a minimum of one word cannot be written or read. For example, if a two-bit word is written and a four-bit word is being read, FIFO will remain in the Empty state when the first word is written. This occurs even if the FIFO is not completely empty, because in this case a complete word cannot be read. The same is applicable in the Full state. If a four-bit word is written and a two-bit word is read, the FIFO is full and one word is read. The FULL flag will remain asserted because a complete word cannot be written at this point.

FIFO Characteristics
Timing Waveforms

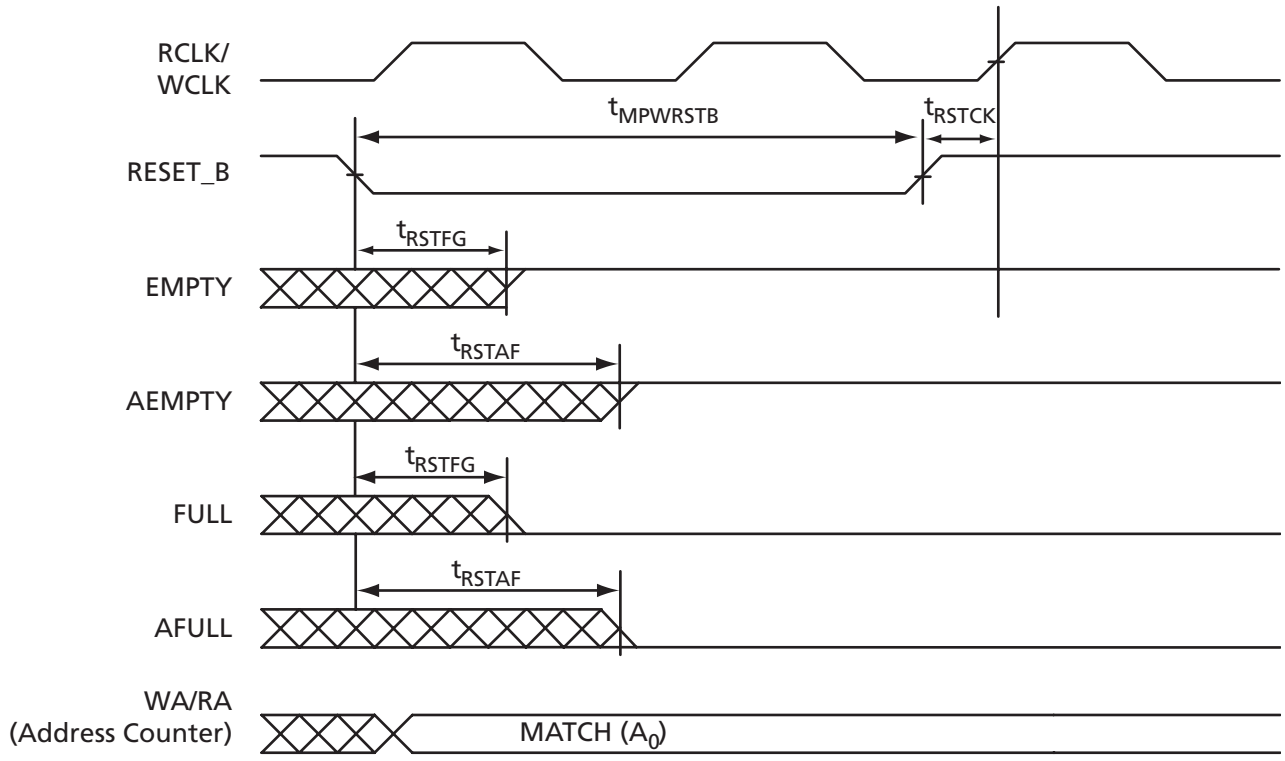


Figure 2-56 • **FIFO Reset**

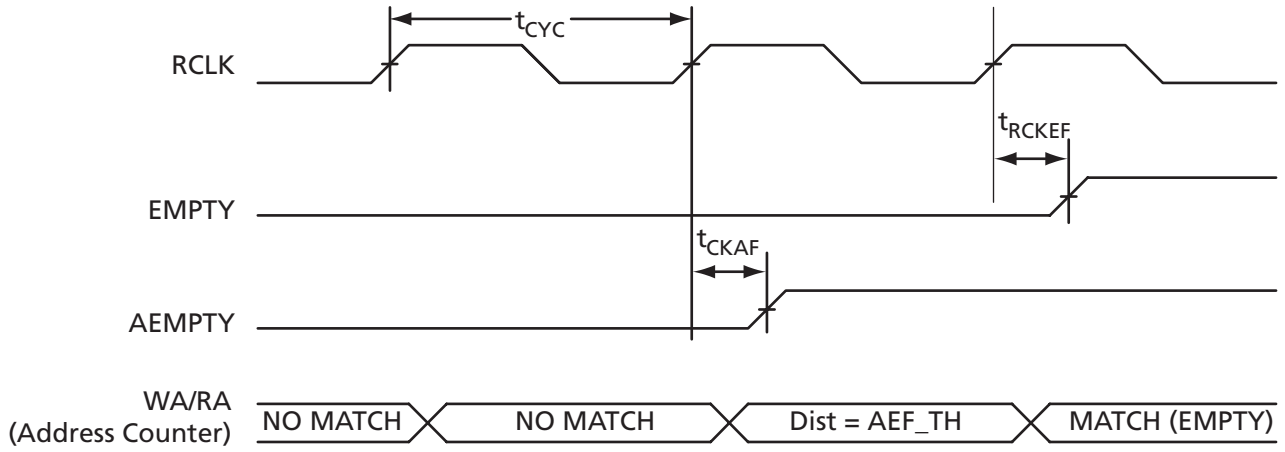


Figure 2-57 • **FIFO EMPTY Flag and AEMPTY Flag Assertion**

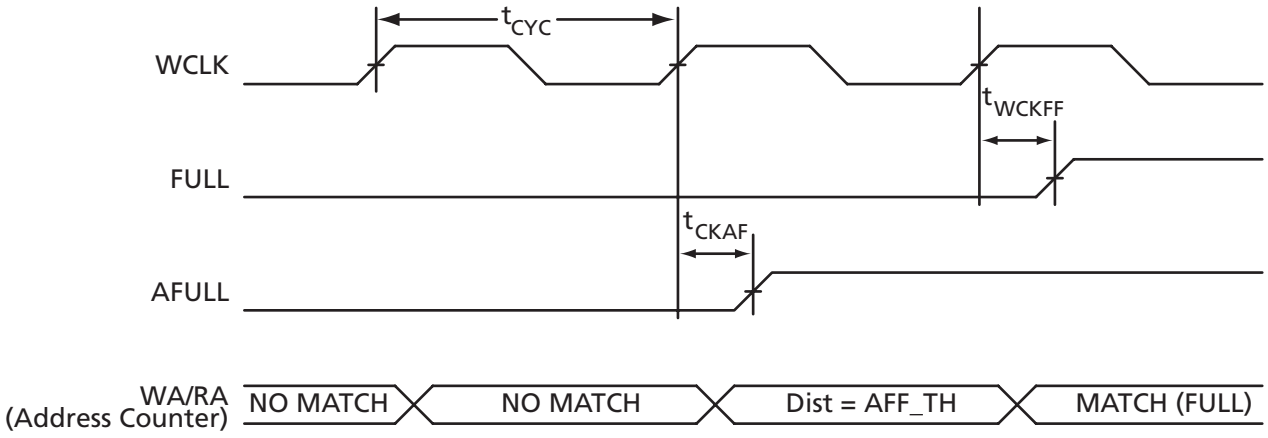


Figure 2-58 • **FIFO FULL and AFULL Flag Assertion**

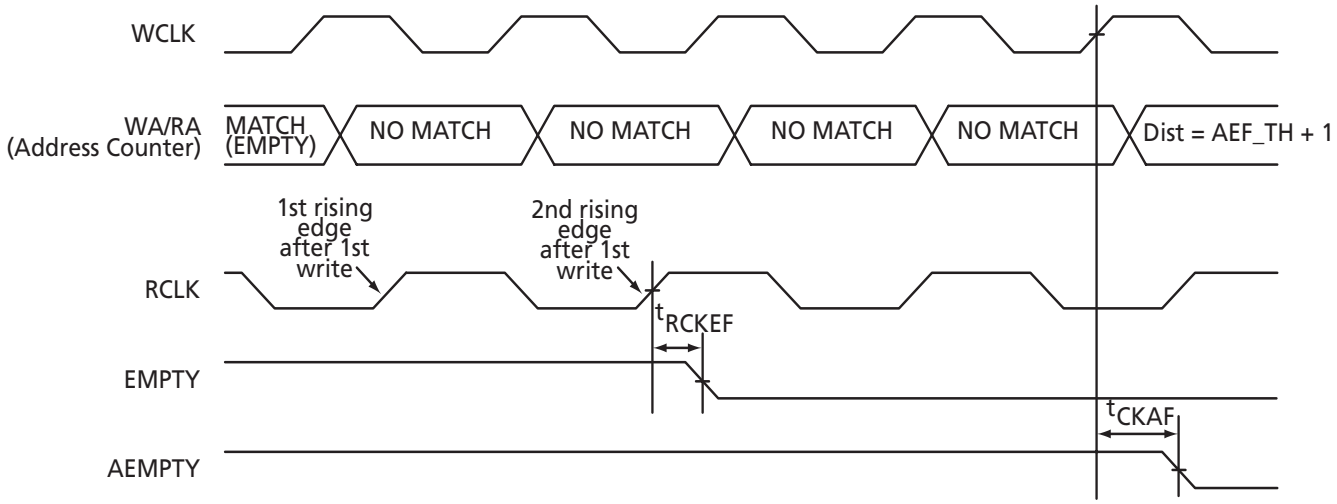


Figure 2-59 • **FIFO EMPTY Flag and AEMPTY Flag Deassertion**

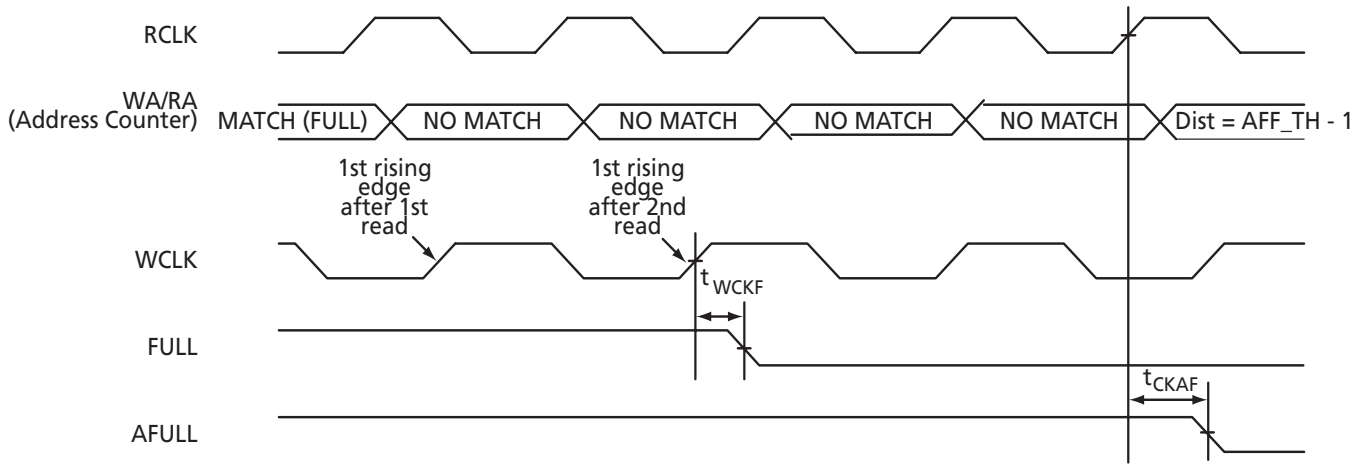


Figure 2-60 • **FIFO FULL Flag and AFULL Flag Deassertion**

Timing Characteristics

Table 2-33 • **FIFO**
Commercial Case Conditions: T_J = 70°C, V_{CC} = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{ENS}	REN_B,WEN_B Setup time	0.21	0.24	0.29	ns
t_{ENH}	REN_B, WEN_B Hold time	0.02	0.02	0.02	ns
t_{BKS}	BLK_B Setup time	0.25	0.29	0.34	ns
t_{BKH}	BLK_B Hold time	0.00	0.00	0.00	ns
t_{DS}	Input data (DI) Setup time	0.18	0.21	0.25	ns
t_{DH}	Input data (DI) Hold time	0.00	0.00	0.00	ns
t_{CKQ1}	Clock High to New Data Valid on DO (flow-through)	2.36	2.68	3.15	ns
t_{CKQ2}	Clock High to New Data Valid on DO (pipelined)	0.89	1.02	1.20	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	1.72	1.96	2.30	ns
t_{WCKFF}	WCLK High to Full Flag Valid	1.63	1.86	2.18	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	3.77	4.30	5.05	ns
t_{RSTFG}	RESET_B Low to Empty/Full Flag valid	1.69	1.93	2.27	ns
t_{RSTAF}	RESET_B Low to Almost-Empty/Full Flag Valid	3.66	4.17	4.90	ns
t_{RSTBQ}	RESET_B Low to Data out Low on DO (flow-through)	0.92	1.05	1.23	ns
	RESET_B Low to Data out Low on DO (pipelined)	0.92	1.05	1.23	ns
$t_{REMRSTB}$	RESET_B Removal	0.25	0.28	0.33	ns
$t_{RECRSTB}$	RESET_B Recovery	1.46	1.65	1.94	ns
$t_{MPWRSTB}$	RESET_B Minimum Pulse Width	0.20	0.23	0.27	ns
t_{CYC}	Clock Cycle time	1.85	2.09	2.46	ns

Note: *For the derating values at specific junction-temperature and voltage-supply levels, refer to Table 3-6 on page 3-6.*

Analog Block

With the Fusion family, Actel has introduced the world's first mixed-mode FPGA solution. Supporting a robust analog peripheral mix, Fusion devices will support a wide variety of applications. It is this Analog Block that separates Fusion from all other FPGA solutions on the market today.

By combining both Flash and high-speed CMOS processes in a single chip, these devices offer the best of both worlds. The high-performance CMOS is used for building RAM resources. These high performance structures support device operation up to 350 MHz. Additionally, the advanced Actel 0.13 µm Flash process incorporates high-voltage transistors and a high-isolation, triple-well process. Both of these are suited for the Flash-based programmable logic and nonvolatile memory structures.

High-voltage transistors support the integration of analog technology in several ways. They aid in noise immunity so that the analog portions of the chip can be better isolated from the digital portions, increasing analog accuracy. Because they support high voltages, Actel Flash FPGAs can be connected directly to high-voltage input signals, eliminating the need for external resistor divider networks, reducing component count, and increasing accuracy. By supporting higher internal voltages, the Actel advanced Flash process enables high-dynamic range on analog circuitry, increasing precision and signal/noise ratio. Actel Flash FPGAs also drive high-voltage outputs, eliminating the need for external level shifters and drivers.

The unique triple-well process enables the integration of high-performance analog features with increased noise immunity and better isolation. By increasing the efficiency of analog design, the triple-well process also enables a smaller overall design size, reducing die size and cost.

The Analog Block consists of the Analog Quad I/O structure, real-time counter (for details refer to the "Real-Time Counter System" section on page 2-31), analog to digital converter (ADC), and analog configuration multiplexer (ACM). All of these elements are combined in the single Analog Block macro, with which the user implements this functionality (Figure 2-61).

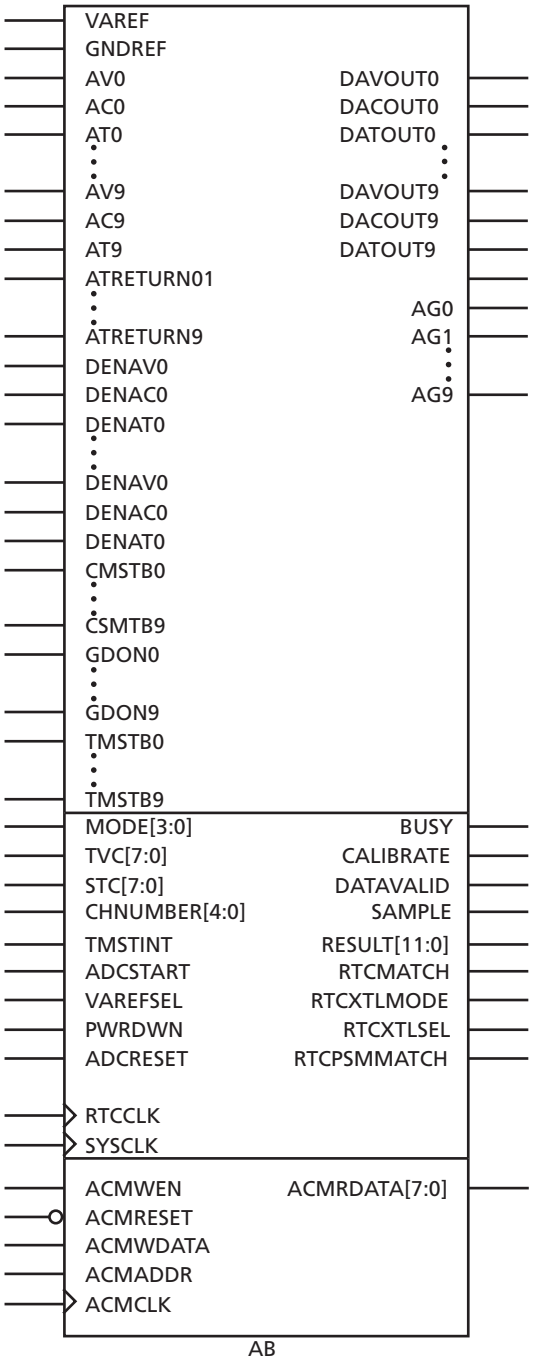


Figure 2-61 • **Analog Block Macro**

Table 2-34 describes each pin in the Analog Block. Each function within the Analog Block will be explained in detail in in the following sections.

Table 2-34 • **Analog Block Pin Description**

Signal Name	Number of Bits	Direction	Function	Location of Details
VAREF	1	Input/Output	Voltage reference for ADC; used as either input or output, depending on VREFSEL	ADC
GNDREF	1	Input	External ground reference	ADC
MODE[3:0]	4	Input	ADC operating mode	ADC
SYSCLK	1	Input	External system clock	
TVC[7:0]	8	Input	Clock divide control	ADC
STC[7:0]	8	Input	Sample time control	ADC
ADCSTART	1	Input	Start of conversion	ADC
PWRDWN	1	Input	Comparator power-down if 1	ADC
ADCRESET	1	Input	ADC initialize if 1	ADC
BUSY	1	Output	1 – Running conversion	ADC
CALIBRATE	1	Output	1 – Power-up calibration	ADC
DATAVALID	1	Output	1 – Valid conversion result	ADC
RESULT[11:0]	12	Output	Conversion result	ADC
TMSTBINT	1	Input	Internal temp. monitor strobe	ADC
SAMPLE	1	Output	1 – Analog input is sampled	ADC
VAREFSEL	1	Input	0 = Output internal voltage reference (2.56 V) to VAREF 1 = Input external voltage reference from VAREF and GNDREF	ADC
CHNUMBER[4:0]	5	Input	Analog input channel select	Input multiplexer
ACMCLK	1	Input	ACM clock	ACM
ACMWEN	1	Input	ACM write enable – active high	ACM
ACMRESET	1	Input	ACM reset – active low	ACM
ACMWDATA[7:0]	8	Input	ACM write data	ACM
ACMRDATA[7:0]	8	Output	ACM read data	ACM
ACMADDR[7:0]	8	Input	ACM address	ACM
CMSTB0 to CMSTB9	10	Input	Current monitor strobe – 1 per quad, active high	Analog Quad
GDON0 to GDON9	10	Input	Control to power MOS – 1 per quad	Analog Quad
TMSTB0 to TMSTB9	10	Input	Temperature monitor strobe – 1 per quad; active high	Analog Quad
DAVOUT0, DACOUT0, DATOUT0 to DAVOUT9, DACOUT9, DATOUT9	30	Output	Digital outputs – 3 per quad	Analog Quad
DENAV0, DENAC0, DENAT0 to DENAV9, DENAC9, DENAT9	30	Input	Digital input enables – 3 per quad	Analog Quad
AV0	1	Input	Analog Quad 0	Analog Quad
AC0	1	Input		Analog Quad
AG0	1	Output		Analog Quad
AT0	1	Input		Analog Quad

Table 2-34 • **Analog Block Pin Description (Continued)**

Signal Name	Number of Bits	Direction	Function	Location of Details
ATRETURN01	1	Input	Temperature monitor return shared by Analog Quads 0 and 1	Analog Quad
AV1	1	Input	Analog Quad 1	Analog Quad
AC1	1	Input		Analog Quad
AG1	1	Output		Analog Quad
AT1	1	Input		Analog Quad
AV2	1	Input	Analog Quad 2	Analog Quad
AC2	1	Input		Analog Quad
AG2	1	Output		Analog Quad
AT2	1	Input		Analog Quad
ATRETURN23	1	Input	Temperature monitor return shared by Analog Quads 2 and 3	Analog Quad
AV3	1	Input	Analog Quad 3	Analog Quad
AC3	1	Input		Analog Quad
AG3	1	Output		Analog Quad
AT3	1	Input		Analog Quad
AV4	1	Input	Analog Quad 4	Analog Quad
AC4	1	Input		Analog Quad
AG4	1	Output		Analog Quad
AT4	1	Input		Analog Quad
ATRETURN45	1	Input	Temperature monitor return shared by Analog Quads 4 and 5	Analog Quad
AV5	1	Input	Analog Quad 5	Analog Quad
AC5	1	Input		Analog Quad
AG5	1	Output		Analog Quad
AT5	1	Input		Analog Quad
AV6	1	Input	Analog Quad 6	Analog Quad
AC6	1	Input		Analog Quad
AG6	1	Output		Analog Quad
AT6	1	Input		Analog Quad
ATRETURN67	1	Input	Temperature monitor return shared by Analog Quads 6 and 7	Analog Quad
AV7	1	Input	Analog Quad 7	Analog Quad
AC7	1	Input		Analog Quad
AG7	1	Output		Analog Quad
AT7	1	Input		Analog Quad
AV8	1	Input	Analog Quad 8	Analog Quad
AC8	1	Input		Analog Quad
AG8	1	Output		Analog Quad
AT8	1	Input		Analog Quad
ATRETURN89	1	Input	Temperature monitor return shared by Analog Quads 8 and 9	Analog Quad

Table 2-34 • **Analog Block Pin Description (Continued)**

Signal Name	Number of Bits	Direction	Function	Location of Details
AV9	1	Input	Analog Quad 9	Analog Quad
AC9	1	Input		Analog Quad
AG9	1	Output		Analog Quad
AT9	1	Input		Analog Quad
RTCMATCH	1	Output	MATCH	RTC
RTCPSMMATCH	1	Output	MATCH connected to VRPSM	RTC
RTCXTLMODE[1:0]	2	Output	Drives XTLOSC RTCMODE[1:0] pins	RTC
RTCXTLSEL	1	Output	Drives XTLOSC MODESEL pin	RTC
RTCCLK	1	Input	RTC clock input	RTC

Analog Quad

With the Fusion family, Actel introduces the Analog Quad, shown in Figure 2-62 on page 2-70, as the basic analog I/O structure. The Analog Quad is a four-channel system used to precondition a set of analog signals before sending to the ADC for conversion into a digital signal. In order to maximize the usefulness of the Analog Quad, the analog input signals may also be configured as LVTTL digital input signals. The Analog Quad is divided into four sections.

The first section is called the Voltage Monitor Block and its input pin is named AV. It contains a 2-channel analog multiplexer which allows an incoming analog signal to be routed directly to the ADC or allows the signal to be routed to a pre-scaler circuit before being sent to the ADC. The pre-scaler can be configured to accept analog signals between –12 V and 0, or between 0 and +12 V. The pre-scaler circuit scales the voltage applied to the ADC input pad such that it is compatible with the ADC input voltage range. The AV pin may also be used as a digital input pin.

The second section of the Analog Quad is called the Current Monitor Block. Its input pin is named AC. The Current Monitor Block contains all the same functions as the Voltage Monitor Block with one addition, which is a current monitoring function. A small external current sensing resistor (typically less than 1 Ω) is connected between the AV and AC pins and is in series with a power source. The Current Monitor Block contains a current monitor circuit that converts the current through the external resistor to a voltage which can then be read using the ADC.

The third part of the Analog Quad is called the Gate Driver Block and its output pin is named AG. This section is used to drive an external FET. There are two modes available: a high current drive mode and a current source control mode. Both negative and positive voltage polarities are available and in the current source control mode, four different current levels are available.

The fourth section of the Analog Quad is called the Temperature Monitor Block and its input pin name is AT. This block is similar to the Voltage Monitor Block except that it has an additional function: it can be used to monitor the temperature of an external diode connected transistor. It has a modified pre-scaler and is limited to positive voltages only.

The Analog Quad can be configured during design time by Actel Libero IDE; however, the Analog Configuration MUX (ACM) can be used to change the parameters of any of these I/Os during runtime. This type of change is referred to as a context switch. The Analog Quad is a modular structure that is replicated to generate the analog I/O resources. Each Fusion device supports between 5 and 10 Analog Quads.

The analog pads are numbered to clearly identify both the type of pad (voltage, current, gate driver, or temperature pad) and its corresponding Analog Quad (AV0, AC0, AG0, AT0, AV1, …, AC9, AG9, and AT9). There are three types of input pads (AVx, ACx, and ATx) and one type of analog output pad (AGx). Since there can be up to 10 Analog Quads on a device, there can be a maximum of 30 analog input pads and 10 analog out pads.

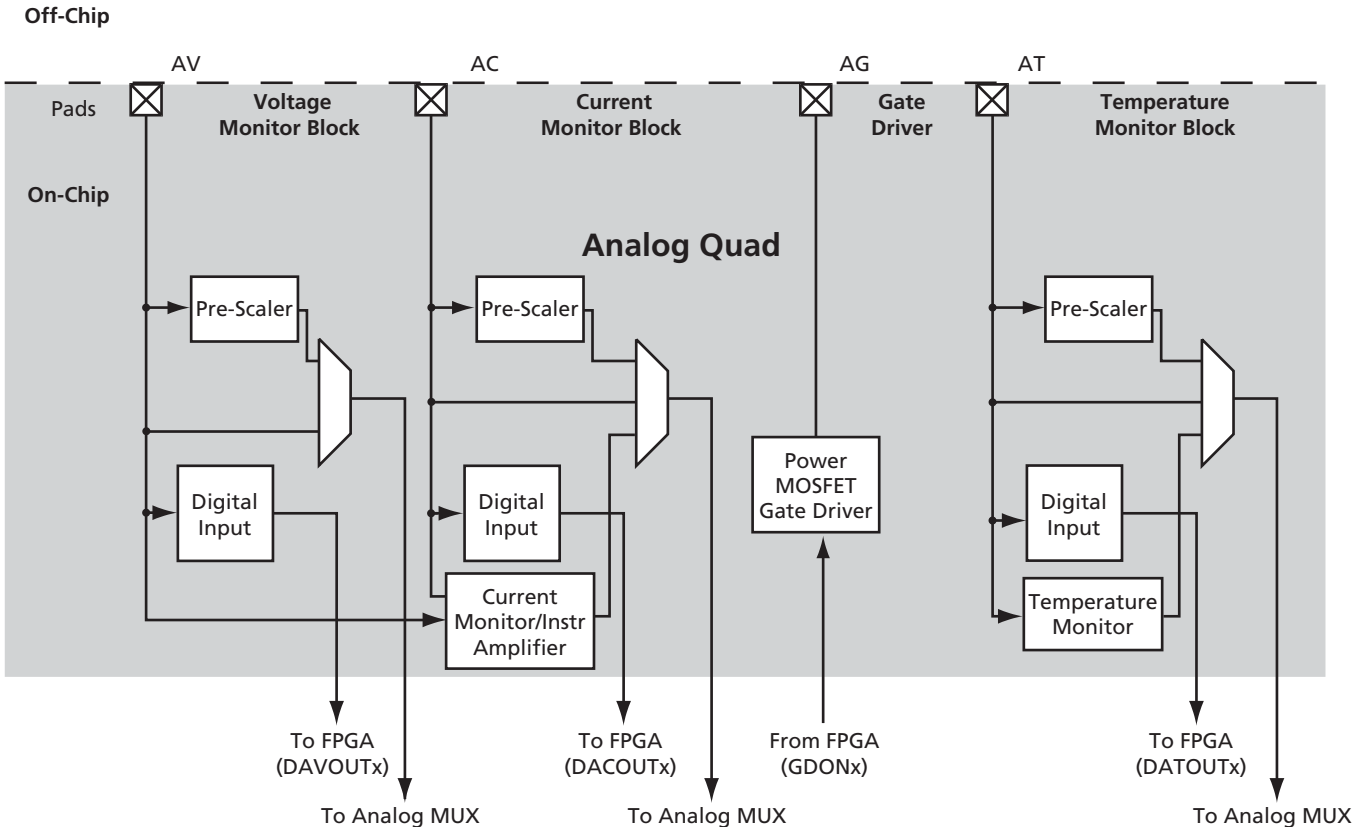


Figure 2-62 • **Analog Quad**

Voltage Monitor

The Fusion Analog Quad offers a robust set of voltage monitoring capabilities unique in the FPGA industry. The Analog Quad is comprised of three analog input pads—Analog Voltage (AV), Analog Current (AC), and Analog Temperature (AT)—and a single gate driver output pad, Analog Gate (AG). There are many common characteristics among the analog input pads. Each analog input can be configured to connect directly to the input MUX of the ADC. When configured in this manner (Figure 2-63), there will be no prescaling of the input signal. Care must be taken in this mode not to drive the ADC into saturation by applying an input voltage greater than the reference voltage. The internal reference voltage of the ADC is 2.56 V. Optionally, an external reference can be supplied by the user. The external reference can be a maximum of 3.3 V DC.

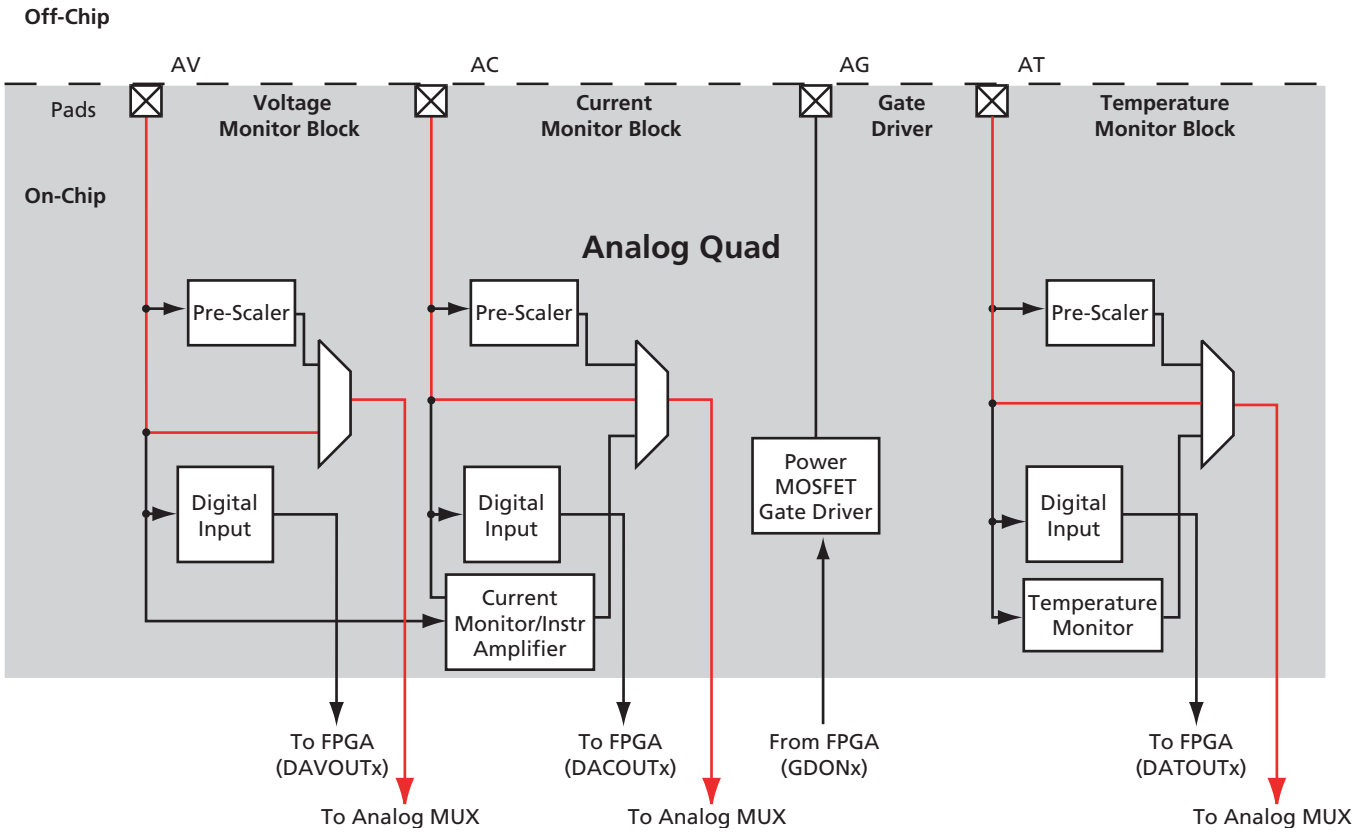


Figure 2-63 • **Analog Quad Direct Connect**

The Analog Quad inputs are tolerant up to 12 V ± 10%. The Analog Quad offers a wide variety of prescaling options to enable the ADC to resolve the input signals. Figure 2-64 shows the path through the Analog Quad for a signal that is to be prescaled prior to conversion. The ADC internal reference voltage and the pre-scaler factors were selected to make both prescaling and postscaling of the signals easy, binary calculations (refer to Table 2-44 on page 2-91 for details). When an analog input pad is configured with a pre-scaler, there will be a 1 MΩ resistor to ground. This occurs even when the device is off.

These scaling factors hold true whether the particular pad is configured to accept a positive or negative voltage. Note that while the AV and AC pads support the same prescaling factors, the AT pad supports a reduced set of prescaling factors and support positive voltages only.

Typical scaling factors are given in Table 2-44 on page 2-91, and the gain error (which contributes to the minimum and maximum) is in Table 2-40 on page 2-86.

Each I/O will draw power when connected to power (3 mA at 3 V) (added to power consumption portion of this section.

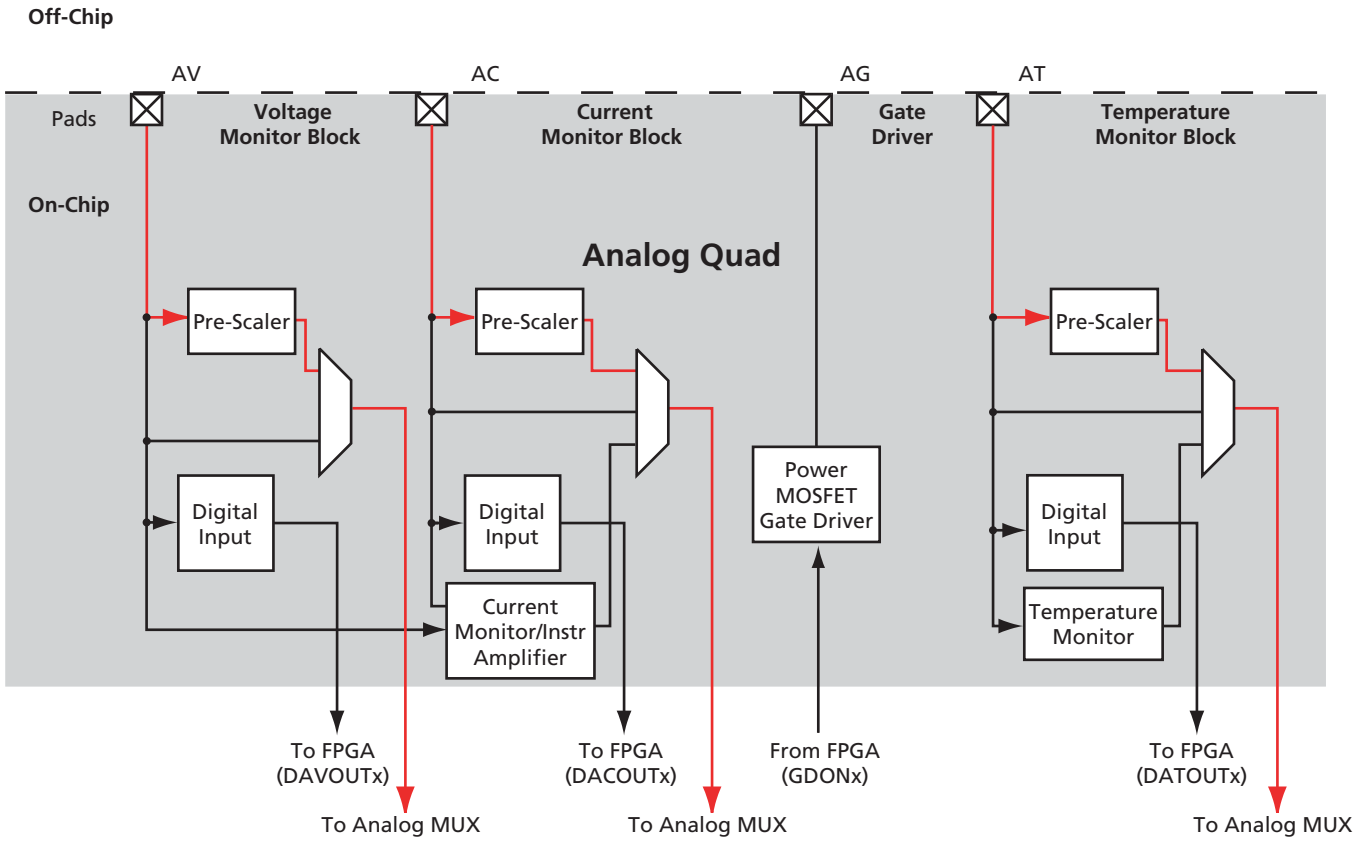


Figure 2-64 • **Analog Quad Pre-Scaler Input Configuration**

Direct Digital Input

The AV, AC, and AT pads can also be configured as high voltage digital inputs (Figure 2-65). As these pads are 12 V tolerant, the digital input can also be up to 12 V. However, the frequency at which these pads can operate is limited to 10 MHz.

To enable one of these analog input pads to operate as a digital input, its corresponding Digital Input enable (DENAxy) pin on the Analog Block must be pulled high, where x is either V, C, or T (for AV, AC, or AT pads respectively) and y is 0 to 9, corresponding to the appropriate Analog Quad.

When the pad is configured as a digital input, this signal will come out of the Analog Block macro on the appropriate DAxOUTy pin, where x represents the pad type (V for AV pad, C for AC pad, or T for AT pad) and y represents the appropriate Analog Quad number. Example: if the AT pad in Analog Quad 5 is configured as a digital input, it will come out on the DATOUT5 pin of the Analog Block macro.

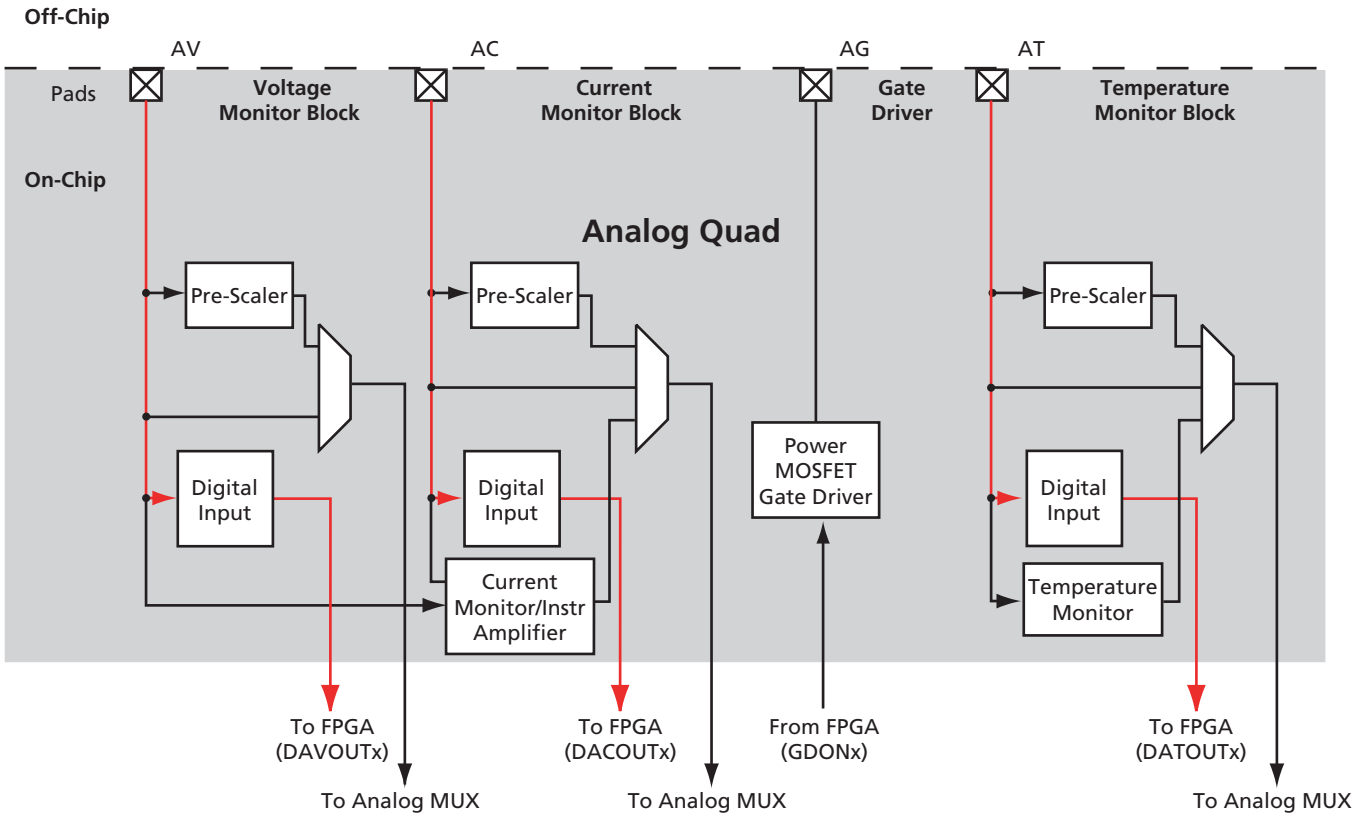


Figure 2-65 • **Analog Quad Direct Digital Input Configuration**

Current Monitor

The Fusion Analog Quad is an excellent element for voltage and current monitoring applications. In addition to supporting the functionality offered by the AV pad, the AC pad may be configured to monitor current across an external sense resistor (Figure 2-66). To support this current monitor function, the 10x differential amplifier passes the amplified difference between the AV and AC pads to the ADC. The potential on the AV pad MUST be greater than the AC pad in current monitor mode. The amplifier enables the user to use very small resistor values, thereby limiting any impact on the circuit. This function of the AC pad does not affect the AV pad operation. The current monitor can resolve differences between the AV and AC pads as low as 2 mV.

The current monitor is activated via the Current Monitor Strobe pin (CMST) on the Analog Block macro. There is a CMST pin for each Analog Quad present on the device (CMST0–CMST9).

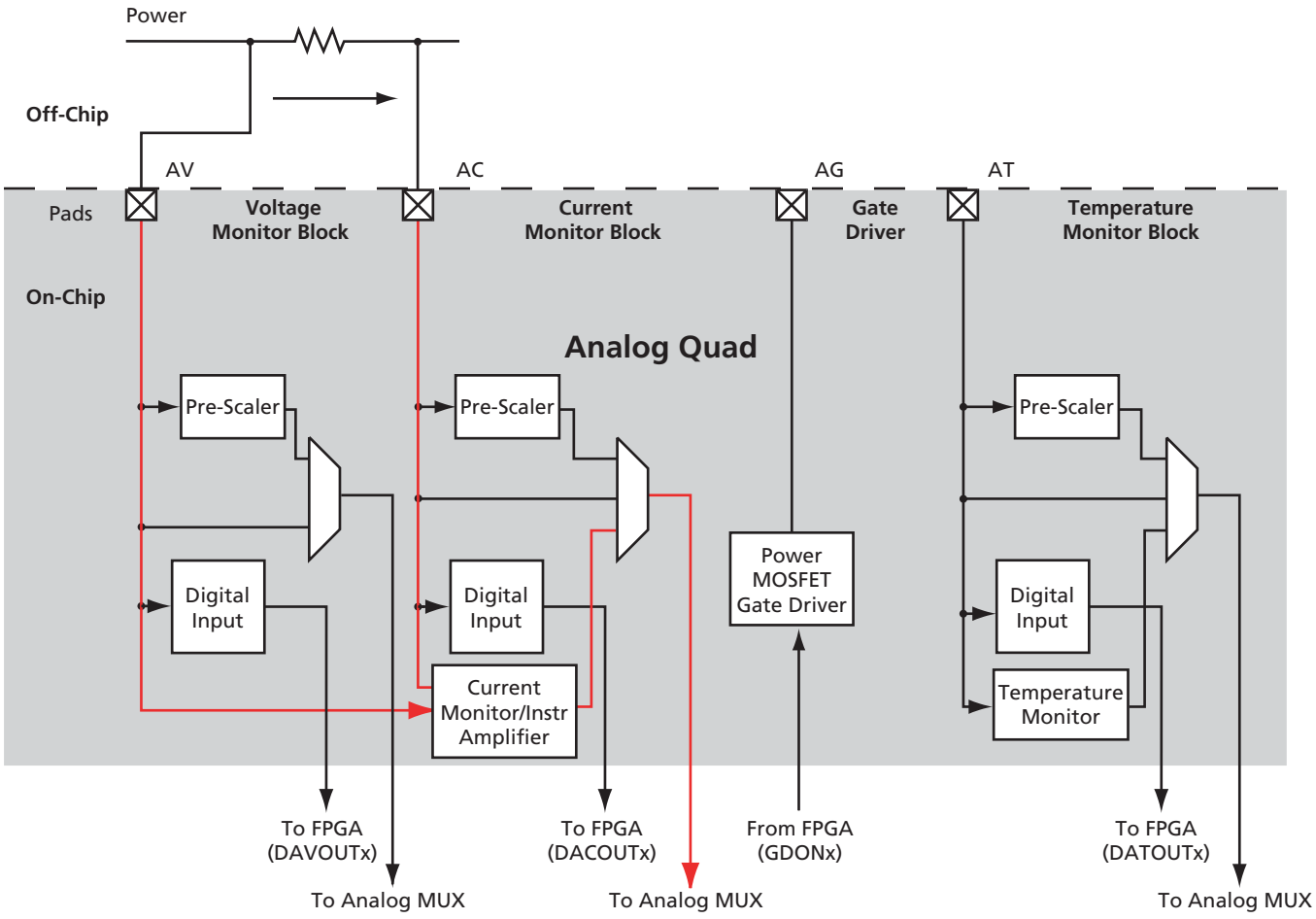


Figure 2-66 • **Analog Quad Current Monitor Configuration**

Figure 2-67 illustrates the current monitor operation with an example of the AC pad operating in current monitor mode. In this example, a 10 V supply is passed across a 0.10 Ω resistor. The difference between the AV and AC pad passes through the 10x amplifier and is then converted by the ADC. In this example, the current drawn from a 10 V supply is measured by the voltage drop it creates across the 0.1 Ω current sampling resistor. This voltage drop is in turn amplified by ten times by the 10x amplifier and then measured by the ADC. Considering the values shown in Figure 2-67, and making use of Ohm's law, it can be seen that the 1 A current creates a voltage drop across the sampling resistor of 0.1 V, which becomes 1 V after amplification. Thus, the ADC measures a current of 1 A as 1 V, and a current of 0.2 A would therefore be read as 0.2 V by the ADC.

Note that because of the 10x amplification of the voltage difference between these pads, the maximum measurable difference between the AV and AC pads is the ADC reference voltage divided by 10. A larger AV-to-AC voltage drop will result in ADC saturation, i.e., the digital code output by the ADC will stay stuck at the full scale value for the chosen ADC reference voltage. Therefore, the user must select the external sense resistor appropriately. Another important consideration is that the absolute value of the voltage on the AV pin should be greater than or equal to the absolute value of the voltage on the AC pin for the current monitor to function correctly. If voltage available for reading by the ADC the current monitor output voltage available for reading by the ADC will be zero.

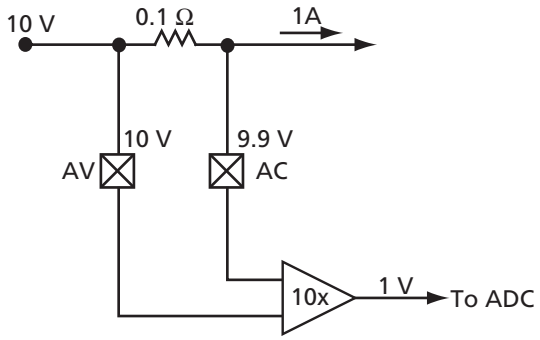


Figure 2-67 • **Current Monitor Example**

Gate Driver

The Fusion Analog Quad includes a Gate Driver, connected to the quad's AG pin (Figure 2-68). Designed to work with external P-Channel or N-Channel MOSFETs, the Gate driver is a configurable current sink or source and requires an external pull-up or a pull-down resistor. The AG supports 4 selectable gate drive levels: 1 µA, 3 µA, 10 µA, and 30 µA (Figure 2-69 on page 2-77). The AG also supports a High Current Drive mode in which it can sink 25 mA. Modeled on an open drain style output, it does not output a voltage level without an appropriate pull-up or pull-down resistor.

The AG pad is turned on via the corresponding GDONx pin in the Analog Block macro, where x is the number of the corresponding Analog Quad for AG pad to be enabled (GDON0 to GDON9). The maximum AG pad switching frequency is 1.25 MHz.

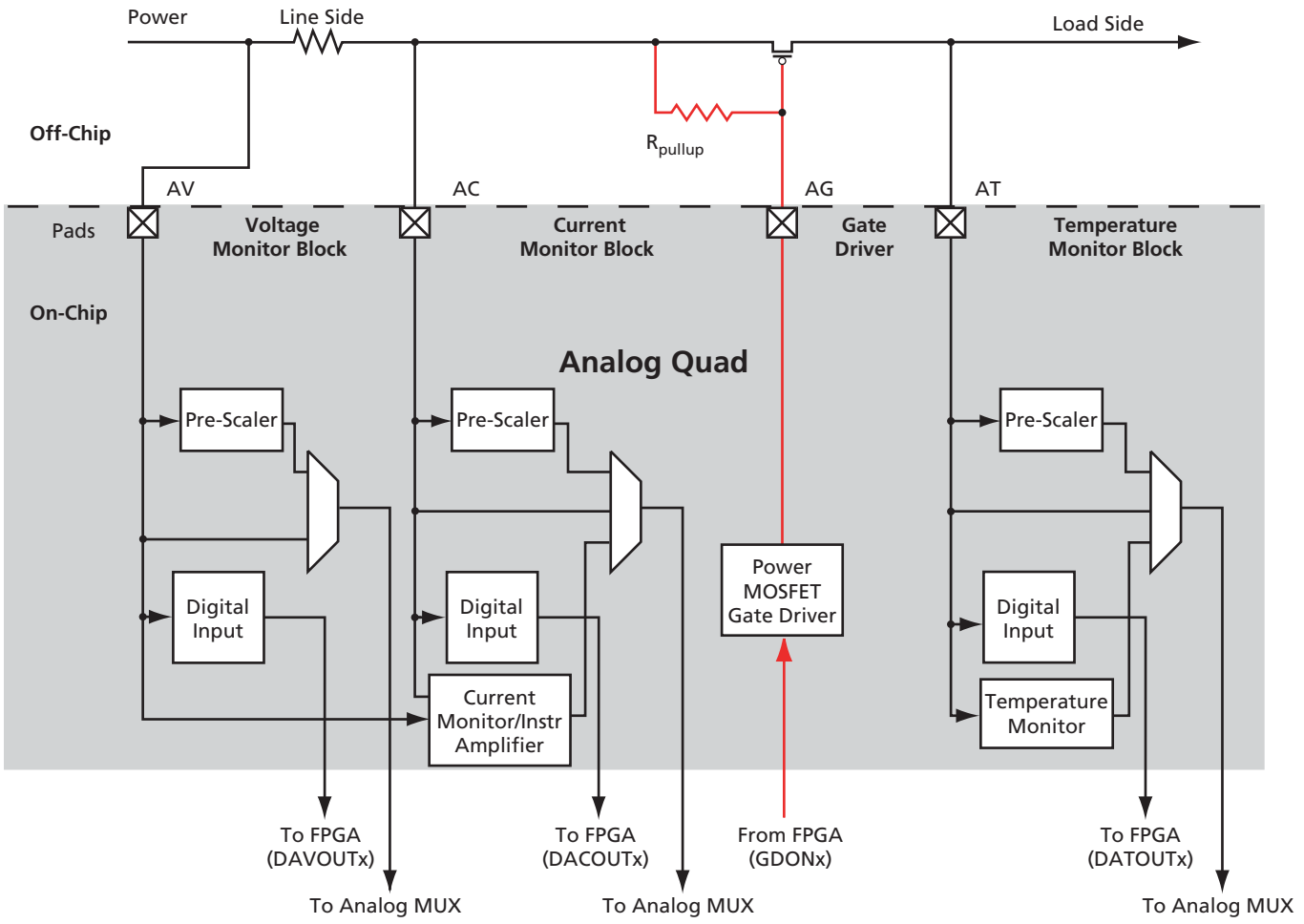


Figure 2-68 • **Gate Driver**

The gate-to-source voltage (Vgs) of the external MOSFET is limited to the programmable drive current times the external pull-up or pull-down resistor value (EQ 2-1).

$$Vgs \leq Ig \times (R_{pullup} \text{ or } R_{pulldown})$$

EQ 2-1

The rate at which the gate voltage of the external MOSFET slews is determined by the current Ig sourced or sunk by the AG pin and the gate to source capacitance CGS of the external MOSFET. As an approximation, the slew rate is given by EQ 2-2.

$$dv/dt = Ig/CGS$$

EQ 2-2

CGS is not a fixed capacitance but, depending on the circuitry connected to its drain terminal, can vary significantly during the course of a turn-on or turn-off transient. Thus EQ 2-2 on page 2-76 can only be used for a first order estimate of the switching speed of the external MOSFET.

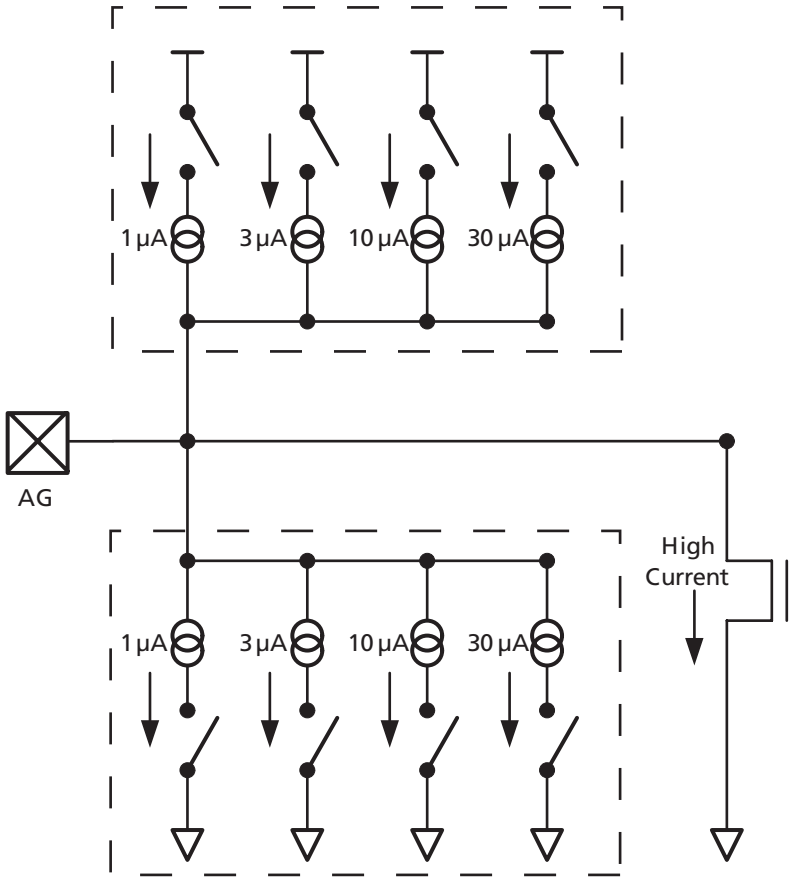


Figure 2-69 • **Gate Driver Example**

Temperature Monitor

The final pin in the Analog Quad is the Analog Temperature (AT) pin. The AT pin is used to implement an accurate temperature monitor in conjunction with an external diode connected bipolar transistor (Figure 2-70). For improved temperature measurement accuracy, it is important to use the ATRTN pin for the return path of the current sourced by the AT pin. Each ATRTN pin is shared between two adjacent Analog Quads. Additionally, if not used for temperature monitoring, the AT pin can provide functionality similar to that of the AV pad. However, in this mode only positive voltages may be applied to the AT pin and only two pre-scaler factors are available (16 V and 4 V full scale—refer to Table 2-34 on page 2-67).

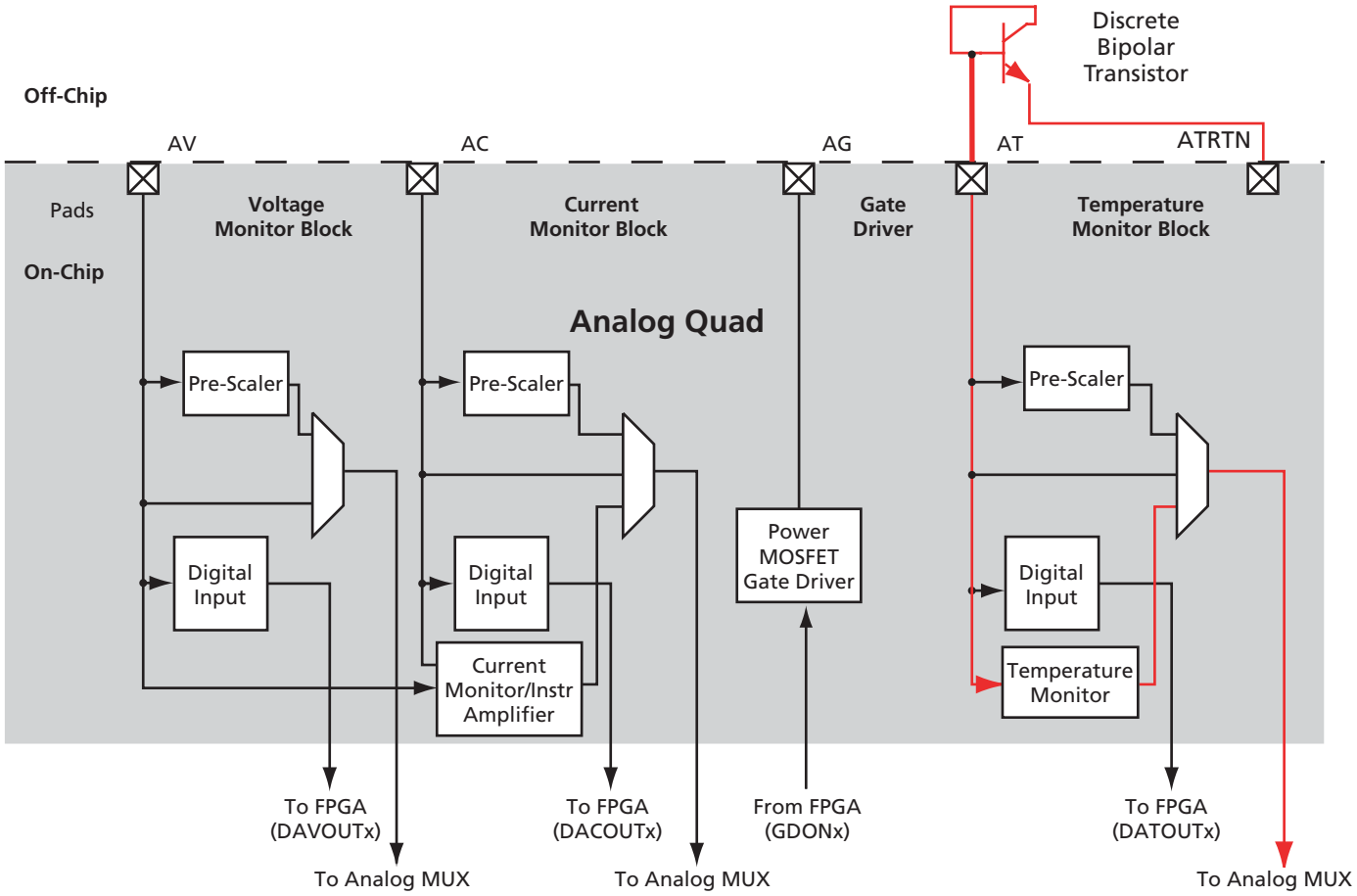


Figure 2-70 • **Temperature Monitor Quad**

The well-known temperature dependence of the current versus voltage characteristics of a PN junction form the basis of the temperature measurement scheme implemented in the Fusion devices. Figure 2-71 shows a simplified schematic of this implementation. The diode connected bipolar transistor is used as the temperature sensor. The 12.5x amplifier is a switched-capacitor based design and as such can make pseudo-differential measurements i.e., it multiplies by 12.5 the difference between the voltages that appears across the diode connected bipolar transistor with the 90 µA current source switched in (diode current = 100 µA) and when it is switched out (diode current = 10 µA). The voltage applied to the ADC is then given in EQ 2-3.

$$V_{ADC} = 12.5[(nkT/q) \text{ in } (100\ \mu A/10\ \mu A)] = 250 \times 10^{-3} \times T$$

EQ 2-3

where

n = Ideality factor of the diode connected transistor. It is typically 1.008 for the Actel recommended transistor type 2N3904. It does vary from transistor to transistor even of the same type and so for very accurate results calibration is needed.

k = 1.3806×10^{-23} J/K is the Boltzman constant

q = 1.602×10^{-19} C is the charge of a proton and as such the ADC reads the temperature T in degrees Kelvin

The temperature monitor block is accurate to 5°C. This accuracy is limited by the ideality of the external diode connected bipolar transistor. From the above equation it can be seen that voltage output by the temperature monitor block is about 2.50 mV per degree Kelvin. Thus, it is essential to observe good design practices to reduce noise coupled to the on-board and off-board wiring associated with the diode connected bipolar transistor.

A temperature reading is initiated via the Temperature Monitor Strobe (TMSTB) pin associated with a particular Analog Quad. There are up to 10 TMSTB pins in the device (TMSTB0 – TMSTB9).

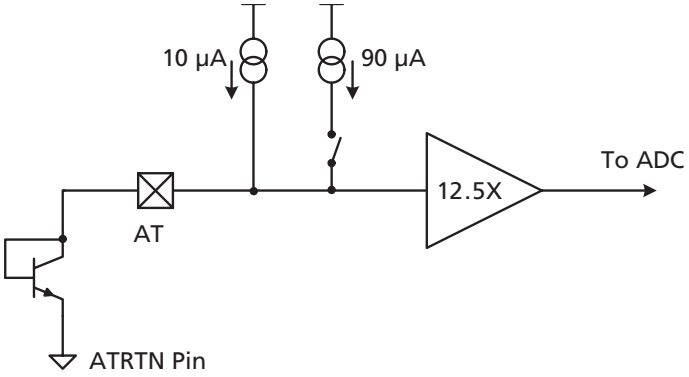


Figure 2-71 • **Temperature Monitor Circuit**

Analog to Digital Converter Block

At the heart of the Fusion analog system is a programmable Successive Approximation Register (SAR) analog to digital converter (ADC). The ADC can support 8-, 10-, or 12-bit modes of operation. In 12-bit mode, the ADC can resolve 500 ksps. The input to the ADC is a large 32:1 analog input multiplexer. A simplified block diagram of the Analog Quads, analog input multiplexer, and ADC is shown in Figure 2-72. The ADC offers multiple self-calibrating modes to ensure consistent high performance at both power-up and during runtime.

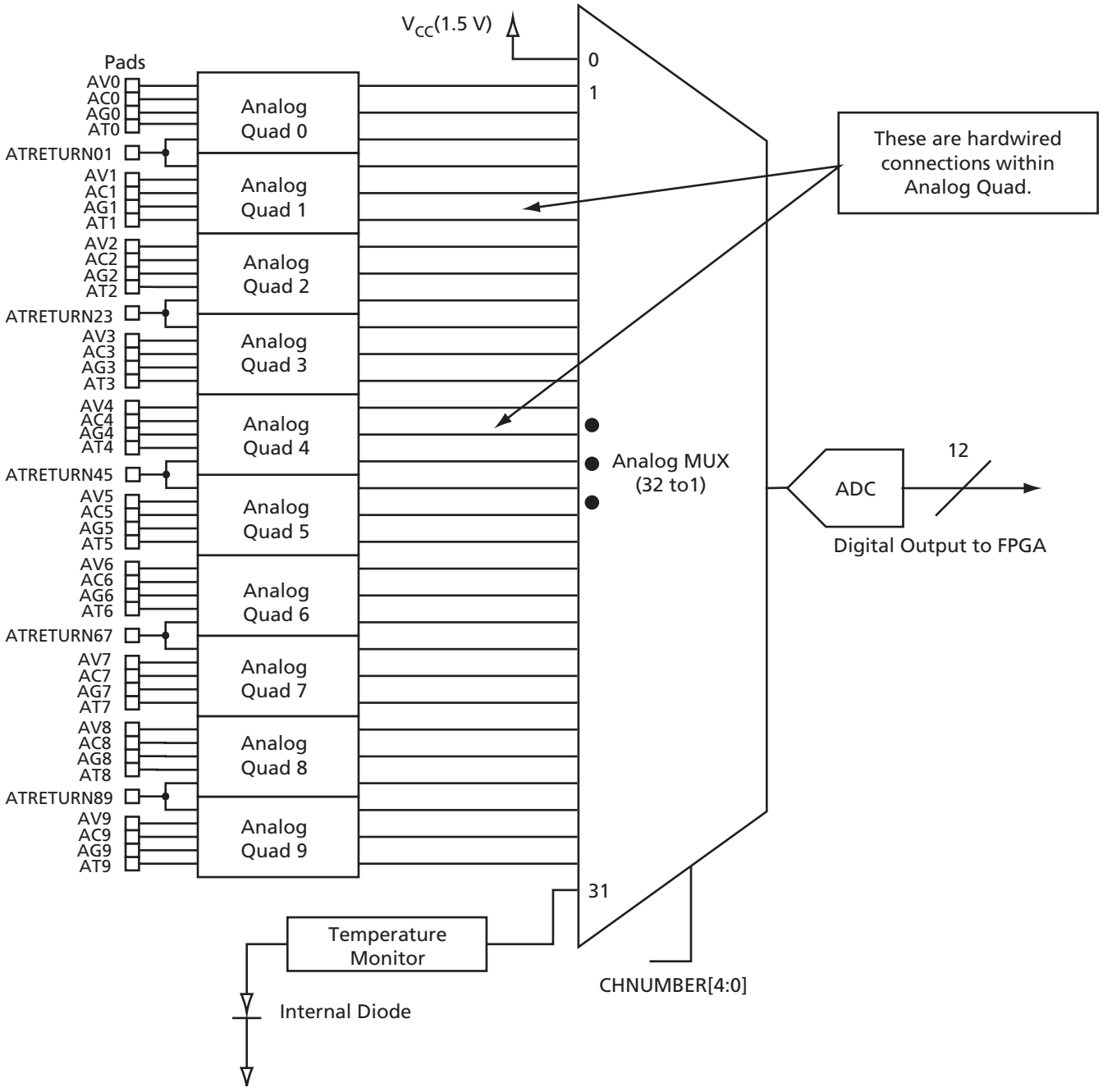


Figure 2-72 • **ADC Block Diagram**

ADC Input Multiplexer

At the input to the Fusion ADC is a 32:1 multiplexer. Of the 32 input channels, up to 30 are user definable. Two of these channels are hardwired internally. Channel 31 connects to an internal temperature diode, so that the temperature of the Fusion device itself can be monitored. Channel 0 is wired to the FPGA's 1.5 V V_{CC} supply, enabling the Fusion device to monitor its own power supply. Doing this internally makes it unnecessary to use an analog I/O to support these functions. The balance of MUX inputs are connected to Analog Quads (see the "Analog Quad" section on page 2-69). Table 2-35 defines which Analog Quad inputs are associated with which specific analog MUX channel. The number of Analog Quads present is device-dependent; refer to the family list in Table 1 on page i of this datasheet for the number of quads per device. Regardless of the number of quads populated in a device, the internal connections to both V_{CC} and internal temperature diode remain on Channels 0 and 31 respectively. In order to sample the internal temperature monitor, it must be strobed (similar to the AT pads). The TMSTBINT pin on the Analog Block macro is the control for strobing the internal temperature measurement diode.

To determine which channel is selected for conversion, there is a 5-pin interface on the Analog Block, CHNUMBER[4:0], defined in Table 2-36 on page 2-82. Table 2-35 shows the correlation between the analog MUX input channels and the analog input pins.

Table 2-35 • **Analog MUX Channels**

Analog MUX Channel	Signal	Analog Quad Number
0	Vcc_analog	
1	AV0	Analog Quad 0
2	AC0	
3	AT0	
4	AV1	Analog Quad 1
5	AC1	
6	AT1	
7	AV2	Analog Quad 2
8	AC2	
9	AT2	
10	AV3	Analog Quad 3
11	AC3	
12	AT3	
13	AV4	Analog Quad 4
14	AC4	
15	AT4	
16	AV5	Analog Quad 5
17	AC5	
18	AT5	
19	AV6	Analog Quad 6
20	AC6	
21	AT6	
22	AV7	Analog Quad 7
23	AC7	
24	AT7	
25	AV8	Analog Quad 8
26	AC8	

Table 2-35 • **Analog MUX Channels (Continued)**

Analog MUX Channel	Signal	Analog Quad Number
27	AT8	
28	AV9	Analog Quad 9
29	AC9	
30	AT9	
31	Internal temperature monitor	

Table 2-36 • **Channel Selection**

Channel Number	CHNUMBER[4:0]
0	00000
1	00001
2	00010
3	00011
.	.
.	.
.	.
30	11110
31	11111

ADC Description

The Actel Fusion ADC is a 12-bit SAR ADC. It offers a wide variety of configurations to support many customer use models. It can be programmed to operate in 8-, 10-, or 12-bit modes. This is controlled by MODE[3:0], as defined in Table 2-37.

The conversion time can vary greatly depending on the SYSCLK frequency, ADCCLK frequency (determined by TVC), the STC settings, and the conversion bit-resolution (MODE). See EQ 2-4 through EQ 2-6.

$$t\_conv = t\_sync\_read + t\_sample + t\_distrib + t\_post\_cal + t\_sync\_write$$

EQ 2-4

$$t\_conv = SYSCLK\ period + ((2 + STC) * ADCCLK\ period) + (8, 10\ or\ 12 * ADCCLK\ period) + (2 * ADCCLK\ period) + SYSCLK\ period$$

EQ 2-5

$$ADCCLK = SYSCLK/4 * (1 + TVC)$$

EQ 2-6

where:

t_sync_read = Time for latching the input data

t_sample = Time for sampling the analog signal

t_distrib = Time for charge distribution

t_post_cal = Time for post-calibration

t_sync_write = Time for latching the output data

Table 2-37 • **MODE[3:0] Truth Table**

ADC Mode	Mode[3]	Mode[2]	Mode[1]	Mode[0]
10-bit	0	0	0	0
12-bit	0	0	0	1
8-bit	0	0	1	0
Reserved	0	0	1	1
10-bit without internal power-down after conversion	0	1	0	0
12-bit without internal power-down after conversion	0	1	0	1
8-bit without internal power-down after conversion	0	1	1	0
Reserved	0	1	1	1
10-bit without internal calibration	1	0	0	0
12-bit without internal calibration	1	0	0	1
8-bit without internal calibration	1	0	1	0
Reserved	1	0	1	1
10-bit without internal calibration and without internal power-down after conversion	1	1	0	0
12-bit without internal calibration and without internal power-down after conversion	1	1	0	1
8-bit without internal calibration and without internal power-down after conversion	1	1	1	0
Reserved	1	1	1	1

In addition to the resolution, the ADC offers many different timing configurations. The clock for the ADC is brought into the ADC via the SYSCLK pin on the Analog Block. This base clock can be divided down to suit ADC performance requirements. The clock divider for the ADC clock is TVC[7:0], defined in Table 2-38.

Table 2-38 • **ADC Clock Divider**

TVC[7:0]	**ADC Clock = SYSCLK/(4 × (TVC + 1))**	
0	00000000	SYSCLK/4
1	00000001	SYSCLK/8
.		.
.		.
.		.
126	01111110	SYSCLK/508
127	01111111	SYSCLK/5012
128	10000000	SYSCLK/516
.		
.		
255	11111111	SYSCLK/1024

The amount of time allocated for a single sample is also programmable. The clock period defined by 1/ADC clock is the basic unit of measurement for the Sample Time Control (STC). The Sample Time Control table details how the STC can be configured via the STC[7:0] pins on the Analog Block, defined in Table 2-39.

Table 2-39 • **Sample Time Control (STC)**

	STC[7:0]	**Sample Time = (STC + 2) × ADC_CLK Period**
0	00000000	2 ADC clock periods
1	00000001	3 ADC clock periods
.		
.		
254	11111110	256 ADC clock periods
255	11111111	257 ADC clock periods

The Fusion device has an integrated on-chip 2.56 V reference for the ADC. The value of this reference voltage was chosen to make the pre-scaling and postscaling factors for the pre-scaler blocks change in a binary fashion. However, if desired an external reference voltage of up to 3.3 V can be connected between the VAREF and GNDREF pins. The VAREFSEL control pin is used to select the reference voltage.

- 0 = Output internal voltage reference (2.56 V) to VAREF
- 1 = Input external voltage reference from VAREF and GNDREF

The ADC can be powered down independently of the FPGA core as an additional control or for power saving considerations, via the PWRDWN pin of the Analog Block.

Once the ADC has powered up and been released from reset, ADCRESET, the ADC will initiate a calibration routine designed to provide optimal ADC performance.

The Fusion ADC offers a robust calibration scheme to reduce integrated offset and linearity errors. The offset and linearity errors of the main capacitor array are compensated with an 8-bit calibration capacitor array.

The offset/linearity error calibration is carried out in two ways. First, a power-up calibration is carried out when the ADC comes out of reset. This is initiated by the CALIBRATE output of the Analog Block macro and is a fixed number of ADC_CLK cycles (3,840 cycles). In this mode, the linearity and offset errors of the capacitors are calibrated. Secondly, to compensate for drift and temperature-dependent effects, every conversion is followed by calibration of either the offset or a bit of the main capacitor array. The calibration procedure takes two additional ADC clock cycles. This ensures that over time and with temperature, the ADC remains consistent.

After both calibration and setting the appropriate configurations as explained above, the ADC is ready for operation. Driving the SAMPLE pin will cause the sample and hold circuit to capture the input of the channel as configured by the CHNUMBER[4:0] (see Table 2-36 on page 2-82). Subsequently driving the ADCSTART pin will initiate the conversion of the analog signal, and the BUSY signal will go high during the conversion process, letting the user know that the ADC is performing an operation. When the conversion is completed, the DATAVALID pin will go high (BUSY will go low), indicating that the digital result is available on the RESULT[11:0] pins.

Analog System Characteristics

Table 2-40 • **Electrical Specifications**

Parameter	Description	Condition	Min.	Typ.	Max.	Units
ADC						
V_{REFADC}	Reference Voltage	Internal Reference		2.560		V
		External Reference	2.527		V_{CC33A} + 0.05	V
t_{CONV}	Conversion Time	8-bit mode	1.67			uS
		10-bit mode	1.82			uS
		12-bit mode	2.00			uS
	Sample Rate[1]	8-bit mode			600	ksps
		10-bit mode			550	ksps
		12-bit mode			500	ksps
All Analog Inputs (Direct Input)						
V_{INAD}	Input Voltage		–0.2		≤ VREF	V
C_{INAD}	Input Capacitance	Channel not selected		7		pF
		Channel selected but not sampling		8		pF
		Channel selected and sampling		18		pF
TUE	Total Unadjusted Error (external reference)	8-bit mode		2		LSB
		10-bit mode		4		LSB
		12-bit mode		6		LSB
Z_{INAD}	Input Impedance	8-bit mode		2		kΩ
		10-bit mode		2		kΩ
		12-bit mode		2		kΩ
All Analog Inputs (Using Pre-Scaler)						
V_{INAP}	Input Voltage[2]		–12		12	V
	Accuracy	Positive DC Inputs		1		%
		Negative DC Inputs		2		%
	Offset			2 ± 0.2% of range		mV
	Bandwidth		100			kHz
Z_{INAP}	Impedance (2, 4, 8, and 12-Volt ranges)		1			MΩ
	Scaling Factor	Pre-Scaler Modes (Table 2-35 on page 2-81)				

Notes:

1. *The Sample Rate is time-shared among active analog inputs.*
2. *The input voltage range for the Temperature Monitor Block Pre-Scaler is 0 to 12 V.*
3. *VRSM is the maximum voltage drop across the current sense resistor.*

Table 2-40 • **Electrical Specifications (Continued)**

Parameter	Description	Condition	Min.	Typ.	Max.	Units
	Settling Time	To 0.1% of final value			10	µs
Current Monitor						
V_{RSM}	Maximum Differential Input				V_{REFADC}/10	mV
	Resolution		1			mV
	Common Mode Range		–12		12	V
	Gain			10		
C_{MRR}	Common mode rejection ratio	DC – 1 kHz		60		dB
		1 kHz – 10 kHz		50		dB
		> 10 kHz		30		dB
	Pole			100		kHz
V_{MPWC}	Strobe	Minimum Pulse Width	10			µs
Temperature Monitor						
	Resolution			1		°C
	Accuracy			5	+/- 10	°C
V_{MPWT}	Strobe	Minimum Pulse Width	10			µs
Analog Input as a Digital Input						
V_{IND}	Input Voltage		–0.2		AVDD + 0.2	V
V_{HYSDIN}	Hysteresis			0.3		V
V_{IHDIN}	Input High			1.2		V
V_{ILDIN}	Input Low			0.9		V
V_{MPWDIN}	Minimum Pulse Width		100			nS
I_{STBDIN}	Standby Current				20	nA
I_{DYNDIN}	Dynamic Current				20	µA
t_{INDIN}	Input Delay			10		nS
Analog Output Pad (G Pad)						
V_G	Voltage Range		–12		12	V
I_G	Minimum Output Current Drive	High Current Mode at 1.0 V		25		mA
		Low Current Mode—1 µA		1		µA
		Low Current Mode—3 µA		3		µA
		Low Current Mode—10 µA		10		µA
		Low Current Mode—30 µA		30		µA
I_{OFFG}	Maximum Off Current			100		µA

Notes:

1. *The Sample Rate is time-shared among active analog inputs.*
2. *The input voltage range for the Temperature Monitor Block Pre-Scaler is 0 to 12 V.*
3. *VRSM is the maximum voltage drop across the current sense resistor.*

Analog Configuration MUX

The Analog Configuration MUX (ACM) is the interface between the FPGA, the Analog Block configurations, and the real-time counter. The Actel Libero IDE Tool will generate IPs that will load and configure the Analog Block via the ACM. However, users are not limited to only using the Libero IDE IP. This section provides a detailed description of the ACM's register map, truth tables for proper configuration of the Analog Block and RTC, as well as timing waveforms so users can access and control the ACM directly from their designs.

The Analog Block contains four 8-bit latches per Analog Quad that are initialized through the ACM. These latches act as configuration bits for Analog Quads. The ACM block runs from the core voltage supply (1.5 V).

Access to the ACM is achieved via 8-bit address and data buses with enables. The pin list is provided in Table 2-34 on page 2-67. The ACM clock speed is limited to a maximum of 10 MHz operation, more than sufficient to handle the low bandwidth requirements of configuring the Analog Block and the RTC (sub-block of the Analog Block).

Table 2-41 decodes the ACM address space and maps it to the corresponding Analog Quad and configuration byte for that quad.

Table 2-41 • **ACM Pin List**

Symbol	Type	Function
ACMWDATA[7:0]	Digital Input	Write data input from FPGA
ACMRDATA[7:0]	Digital Output	Read data to FPGA
ACMADDRESS[7:0]	Digital Input	Address input from FPGA
ACMWEN	Digital Input	Write enable from FPGA
ACMCLK	Digital Input	Clock input from FPGA
ACMRESET	Digital Input	Asynchronous reset from FPGA

ACM Characteristics[1]

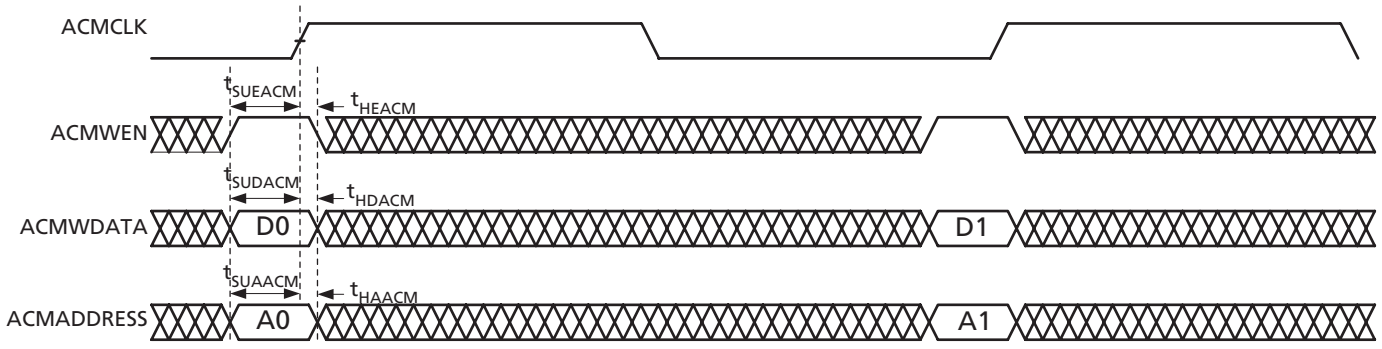


Figure 2-73 • **ACM Write Waveform**

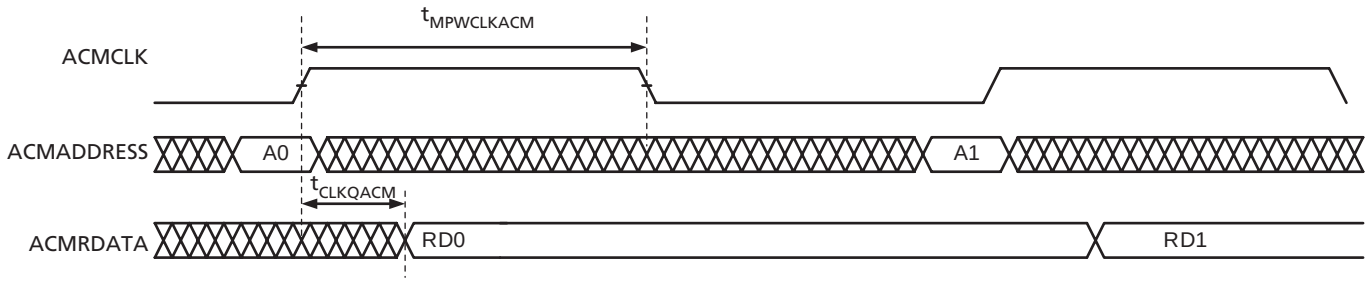


Figure 2-74 • **ACM Read Waveform**

Timing Characteristics

Table 2-42 • **Analog Configuration Multiplexer (ACM) Timing**
Commercial-Case Conditions: T_J = 25°C, Typical Case, V_{CC} = 1.5 V

Parameter	Description	Min.	Typ.	Max.	Units
$t_{CLKQACM}$	Clock-to-Q of the ACM	10			ns
t_{SUDACM}	Data Setup time for the ACM	10			ns
t_{HDACM}	Data Hold time for the ACM	0			ns
t_{SUAACM}	Address Setup time for the ACM	10			ns
t_{HAACM}	Address Hold time for the ACM	0			ns
t_{SUEACM}	Enable Setup time for the ACM	10			ns
t_{HEACM}	Enable Hold time for the ACM	0			ns
$t_{MPWARACM}$	Asynchronous Reset Minimum Pulse Width for the ACM	10			ns
$t_{REMARACM}$	Asynchronous Reset Removal time for the ACM	10			ns
$t_{RECARACM}$	Asynchronous Reset Recovery time for the ACM	10			ns
$t_{MPWCLKACM}$	Clock Minimum Pulse Width for the ACM	50			ns

1. *When addressing the RTC addresses (i.e., ACMADDR 64 to 89), there is no timing generator, and the rc_osc, byte_en, and aq_wen signals have no impact.*

Analog Quad ACM Description

Table 2-43 maps out the Analog Configuration MUX (ACM) space associated with configuration of the Analog Quads within the Analog Block. Table 2-43 shows the byte assignment within each quad and function of each bit within each byte. Subsequent tables will explain each bit setting and how that corresponds to a particular configuration. After 3.3 V and 1.5 V is applied to Fusion, analog quad configuration registers are loaded with default setting until initialization and configuration state machine changes it to user defined setting.

Table 2-43 • **Analog Quad ACM Byte Assignment**

Byte	Bit	Signal (Bx)	Function	Default Setting
Byte 0 (AV)	0	B0[0]	Scaling factor control – pre-scaler	Highest voltage Range
	1	B0[1]		
	2	B0[2]		
	3	B0[3]	Analog MUX select	Pre-Scaler
	4	B0[4]	Current monitor switch	Off
	5	B0[5]	Direct analog input switch	Off
	6	B0[6]	Selects V-pad polarity	Positive
	7	B0[7]	pre-scaler op-amp mode	Power-down
Byte 1 (AC)	0	B1[0]	Scaling factor control – pre-scaler	Highest voltage range
	1	B1[1]		
	2	B1[2]		
	3	B1[3]	Analog MUX select	Pre-Scaler
	4	B1[4]		
	5	B1[5]	Direct analog input switch	Off
	6	B1[6]	Selects C-pad polarity	Positive
	7	B1[7]	Pre-scaler op-amp mode	Power-down
Byte 2 (AG)	0	B2[0]	Chip temperature monitor	Off
	1	B2[1]	Spare	–
	2	B2[2]	Current drive control	Lowest current
	3	B2[3]		
	4	B2[4]	Spare	–
	5	B2[5]	Spare	–
	6	B2[6]	Selects G-pad polarity	Positive
	7	B2[7]	Selects low/high drive	Low drive
Byte 3 (AT)	0	B3[0]	Scaling factor control – pre-scaler	Highest voltage range
	1	B3[1]		
	2	B3[2]		
	3	B3[3]	Analog MUX select	Pre-Scaler
	4	B3[4]		
	5	B3[5]	Direct analog input switch	Off
	6	B3[6]	Selects T-pad polarity	Positive
	7	B3[7]	Pre-scaler op-amp mode	Power-down

Table 2-44 details the settings available to control the pre-scaler values of the AV, AC, and AT pins. Note that the AT pin has a reduced number of available pre-scaler values.

Table 2-44 • **Pre-Scaler Control Truth Table (AV (x = 0), AC (x = 1), and AT (x = 3))**

Control Lines Bx[2:0]	Scaling Factor Pad to ADC Input	LSB for an 8-Bit Conversion (mV)	LSB for a 10-Bit Conversion (mV)	LSB for a 12-Bit Conversion (mV)	Full Scale Voltage	Range Name
000*	0.15625	64	16	4	16.368 V	16 V
001	0.3125	32	8	2	8.184 V	8 V
010*	0.625	16	4	1	4.092 V	4 V
011	1.25	8	2	0.5	2.046 V	2 V
100	2.5	4	1	0.25	1.023 V	1 V
101	5.0	2	0.5	0.125	0.5115 V	0.5 V
110	10.0	1	0.25	0.0625	0.25575 V	0.25 V
111	20.0	0.5	0.125	0.03125	0.127875 V	0.125 V

Note: **These are the only valid ranges for the Temperature Monitor Block Pre-Scaler.*

Table 2-45 details the settings available to control the MUX within each of the AV, AC, and AT circuits. This MUX determines whether the signal routed to the ADC is the direct analog input, prescaled signal, or output of either current monitor or temperature monitor blocks.

Table 2-45 • **Analog Multiplexer Truth Table (AV (x = 0), AC (x = 1), and AT (x = 3))**

Control Lines Bx[4]*	Control Lines Bx[3]	ADC Connected To
0	0	Pre-scaler
0	1	Direct input
1	0	Current amplifier/ Temperature Monitor
1	1	Not valid

Note: **This pin is not available for the Voltage Monitor Block.*

Table 2-46 details the settings available to control the Direct Analog Input switch for the AV, AC, and ACT pins.

Table 2-46 • **Direct Analog Input Switch Control Truth Table (AV (x = 0), AC (x = 1), and AT (x = 3))**

Control Lines Bx[5]	Direct Input Switch
0	Off
1	On

Table 2-47 details the settings available to control the polarity of the signals coming to the AV, AC, and AT pins. Note that the only valid setting for the AT pin is logic 0 to support positive voltages.

Table 2-47 • **Voltage Polarity Control Truth Table (AV (x = 0), AC (x = 1), and AT (x = 3)*)**

Control Lines Bx[6]	Input Signal Polarity
0	Positive
1	Negative

Note: **The B3[6] signal for the AT pad should be kept at a logic level 0 to accept only positive voltages.*

Table 2-48 details the settings available to either power down or enable the pre-scaler associated with the analog inputs AV, AC, and AT.

Table 2-48 • **Pre-Scaler Op-Amp Power-Down Truth Table (AV (x = 0), AC (x = 1), and AT (x = 3))**

Control Lines Bx[7]	Pre-Scaler Op-Amp
0	Power-down
1	Operational

Table 2-49 details the settings available to enable the current monitor block associated with the AC pin.

Table 2-49 • **Current Monitor Input Switch Control Truth Table (AV (x = 0))**

Control Lines B0[4]	Current Monitor Input Switch
0	Off
1	On

Table 2-50 details the settings available to configure the drive strength of the gate drive when not in high drive mode.

Table 2-50 • **Low Drive Gate Driver Current Truth Table (AG)**

Control Lines B2[3]	Control Lines B2[2]	Current (µA)
0	0	1
0	1	3
1	0	10
1	1	30

Table 2-51 details the settings available to set the polarity of the gate driver (either P-channel or N-Channel type devices).

Table 2-51 • **Gate Driver Polarity Truth Table (AG)**

Control Lines B2[6]	Gate Driver Polarity
0	Positive
1	Negative

Table 2-52 details the settings available to turn on the Gate Driver and set whether the high drive mode is on or off.

Table 2-52 • **Gate Driver Control Truth Table (AG)**

Control Lines B2[7]	GDON	Gate Driver
0	0	Off
0	1	Low drive on
1	0	Off
1	1	High drive on

User I/Os

Introduction

Fusion devices feature a flexible I/O structure, supporting a range of mixed voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V) through a bank-selectable voltage. Table 2-54, Table 2-55, Table 2-56, and Table 2-57 on page 2-96 show the voltages and the compatible I/O standards. I/Os provide programmable slew rates, drive strengths, weak pull-up, and weak pull-down circuits. 3.3 V PCI and 3.3 V PCI-X are 5 V tolerant. See the "5 V Input Tolerance" section on page 2-105 for possible implementations of 5 V tolerance.

All I/Os are in a known state during power-up and any power-up sequence is allowed without current impact. Refer to the "I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)" section on page 3-3 for more information.

I/O Tile

The Fusion I/O tile provides a flexible, programmable structure for implementing a large number of I/O standards. In addition, the registers available in the I/O tile in selected I/O banks can be used to support high-performance register inputs and outputs, with register enable if desired (Figure 2-75 on page 2-94). The registers can also be used to support the JESD-79C Double Data Rate (DDR) standard within the I/O structure (see the "Double Data Rate (DDR) Support" section on page 2-100 for more information).

As depicted in Figure 2-76 on page 2-99, all I/O registers share one CLR port. The output register and output enable register share one CLK port. Refer to the "I/O Registers" section on page 2-99 for more information.

I/O Banks and I/O Standards Compatibility

The digital I/Os are grouped into I/O voltage banks. There are three digital I/O banks on the AFS090 and AFS250 devices and four digital I/O banks on the AFS600 and AFS1500 devices. Figure 2-89 on page 2-118 and Figure 2-90 on page 2-119 show the bank configuration by device. The north side of I/O in the AFS600 and AFS1500 devices is comprised of two banks of Actel Pro I/Os. The Actel Pro I/Os support a wide number of voltage referenced I/O standards in addition to the multitude of single-ended and differential I/O standards common throughout all of the Actel digital I/Os. Each I/O voltage bank has dedicated input/output supply and ground voltages (VMV/GNDQ for input buffers and V_{CCI}/GND for output buffers). Because of these dedicated supplies, only I/Os with compatible standards can be assigned to the same I/O voltage bank. Table 2-55 and Table 2-56 on page 2-95 show the required voltage compatibility values for each of these voltages.

For more information about I/O and global assignments to I/O banks, refer to the specific pin table of the device in the "Package Pin Assignments" section on page 4-1 and the "User I/O Naming Convention" section on page 2-118.

Each Pro I/O bank is divided into minibanks. Any user I/O in a V_{REF} minibank (a minibank is the region of scope of a V_{REF} pin) can be configured as a V_{REF} pin (Figure 2-75 on page 2-94). Only one V_{REF} pin is needed to control the entire V_{REF} minibank. The location and scope of the V_{REF} minibanks can be determined by the I/O name. For details, see the "User I/O Naming Convention" section on page 2-118.

Table 2-56 on page 2-95 shows the I/O standards supported by the Fusion devices and the corresponding voltage levels.

I/O standards are compatible if:

- Their V_{CCI} and VMV values are identical
- If both of the standards need a V_{REF}, their V_{REF} values must be identical (Pro I/O only)

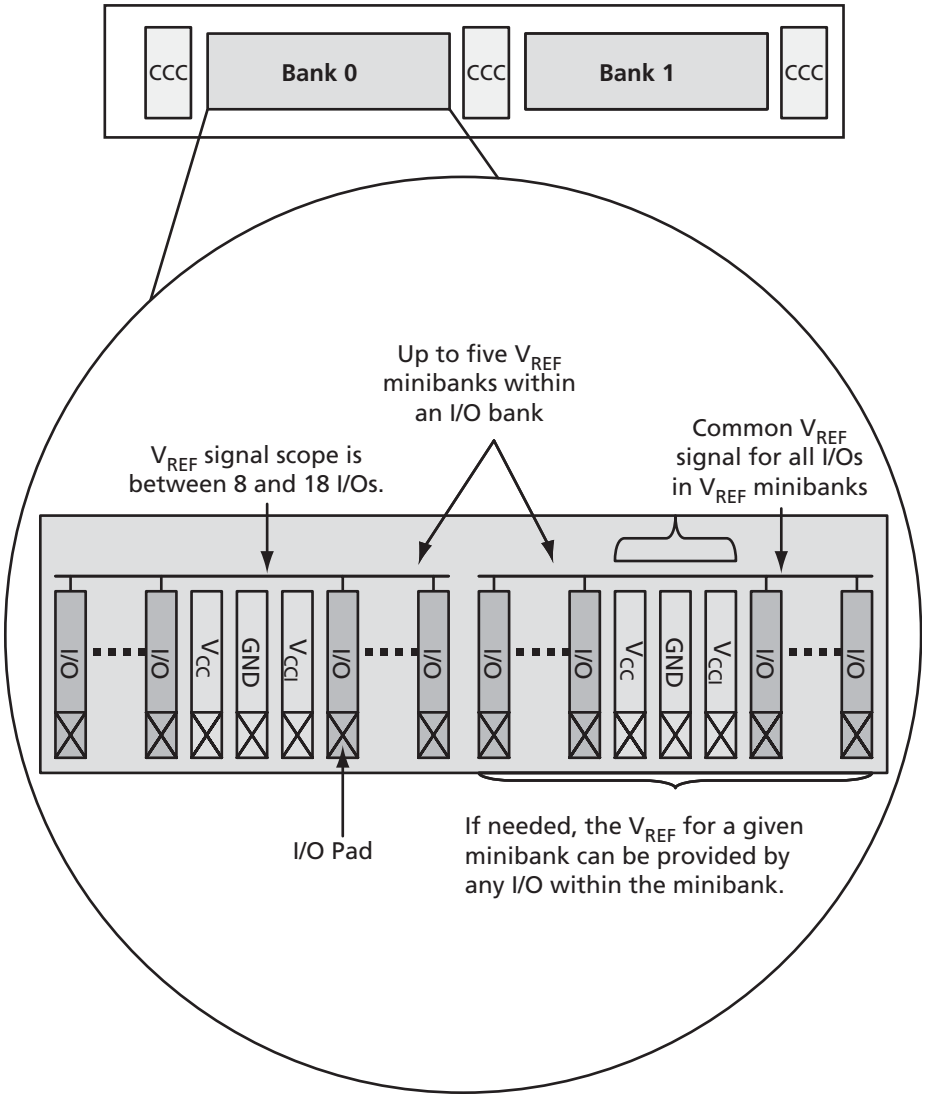


Figure 2-75 • **Fusion Pro I/O Bank Detail Showing V_{REF} Minibanks (north side of AFS600 and AFS1500)**

Table 2-53 • **I/O Standard Supported by Bank Type**

I/O Bank	Single-Ended I/O Standard	Differential I/O Standard	Voltage-Referenced	Hot-Swap
Hot-Swap	LVTTL/LVCMOS 3.3 V, LVCMOS 2.5 V/1.8 V/ 1.5 V, LVCMOS2.5/5.0 V	–	–	Yes
LVDS	LVTTL/LVCMOS 3.3 V, LVCMOS 2.5 V/1.8 V/ 1.5 V, LVCMOS2.5/5.0 V, 3.3 V PCI/3.3 V PCI-X	LVPECL and LVDS	–	–
Pro I/O	LVTTL/LVCMOS 3.3 V, LVCMOS 2.5 V/1.8 V/ 1.5 V, LVCMOS2.5/5.0 V, 3.3 V PCI/3.3 V PCI-X	LVPECL and LVDS	GTL+ 2.5 V / 3.3 V, GTL 2.5 V / 3.3 V, HSTL Class I and II, SSTL2 Class I and II, SSTL3 Class I and II	Yes

Table 2-54 • **I/O Bank Support by Device**

I/O Bank	AFS090	AFS250	AFS600	AFS1500
Hot-Swap	N	N	–	–
LVDS, BLVDS, M-LVDS	E, W	E, W	E, W	E, W
Pro I/O	–	–	N	N
Analog Quad	S	S	S	S

Note: *E = East side of the device*
W = West side of the device
N = North side of the device
S = South side of the device

Table 2-55 • **Fusion V_{CCI} Voltages and Compatible Standards**

V_{CCI} and VMV (typical)	Compatible Standards
3.3 V	LVTTL/LVCMOS 3.3, PCI 3.3, SSTL3 (Class I and II)*, GTL+ 3.3, GTL 3.3*, LVPECL
2.5 V	LVCMOS 2.5, LVCMOS 2.5/5.0, SSTL2 (Class I and II)*, GTL+ 2.5*, GTL 2.5*, LVDS, BLVDS, M-LVDS
1.8 V	LVCMOS 1.8
1.5 V	LVCMOS 1.5, HSTL (Class I)*, HSTL (Class II)*

Note: **I/O standard supported by Pro I/O banks.*

Table 2-56 • **Fusion V_{REF} Voltages and Compatible Standards***

V_{REF} (typical)	Compatible Standards
1.5 V	SSTL3 (Class I and II)
1.25 V	SSTL2 (Class I and II)
1.0 V	GTL+ 2.5, GTL+ 3.3
0.8 V	GTL 2.5, GTL 3.3
0.75 V	HSTL (Class I), HSTL (Class II)

Note: **I/O standard supported by Pro I/O banks.*

Table 2-57 • **Fusion Standard and LVDS I/O Features**

I/O Bank Voltage (typical)	Minibank Voltage (typical)	LVTTL/LVCMOS 3.3 V	LVCMOS 2.5 V	LVCMOS 1.8 V	LVCMOS 1.5 V	3.3 V PCI / PCI-X	GTL + (3.3 V)	GTL + (2.5 V)	GTL (3.3 V)	GTL (2.5 V)	HSTL Class I and II (1.5 V)	SSTL2 Class I and II (2.5 V)	SSTL3 Class I and II (3.3 V)	LVDS (2.5 V ± 5%)	LVPECL (3.3 V)
3.3 V	–														
	0.80 V														
	1.00 V														
	1.50 V														
2.5 V	–														
	0.80 V														
	1.00 V														
	1.25 V														
1.8 V	–														
1.5 V	–														
	0.75 V														

Note: *White box: Allowable I/O standard combinations.*
Gray box: Illegal I/O standard combinations.

Features Supported on Every I/O

Table 2-58 lists all features supported by transmitter/receiver for single-ended and differential I/Os.

Table 2-58 • **Fusion Pro I/O Features**

Feature	Description
Single-ended and voltage-referenced transmitter features	• Hot insertion in every mode except PCI or 5 V input tolerant (these modes use clamp diodes and do not allow hot insertion) • Activation of hot insertion (disabling the clamp diode) is selectable by I/Os • Weak pull-up and pull-down • Two slew rates • Skew between output buffer enable/disable time: 2 ns delay (rising edge) and 0 ns delay (falling edge) (see "Selectable Skew Between Output Buffer Enable/Disable Time" on page 2-110 for more information) • Five drive strengths • 5 V tolerant receiver ("5 V Input Tolerance" section on page 2-105) • LVTTL/LVCMOS 3.3 V outputs compatible with 5 V TTL inputs ("5 V Output Tolerance" section on page 2-108) • High Performance (Table 2-62 on page 2-104)
Single-ended receiver features	• Schmitt trigger option • ESD protection • Programmable Delay: 0 ns if bypassed, 0.46 ns with 000 setting, 4.66 ns with 111 setting, 0.6 ns intermediate delay increments (at 25°C, 1.5 V) • High performance (Table 2-62 on page 2-104) • Separate ground and power planes, GNDQ/VMV, for input buffers only to avoid output-induced noise in the input circuitry
Voltage-referenced differential receiver features	• Programmable Delay: 0 ns if bypassed, 0.46 ns with 000 setting, 4.66 ns with 111 setting, 0.6 ns intermediate delay increments (at 25°C, 1.5 V) • High performance (Table 2-62 on page 2-104) • Separate ground and power plane, GNDQ, and VMV pins for input buffers only to avoid output-induced noise in the input circuitry
CMOS-style LVDS, BLVDS, M-LVDS, or LVPECL transmitter	• Two I/Os and external resistors are used to provide a CMOS style LVDS, BLVDS, M-LVDS, or LVPECL transmitter solution. • Activation of hot insertion (disabling the clamp diode) is selectable by I/Os • Weak pull-up and pull-down • Fast slew rate
LVDS/LVPECL differential receiver features	• ESD protection • High performance (Table 2-62 on page 2-104) • Programmable Delay: 0 ns if bypassed, 0.46 ns with 000 setting, 4.66 ns with 111 setting, 0.6 ns intermediate delay increments (at 25°C, 1.5 V) • Separate input buffer ground and power planes to avoid output-induced noise in the input circuitry

Table 2-59 • **Maximum I/O Frequency for Single-Ended, Voltage-Referenced, and Differential I/Os**

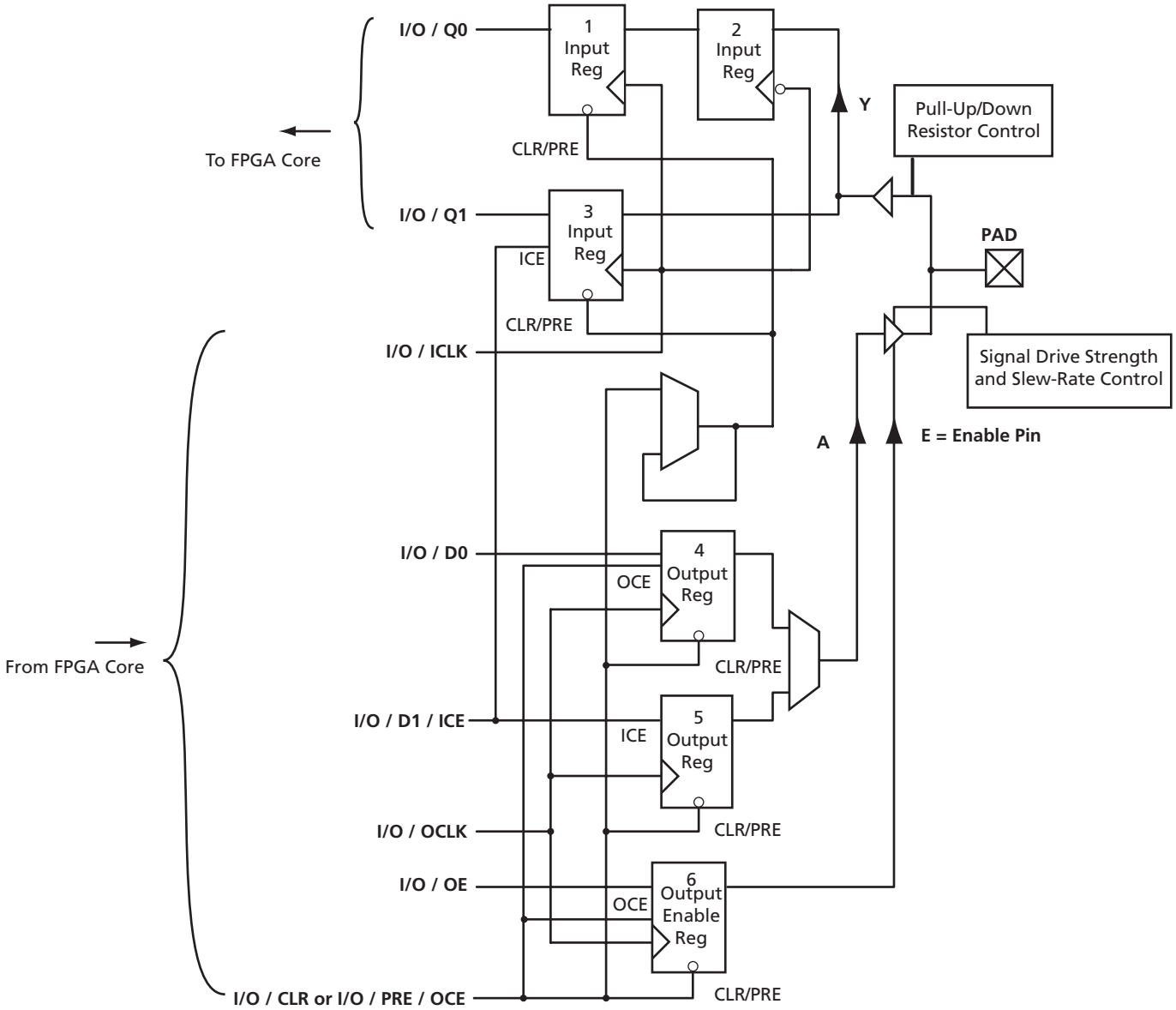
Specification	Performance Up To
LVTTL/LVCMOS 3.3 V	200 MHz
LVCMOS 2.5 V	250 MHz
LVCMOS 1.8 V	200 MHz
LVCMOS 1.5 V	130 MHz
PCI	200 MHz
PCI-X	200 MHz
HSTL-I	300 MHz
HSTL-II	300 MHz
SSTL2-I	300 MHz
SSTL2-II	300 MHz
SSTL3-I	300 MHz
SSTL3-II	300 MHz
GTL+ 3.3 V	300 MHz
GTL+ 2.5 V	300 MHz
GTL 3.3 V	300 MHz
GTL 2.5 V	300 MHz
LVDS	350 MHz
BLVDS	200 MHz
M-LVDS	200 MHz
LVPECL	300 MHz

I/O Registers

Each I/O module contains several input, output, and enable registers. Refer to Figure 2-76 for a simplified representation of the I/O block.

The number of input registers is selected by a set of switches (not shown in Figure 2-76) between registers to implement single or differential data transmission to and from the FPGA core. The Designer software sets these switches for the user.

A common CLR/PRE signal is employed by all I/O registers when I/O register combining is used. Input Register 2 does not have a CLR/PRE pin, as this register is used for DDR implementation. The I/O registers combining must satisfy some rules.



Note: *Fusion I/Os have registers to support DDR functionality (see the "Double Data Rate (DDR) Support" section on page 2-100 for more information).*

Figure 2-76 • **I/O Block Logical Representation**

Double Data Rate (DDR) Support

Fusion Pro I/Os support 350 MHz DDR inputs and outputs. In DDR mode, new data is present on every transition of the clock signal. Clock and data lines have identical bandwidths and signal integrity requirements, making it very efficient for implementing very high-speed systems.

DDR interfaces can be implemented using HSTL, SSTL, LVDS, and LVPECL I/O standards. In addition, high-speed DDR interfaces can be implemented using LVDS I/O.

Input Support for DDR

The basic structure to support a DDR input is shown in Figure 2-77. Three input registers are used to capture incoming data, which is presented to the core on each rising edge of the I/O register clock.

Each I/O tile on Fusion devices supports DDR inputs.

Output Support for DDR

The basic DDR output structure is shown in Figure 2-78 on page 2-101. New data is presented to the output every half clock cycle. Note: DDR macros and I/O registers do not require additional routing. The combiner automatically recognizes the DDR macro and pushes its registers to the I/O register area at the edge of the chip. The routing delay from the I/O registers to the I/O buffers is already taken into account in the DDR macro.

Refer to the Actel application note *Using DDR for Fusion Devices* for more information.

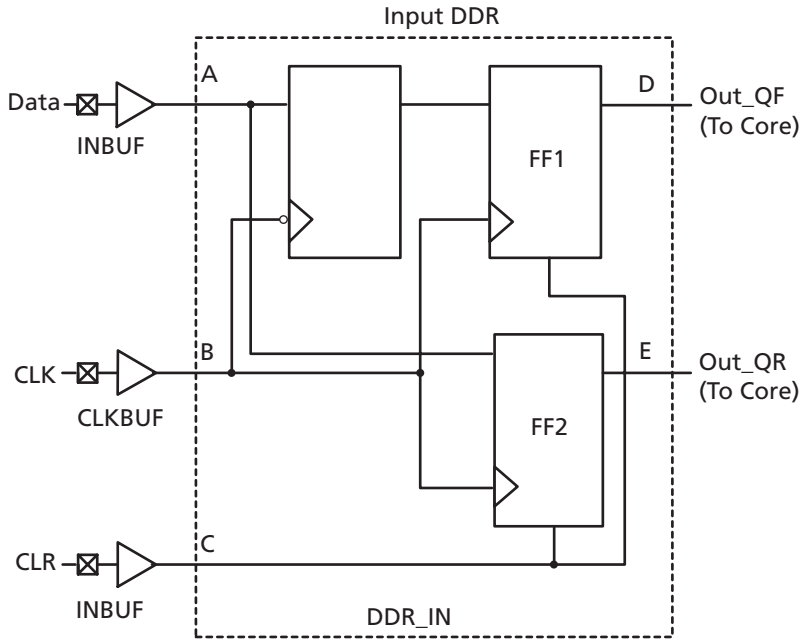


Figure 2-77 • **DDR Input Register Support in Fusion Devices**

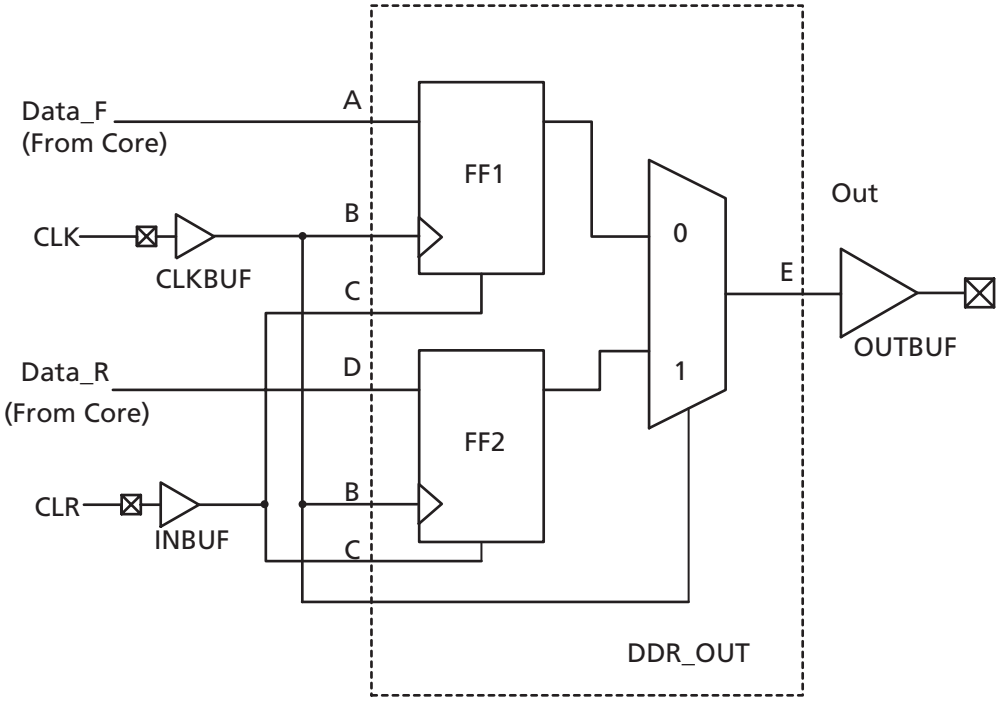


Figure 2-78 • **DDR Output Support in Fusion Devices**

Hot-Swap Support

Hot-swapping (also called hot plugging) is the operation of hot insertion or hot removal of a card in (or from) a powered-up system. The levels of hot-swap support and examples of related applications are described in Table 2-60. The I/Os also need to be configured in hot insertion mode if hot plugging compliance is required.

Table 2-60 • **Levels of Hot-Swap Support**

Hot Swapping Level	Description	Power Applied to Device	Bus State	Card Ground Connection	Device Circuitry Connected to Bus Pins	Example of Application with Cards that Contain Fusion Devices	Compliance of Fusion Devices
1	Cold-Swap	No	–	–	–	System and card with Actel FPGA chip are powered down, then the card gets plugged into the system, then the power supplies are turned on for the system but not for the FPGA on the card.	Compliant I/Os can but do not have to be set to hot-insertion mode.
2	Hot-Swap while reset	Yes	Held in reset state	Must be made and maintained for 1 msec before, during, and after insertion/ removal	–	In PCI hot-plug specification, Reset control circuitry isolates the card busses until the card supplies are at their nominal operating levels and stable.	Compliant I/Os can but do not have to be set to hot-insertion mode.
3	Hot-Swap while bus idle	Yes	Held idle (no ongoing I/O processes during insertion/ removal)	Same as Level 2	Must remain glitch-free during power- up or power-down	Board bus shared with card bus is "frozen," and there is no toggling activity on the bus,. It is critical that the logic states set on the bus signal do not get disturbed during card insertion/removal.	Compliant with cards with two levels of staging. I/Os have to be set to hot-insertion mode.
4	Hot-Swap on an active bus	Yes	Bus may have active I/O processes ongoing, but device being inserted or removed must be idle	Same as Level 2	Same as Level 3	There is activity on the system bus, and it is critical that the logic states set on the bus signal do not get disturbed during card insertion/removal.	Compliant with cards with two levels of staging. I/Os have to be set to hot-insertion mode.

For Fusion devices requiring level 3 and/or level 4 compliance, the board drivers connected to Fusion I/Os need to have 10 kΩ (or lower) output drive resistance at hot insertion, and 1 kΩ (or lower) output drive resistance at hot removal. This resistance is the transmitter resistance sending signal towards the Fusion I/O and no additional resistance is needed on the board. If that cannot be assured, three levels of staging can be used to meet level 3 and/or level 4 compliance. Cards with two levels of staging should have the following sequence:

- Grounds
- Powers, I/Os, other pins

Cold-Sparing Support

Cold-sparing means that a subsystem with no power applied (usually a circuit board) is electrically connected to the system that is in operation. This means that all input buffers of the subsystem must present very high input impedance with no power applied so as not to disturb the operating portion of the system.

Fusion devices support cold-sparing for all I/O configurations. Configurations such as PCI standard requiring clamp diodes on the I/Os can also achieve cold-sparing compliance as the clamp diodes get disconnected internally when the supplies are at 0 V.

In designs where Fusion devices are expected to be cold-sparing compliant after supplies are turned off, a discharge resistor, switched resistor, or discharge path needs to be provided from each power supply to ground. If the resistor is chosen, the resistor value must be calculated based on decoupling capacitance on a given power supply on the board (this decoupling capacitor is in parallel with this resistor). The RC constant should ensure full discharge of supplies before cold-sparing functionality is required. The resistor is necessary to ensure that the power pins get discharged to ground every time there is an interruption of power supply on the device.

Electrostatic Discharge (ESD) Protection

Fusion devices are tested per JEDEC Standard JESD22-A114-B.

Fusion devices contain clamp diodes at every I/O, global, and power pad. Clamp diodes protect all device pads against damage from ESD as well as from excessive voltage transients.

Each I/O has two clamp diodes. One diode has its positive (P) side connected to the pad and its negative (N) side connected to V_{CCI}. The second diode has its P side connected to GND, and its N side connected to the pad. During operation, these diodes are normally biased in the Off state, except when transient voltage is significantly above V_{CCI} or below GND levels.

By selecting the appropriate I/O configuration, the diode is turned on or off. Refer to Table 2-61 for more information about the I/O standards and the clamp diode.

The second diode is always connected to the pad, regardless of the I/O configuration selected.

Table 2-61 • **Fusion Standard, LVDS, and Standard Plus Hot-Swap I/O Hot-Swap and 5 V Input Tolerance Capabilities**

I/O Assignment	Clamp Diode		Hot Insertion		5 V Input Tolerance[1]		Input Buffer	Output Buffer
	Standard Hot-Swap I/O	Standard and LVDS I/O	Standard Hot-Swap I/O	Standard and LVDS I/O	Standard Hot-Swap I/O	Standard and LVDS I/O		
3.3 V LVTTL/LVCMOS	No	Yes	Yes	No	Yes[1]	Yes[1]	Enabled/Disabled	
3.3 V PCI, 3.3 V PCI-X	N/A	Yes	N/A	No	N/A	Yes[1]	Enabled/Disabled	
LVCMOS 2.5 V	No	Yes	Yes	No	Yes[1]	Yes[2]	Enabled/Disabled	
LVCMOS 2.5 V / 5.0 V	No	Yes	Yes	No	Yes[1]	Yes[2]	Enabled/Disabled	
LVCMOS 1.8 V	No	Yes	Yes	No	No	No	Enabled/Disabled	
LVCMOS 1.5 V	No	Yes	Yes	No	No	No	Enabled/Disabled	
Differential, LVDS/BLVDS/ M-LVDS/ LVPECL [3]	N/A	Yes	N/A	No	N/A	No	Enabled/Disabled	

Notes:

1. *Can be implemented with an external IDT bus switch, resistor divider, or zener with resistor.*
2. *Can be implemented with an external resistor and an internal clamp diode.*
3. *Bidirectional LVPECL buffers are not supported. I/Os can either be configured as input buffers or output buffers.*

Table 2-62 • **Fusion Pro I/O Hot-Swap and 5 V Input Tolerance Capabilities**

I/O Assignment	Clamp Diode	Hot Insertion	5 V Input Tolerance	Input Buffer	Output Buffer
3.3 V LVTTL/LVCMOS	No	Yes	Yes[1]	Enabled/Disabled	
3.3 V PCI, 3.3 V PCI-X	Yes	No	Yes[1]	Enabled/Disabled	
LVCMOS 2.5 V [3]	No	Yes	No	Enabled/Disabled	
LVCMOS 2.5 V / 5.0 V [3]	Yes	No	Yes[2]	Enabled/Disabled	
LVCMOS 1.8 V	No	Yes	No	Enabled/Disabled	
LVCMOS 1.5 V	No	Yes	No	Enabled/Disabled	
Voltage-Referenced Input Buffer	No	Yes	No	Enabled/Disabled	
Differential, LVDS/BLVDS/M-LVDS/LVPECL[4]	No	Yes	No	Enabled/Disabled	

Notes:

1. *Can be implemented with an external IDT bus switch, resistor divider, or zener with resistor.*
2. *Can be implemented with an external resistor and an internal clamp diode.*
3. *In the SmartGen, FlashROM, Flash Memory System Builder, and Analog System Builder User's Guide, select the LVCMOS5 macro for the LVCMOS 2.5 V / 5.0 V I/O standard or the LVCMOS25 macro for the LVCMOS 2.5 V I/O standard.*
4. *Bidirectional LVPECL buffers are not supported. I/Os can either be configured as input buffers or output buffers.*

5 V Input Tolerance

I/Os can support 5 V input tolerance when LVTTL 3.3 V, LVCMOS 3.3 V, LVCMOS 2.5 V / 5 V, and LVCMOS 2.5 V configurations are used (see Table 2-63 on page 2-108 for more details). There are four recommended solutions (see Figure 2-79 to Figure 2-82 on page 2-108 for details of board and macro setups) to achieve 5 V receiver tolerance. All the solutions meet a common requirement of limiting the voltage at the I/O input to 3.6 V or less. In fact, the I/O absolute maximum voltage rating is 3.6 V, and any voltage above 3.6 V may cause long-term gate oxide failures.

Solution 1

The board-level design needs to ensure that the reflected waveform at the pad does not exceed the limits provided in Table 3-3 on page 3-2. This is a long-term reliability requirement.

This scheme will also work for a 3.3 V PCI / PCI-X configuration, but the internal diode should not be used for clamping, and the voltage must be limited by the two external resistors as explained below. Relying on the diode clamping would create an excessive pad DC voltage of 3.3 V + 0.7 V = 4 V.

Here are some examples of possible resistor values (based on a simplified simulation model with no line effects, and 10 Ω transmitter output resistance, where Rtx_out_high = ($V_{CCI} - V_{OH}$)/ I_{OH}, Rtx_out_low = V_{OL} / I_{OL}).

Example 1 (high speed, high current):

Rtx_out_high = Rtx_out_low = 10 Ω

R1 = 36 Ω (+/–5%), P(r1)min = 0.069 Ω

R2 = 82 Ω (+/–5%), P(r2)min = 0.158 Ω

Imax_tx = 5.5 V / (82 * 0.95 + 36 * 0.95 +10) = 45.04 mA

t_{RISE} = t_{FALL} = 0.85 ns at C_pad_load = 10 pF (includes up to 25% safety margin)

t_{RISE} = t_{FALL} = 4 ns at C_pad_load = 50 pF (includes up to 25% safety margin)

Example 2 (low-medium speed, medium current):

Rtx_out_high = Rtx_out_low = 10 Ω

R1 = 220 Ω (+/–5%), P(r1)min = 0.018 Ω

R2 = 390 Ω (+/–5%), P(r2)min = 0.032 Ω

Imax_tx = 5.5 V / (220 * 0.95 + 390 * 0.95 +10) = 9.17 mA

t_{RISE} = t_{FALL} = 4 ns at C_pad_load = 10 pF (includes up to 25% safety margin)

t_{RISE} = t_{FALL} = 20 ns at C_pad_load = 50 pF (includes up to 25% safety margin)

Other values of resistors are also allowed as long as the resistors are sized appropriately to limit the voltage at the receiving end to 2.5 V < Vin(rx) < 3.6 V* when the transmitter sends a logic '1'. This range of Vin_dc(rx) must be assured for any combination of transmitter supply (5 V +/- 0.5 V), transmitter output resistance, and board resistor tolerances.

Temporary overshoots are allowed according to Table 3-3 on page 3-2.

Solution 1

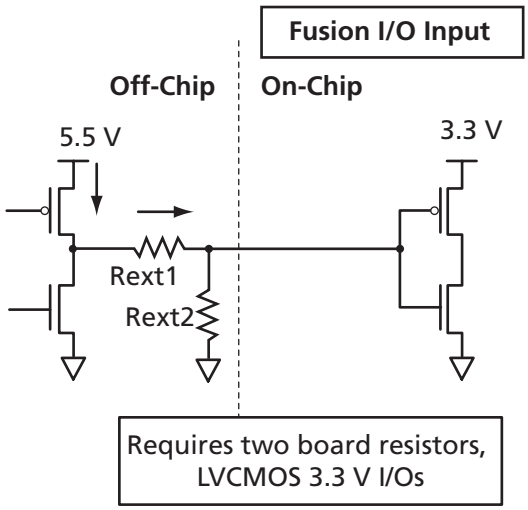


Figure 2-79 • **Solution 1**

Solution 2

The board-level design must ensure that the reflected waveform at the pad does not exceed limits provided in Table 3-3 on page 3-2. This is a long-term reliability requirement.

This scheme will also work for a 3.3 V PCI/PCIX configuration, but the internal diode should not be used for clamping, and the voltage must be limited by the external resistors and zener, as shown in Figure 2-80. Relying on the diode clamping would create an excessive pad DC voltage of 3.3 V + 0.7 V = 4 V.

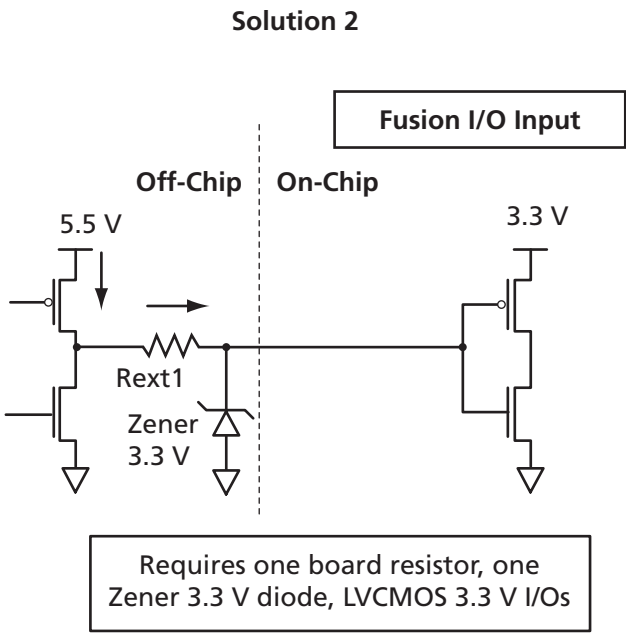


Figure 2-80 • **Solution 2**

Solution 3

The board-level design must ensure that the reflected waveform at the pad does not exceed limits provided in Table 3-3 on page 3-2. This is a long-term reliability requirement.

This scheme will also work for a 3.3 V PCI/PCIX configuration, but the internal diode should not be used for clamping, and the voltage must be limited by the bus switch, as shown in Figure 2-81. Relying on the diode clamping would create an excessive pad DC voltage of 3.3 V + 0.7 V = 4 V.

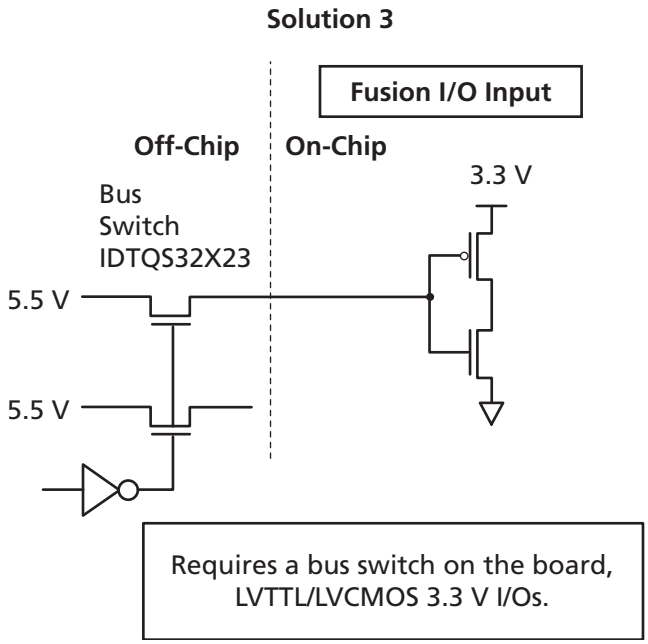


Figure 2-81 • **Solution 3**

Solution 4

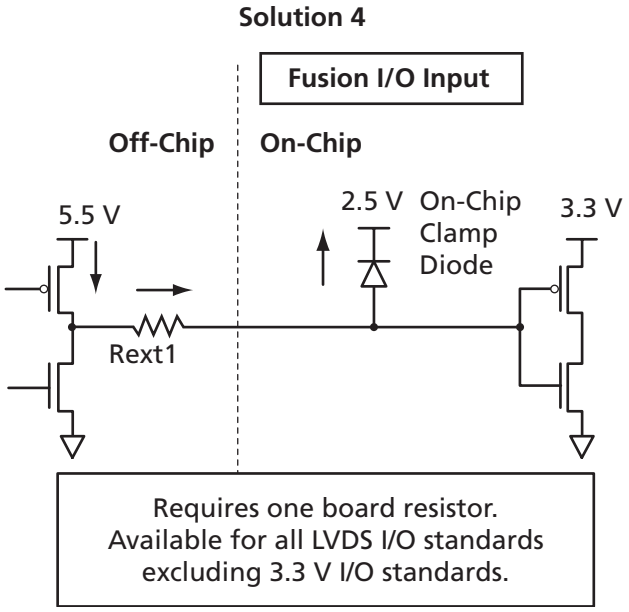


Figure 2-82 • **Solution 4**

Table 2-63 • **Comparison Table for 5-V-Compliant Receiver Scheme**

Scheme	Board Components	Speed	Current Limitations
1	Two resistors	Low to High[1]	Limited by transmitter's drive strength
2	Resistor and Zener 3.3 V	Medium	Limited by transmitter's drive strength
3	Bus switch	High	N/A
4	Minimum resistor value[2] • R = 47 Ω at T_J = 70°C • R = 150 Ω at T_J = 85°C • R = 420 Ω at T_J = 100°C	Medium	Maximum diode current at 100% duty cycle, signal constantly at "1" • 52.7 mA at T_J =70°C / 10-year lifetime • 16.5 mA at T_J = 85°C / 10-year lifetime • 5.9 mA at T_J = 100°C / 10-year lifetime For duty cycles other than 100%, the currents can be increased by a factor = 1/duty cycle Example: 20% duty cycle at 70°C Maximum current = (1/0.2) * 52.7 mA = 5 * 52.7 mA = 263.5 mA

Notes:

1. *Speed and current consumption increase as the board resistance values decrease.*
2. *Resistor values ensure I/O diode long term reliability.*

5 V Output Tolerance

Fusion I/Os must be set to 3.3 V LVTTL or 3.3 V LVCMOS mode to reliably drive 5 V TTL receivers. It is also critical that there be NO external I/O pull-up resistor to 5 V, since this resistor would pull the I/O pad voltage beyond the 3.6 V absolute maximum value, and consequently cause damage to the I/O.

When set to 3.3 V LVTTL or 3.3 V LVCMOS mode, Fusion I/Os can directly drive signals into 5 V TTL receivers. In fact, V_{OL} = 0.4 V and V_{OH} = 2.4 V in both 3.3 V LVTTL and 3.3 V LVCMOS modes exceed the V_{IL} = 0.8 V and V_{IH} = 2 V level requirements of 5 V TTL receivers. Therefore, level '1' and level '0' will be recognized correctly by 5 V TTL receivers.

Simultaneous Switching Outputs and Printed Circuit Board Layout

Simultaneously switching outputs (SSO) can produce signal integrity problems on adjacent signals that are not part of SSO bus. Both inductive and capacitive coupling parasitics of bond wires inside packages and of traces on PCB boards will transfer noise from SSO busses onto signals adjacent to those busses. Additionally, SSOs can produce ground bounce noise and V_{CCI} dip noise. These two noise types are caused by rapidly changing currents through GND and V_{CCI} package pin inductances during switching activities:

- Ground bounce noise voltage = L (GND) * di/dt
- V_{CCI} dip noise voltage = L (V_{CCI}) * di/dt

Any group of four or more input pins switching on the same clock edge is considered an SSO bus. The shielding should be done both on the board and inside the package unless otherwise described.

In-package shielding can be achieved in several ways; the required shielding will vary depending on whether pins next to SSO bus are LVTTL/LVCMOS inputs, LVTTL/LVCMOS outputs, or GTL/SSTL/HSTL/LVDS/LVPECL inputs and outputs. Board traces in the vicinity of the SSO bus have to be adequately shielded from mutual coupling and inductive noise that can be generated by SSO bus. Also, noise generated by SSO bus needs to be reduced inside the package.

Printed circuit boards (PCB) perform an important function in feeding stable supply voltage to the IC and at the same time maintain signal integrity between devices.

Key issues that need to considered are:

- Power and Ground plane design and decoupling network design
- Transmission Line Reflections and Terminations

Selectable Skew Between Output Buffer Enable/Disable Time

The configurable skew block is used to delay the output buffer assertion (enable) without affecting deassertion (disable) time.

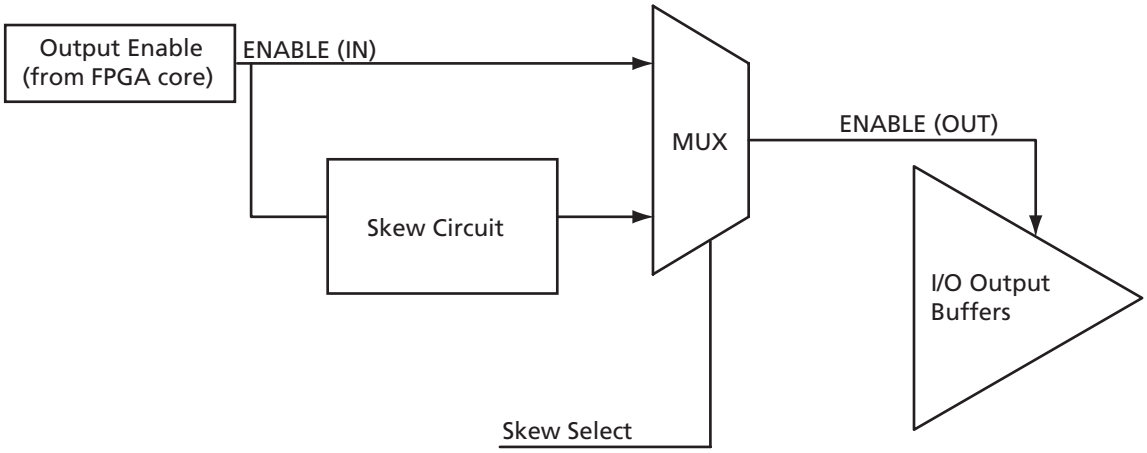


Figure 2-83 • **Block Diagram of Output Enable Path**

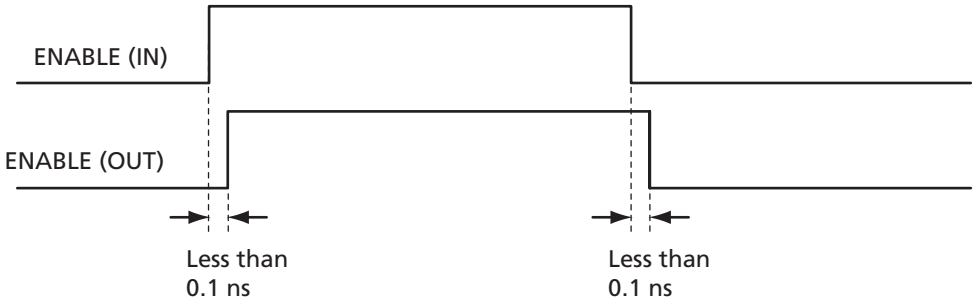


Figure 2-84 • **Timing Diagram (Option1: Bypasses Skew Circuit)**

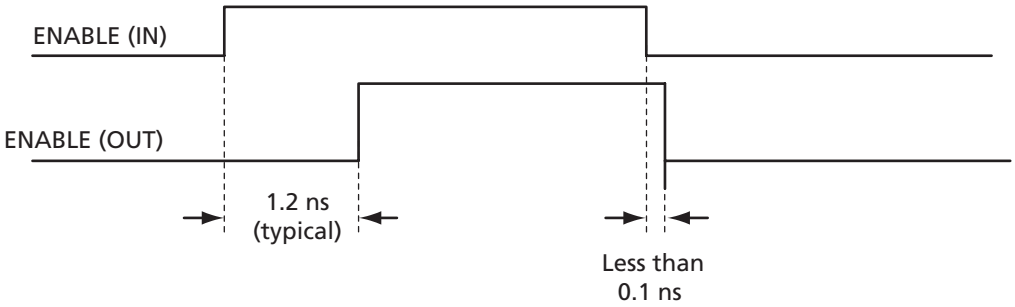


Figure 2-85 • **Timing Diagram (Option 2: Enables Skew Circuit)**

At the system level, the skew circuit can be used in applications where transmission activities on bidirectional data lines need to be coordinated. This circuit, when selected, provides a timing margin that can prevent bus contention and subsequent data loss and/or transmitter overstress due to transmitter-to-transmitter current shorts. Figure 2-86 presents an example of the skew circuit implementation in a bidirectional communication system. Figure 2-87 shows how bus contention is created, and Figure 2-88 on page 2-112 shows how it can be avoided with the skew circuit.

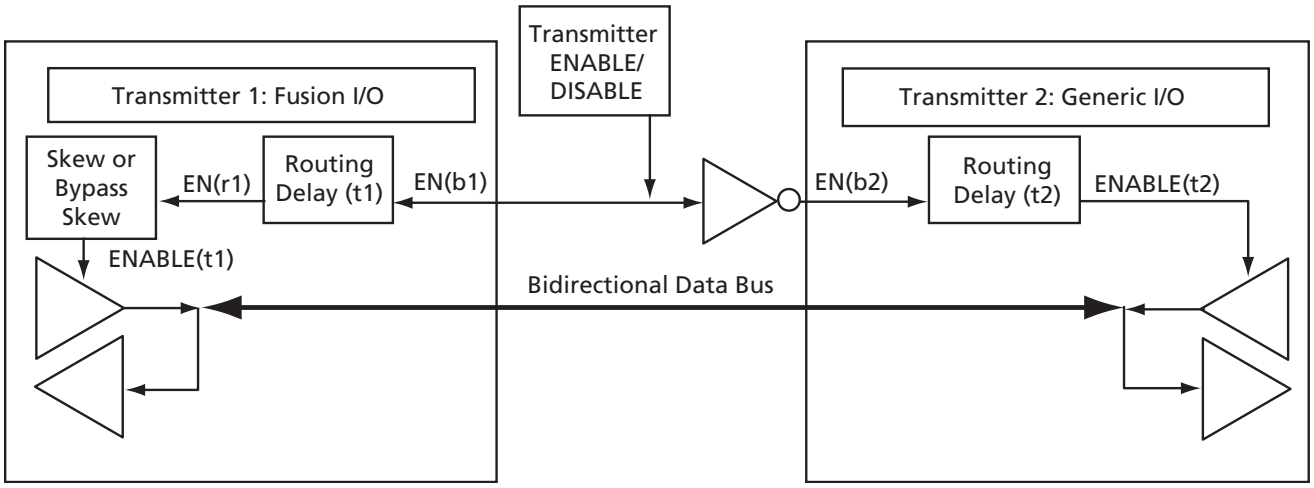


Figure 2-86 • **Example of Implementation of Skew Circuits in Bidirectional Transmission Systems Using Fusion Devices**

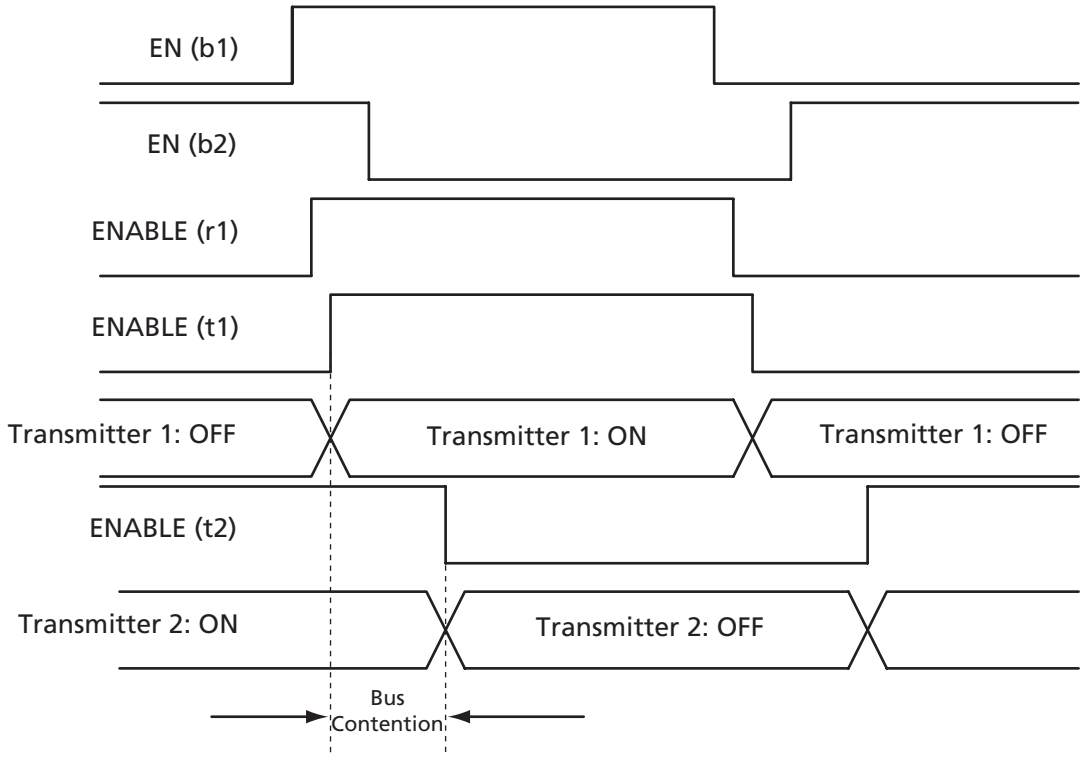


Figure 2-87 • **Timing Diagram (Bypasses Skew Circuit)**

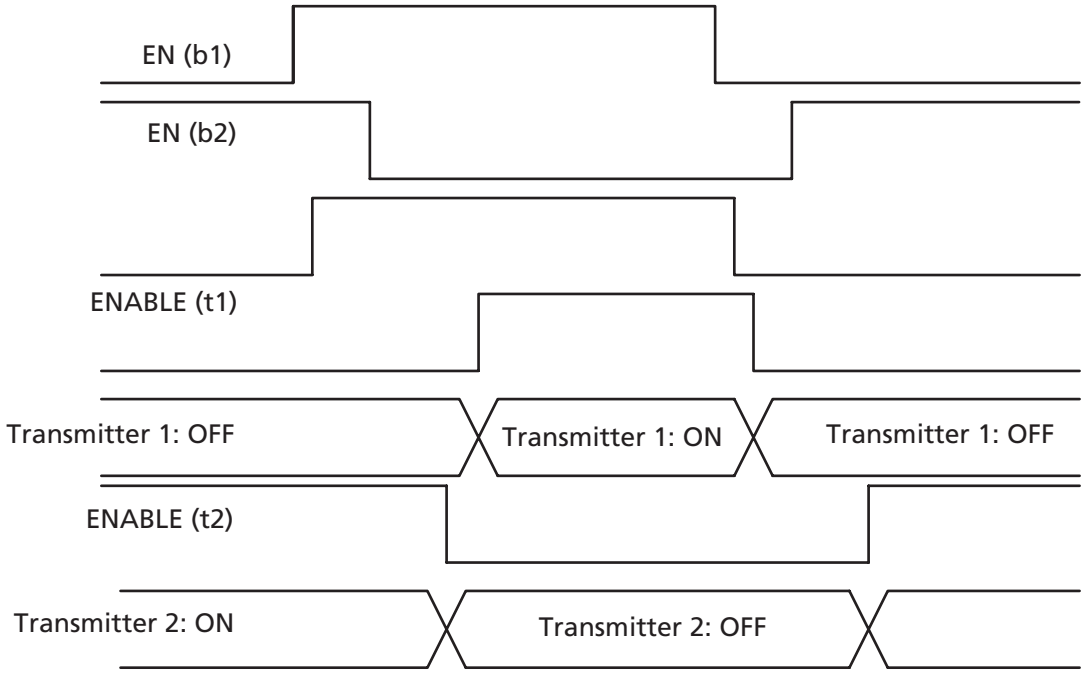


Figure 2-88 • **Timing Diagram (with Skew Circuit Selected)**

Weak Pull-Up and Weak Pull-Down Resistors

Fusion devices support optional weak pull-up and pull-down resistors per I/O pin. When the I/O is pulled up, it is connected to the V_{CCI} of its corresponding I/O bank. When it is pulled-down it is connected to GND. Refer to Table 2-79 on page 2-129 for more information.

Slew Rate Control and Drive Strength

Fusion devices support output slew rate control: high and low. The Standard hot-swap I/Os do not support slew rate control. The high slew rate option is recommended to minimize the propagation delay. This high-speed option may introduce noise into the system if appropriate signal integrity measures are not adopted. Selecting a low slew rate reduces this kind of noise but adds some delays in the system. Low slew rate is recommended when bus transients are expected. Drive strength should also be selected according to the design requirements and noise immunity of the system.

The output slew rate and multiple drive strength controls are available in LVTTL/LVCMOS 3.3 V, LVCMOS 2.5 V, LVCMOS 2.5 V / 5.0 V input, LVCMOS 1.8 V, and LVCMOS 1.5 V. All other I/O standards have a high output slew rate by default.

For Fusion slew rate and drive strength specifications, refer to the appropriate I/O bank table:

- Fusion hot-swap I/O (Table 2-64 on page 2-113)
- Fusion LVDS I/O (Table 2-65 on page 2-113)
- Fusion Pro I/O (Table 2-66 on page 2-113)

Table 2-68 on page 2-115 lists the default values for the above selectable I/O attributes as well as those that are preset for that I/O standard.

Refer to Table 2-64, Table 2-65, and Table 2-66 on page 2-113 for SLEW and OUT_DRIVE settings. Table 2-67 on page 2-114 lists the I/O default attributes. Table 2-68 on page 2-115 lists the voltages for the supported I/O standards.

Table 2-64 • **Fusion Hot-Swap I/O Standards—OUT_DRIVE Settings**

I/O Standards	OUT_DRIVE (mA)		
	2	4	8
LVTTL/LVCMOS 3.3 V	✓	✓	✓
LVCMOS 2.5 V	✓	✓	✓
LVCMOS 1.8 V	✓	✓	–
LVCMOS 1.5 V	✓	–	–

Table 2-65 • **Fusion LVDS I/O Standards—SLEW and OUT_DRIVE Settings**

I/O Standards	OUT_DRIVE (mA)							
	2	4	6	8	12	16	Slew	
LVTTL/LVCMOS 3.3 V	✓	✓	✓	✓	✓	✓	High	Low
LVCMOS 2.5 V	✓	✓	✓	✓	✓	–	High	Low
LVCMOS 1.8 V	✓	✓	✓	✓	–	–	High	Low
LVCMOS 1.5 V	✓	✓	–	–	–	–	High	Low

Table 2-66 • **Fusion Pro I/O Standards—SLEW and OUT_DRIVE Settings**

I/O Standards	OUT_DRIVE (mA)							Slew	
	2	4	6	8	12	16	24		
LVTTL/LVCMOS 3.3 V	✓	✓	✓	✓	✓	✓	✓	High	Low
LVCMOS 2.5 V	✓	✓	✓	✓	✓	✓	✓	High	Low
LVCMOS 2.5 V/5.0 V	✓	✓	✓	✓	✓	✓	✓	High	Low
LVCMOS 1.8 V	✓	✓	✓	✓	✓	✓	–	High	Low
LVCMOS 1.5 V	✓	✓	✓	✓	✓	–	–	High	Low

Table 2-67 • **Fusion Pro I/O Default Attributes**

I/O Standards	SLEW (output only)	OUT_DRIVE (output only)	SKEW) (tribuf and bibuf only)	RES_PULL	OUT_LOAD (output only)	COMBINE_REGISTER	IN_DELAY (input only)	IN_DELAY_VAL (input only)	SCHMITT_TRIGGER (input only)
LVTTL/LVCMOS 3.3 V	Refer to the following tables for more information: • Table 2-64 on page 2-113 • Table 2-65 on page 2-113 • Table 2-66 on page 2-113	Refer to the following tables for more information: • Table 2-64 on page 2-113 • Table 2-65 on page 2-113 • Table 2-66 on page 2-113	Off	None	35pF	–	Off	0	Off
LVCMOS 2.5 V			Off	None	35 pF	–	Off	0	Off
LVCMOS 2.5/5.0 V			Off	None	35 pF	–	Off	0	Off
LVCMOS 1.8 V			Off	None	35 pF	–	Off	0	Off
LVCMOS 1.5 V			Off	None	35 pF	–	Off	0	Off
PCI (3.3 V)			Off	None	10 pF	–	Off	0	Off
PCI-X (3.3 V)			Off	None	10 pF	–	Off	0	Off
GTL+ (3.3 V)			Off	None	10 pF	–	Off	0	Off
GTL+ (2.5 V)			Off	None	10 pF	–	Off	0	Off
GTL (3.3 V)			Off	None	10 pF	–	Off	0	Off
GTL (2.5 V)			Off	None	10 pF	–	Off	0	Off
HSTL Class I			Off	None	20 pF	–	Off	0	Off
HSTL Class II			Off	None	20 pF	–	Off	0	Off
SSTL2 Class I and II			Off	None	30 pF	–	Off	0	Off
SSTL3 Class I and II			Off	None	30 pF	–	Off	0	Off
LVDS, BLVDS, M-LVDS			Off	None	0 pF	–	Off	0	Off
LVPECL			Off	None	0 pF	–	Off	0	Off

Table 2-68 • **Fusion Pro I/O Supported Standards and the Corresponding V_{REF} and V_{TT} Voltages**

I/O Standard	Input/Output Supply Voltage (VMVtyp/V_{CCI_TYP})	Input Reference Voltage (V_{REF_TYP})	Board Termination Voltage (V_{TT_TYP})
LVTTL/LVCMOS 3.3 V	3.30 V	–	–
LVCMOS 2.5 V	2.50 V	–	–
LVCMOS 2.5 V/5.0 V Input	2.50 V	–	–
LVCMOS 1.8 V	1.80 V	–	–
LVCMOS 1.5 V	1.50 V	–	–
PCI 3.3 V	3.30 V	–	–
PCI-X 3.3 V	3.30 V	–	–
GTL+ 3.3 V	3.30 V	1.00 V	1.50 V
GTL+ 2.5 V	2.50 V	1.00 V	1.50 V
GTL 3.3 V	3.30 V	0.80 V	1.20 V
GTL 2.5 V	2.50 V	0.80 V	1.20 V
HSTL Class I	1.50 V	0.75 V	0.75 V
HSTL Class II	1.50 V	0.75 V	0.75 V
SSTL3 Class I	3.30 V	1.50 V	1.50 V
SSTL3 Class II	3.30 V	1.50 V	1.50 V
SSTL2 Class I	2.50 V	1.25 V	1.25 V
SSTL2 Class II	2.50 V	1.25 V	1.25 V
LVDS, BLVDS, M-LVDS	2.50 V	–	–
LVPECL	3.30 V	–	–

I/O Software Support

In the Fusion development software, default settings have been defined for the various I/O standards that are supported. Changes can be made to the default settings via the use of attributes; however, not all I/O attributes are applicable for all I/O standards. Table 2-69 and Table 2-70 list the valid I/O attributes that can be manipulated by the user for each I/O standard.

Single-ended I/O standards in Fusion support up to five different drive strengths.

Table 2-69 • **Fusion Standard and LVDS I/O Attributes vs. I/O Standard Applications**

I/O Standards	SLEW (output only)	OUT_DRIVE (output only)	SKEW (all macros with OE)*	RES_PULL	OUT_LOAD (output only)	COMBINE_REGISTER
LVTTL/LVCMOS 3.3 V	✓	✓	✓	✓	✓	✓
LVCMOS 2.5 V	✓	✓	✓	✓	✓	✓
LVCMOS 2.5/5.0 V	✓	✓	✓	✓	✓	✓
LVCMOS 1.8 V	✓	✓	✓	✓	✓	✓
LVCMOS 1.5 V	✓	✓	✓	✓	✓	✓
PCI (3.3 V)			✓		✓	✓
PCI-X (3.3 V)	✓		✓		✓	✓
LVDS, BLVDS, M-LVDS			✓			✓
LVPECL						✓

Note: **This does not apply to the north I/O bank on AFS090 and AFS250 devices.*

Table 2-70 • **Fusion Pro I/O Attributes vs. I/O Standard Applications**

I/O Standards	SLEW (output only)	OUT_DRIVE (output only)	SKEW (all macros with OE)	RES_PULL	OUT_LOAD (output only)	COMBINE_REGISTER	IN_DELAY (input only)	IN_DELAY_VAL (input only)	SCHMITT_TRIGGER (input only)	HOT_SWAPPABLE
LVTTL/LVCMOS 3.3 V	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
LVCMOS 2.5 V	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
LVCMOS 2.5/5.0 V	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
LVCMOS 1.8 V	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
LVCMOS 1.5 V	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
PCI (3.3 V)			✓		✓	✓	✓	✓		
PCI-X (3.3 V)	✓		✓		✓	✓	✓	✓		
GTL+ (3.3 V)			✓		✓	✓	✓	✓		✓
GTL+ (2.5 V)			✓		✓	✓	✓	✓		✓
GTL (3.3 V)			✓		✓	✓	✓	✓		✓

Table 2-70 • **Fusion Pro I/O Attributes vs. I/O Standard Applications (Continued)**

I/O Standards	SLEW (output only)	OUT_DRIVE (output only)	SKEW (all macros with OE)	RES_PULL	OUT_LOAD (output only)	COMBINE_REGISTER	IN_DELAY (input only)	IN_DELAY_VAL (input only)	SCHMITT_TRIGGER (input only)	HOT_SWAPPABLE
GTL (2.5 V)			✓		✓	✓	✓	✓		✓
HSTL Class I			✓		✓	✓	✓	✓		✓
HSTL Class II			✓		✓	✓	✓	✓		✓
SSTL2 Class I and II			✓		✓	✓	✓	✓		✓
SSTL3 Class I and II			✓		✓	✓	✓	✓		✓
LVDS, BLVDS, M-LVDS			✓			✓	✓	✓		✓
LVPECL						✓	✓	✓		✓

Table 2-71 lists the default values for the above selectable I/O attributes as well as those that are preset for that I/O standard. See Table 2-64, Table 2-65, and Table 2-66 on page 2-113 for SLEW and OUT_DRIVE settings.

Table 2-71 • **I/O Default Attributes**

I/O Standards	SLEW (output only)	OUT_DRIVE (output only)	SKEW) (tribuf and bibuf only)	RES_PULL	OUT_LOAD (output only)	COMBINE_REGISTER
LVTTL/LVCMOS 3.3 V	Refer to the following tables for more information: • Table 2-64 on page 2-113 • Table 2-65 on page 2-113 • Table 2-66 on page 2-113	Refer to the following tables for more information: • Table 2-64 on page 2-113 • Table 2-65 on page 2-113 • Table 2-66 on page 2-113	Off	None	35 pF	–
LVCMOS 2.5 V			Off	None	35 pF	–
LVCMOS 2.5/5.0 V			Off	None	35 pF	–
LVCMOS 1.8 V			Off	None	35 pF	–
LVCMOS 1.5 V			Off	None	35 pF	–
PCI (3.3 V)			Off	None	10 pF	–
PCI-X (3.3 V)			Off	None	10 pF	–
LVDS, BLVDS, M-LVDS			Off	None	–	–
LVPECL			Off	None	–	–

User I/O Naming Convention

Due to the comprehensive and flexible nature of Fusion device user I/Os, a naming scheme is used to show the details of the I/O (Figure 2-89 and Figure 2-90 on page 2-119). The name identifies to which I/O bank it belongs, as well as the pairing and pin polarity for differential I/Os.

I/O Nomenclature = Gmn/IOuxwBy

Gmn is only used for I/Os that also have CCC access – i.e., global pins.

G = Global

m = Global pin location associated with each CCC on the device: A (northwest corner), B (northeast corner), C (east middle), D (southeast corner), E (southwest corner), and F (west middle).

n = Global input MUX and pin number of the associated Global location m, either A0, A1, A2, B0, B1, B2, C0, C1, or C2. Figure 2-22 on page 2-25 shows the three input pins per each clock source MUX at the CCC location m.

u = I/O pair number in the bank, starting at 00 from the northwest I/O bank in a clockwise direction.

x = P (Positive) or N (Negative) for differential pairs, or R (Regular – single-ended) for the I/Os that support single-ended and voltage-referenced I/O standards only. U (Positive-LVDS only) or V (Negative-LVDS only) restrict the I/O differential pair from being selected as LVPECL pair.

w = D (Differential Pair), P (Pair), S (Single-Ended). D (Differential Pair) if both members of the pair are bonded out to adjacent pins or are separated only by one GND or NC pin; P (Pair) if both members of the pair are bonded out but do not meet the adjacency requirement; or S (Single-Ended) if the I/O pair is not bonded out. For Differential (D) pairs, adjacency for ball grid packages means only vertical or horizontal. Diagonal adjacency does not meet the requirements for a true differential pair.

B = Bank

y = Bank number [0..3]. The Bank number starts at 0 from the northwest I/O bank and proceeds in a clockwise direction.

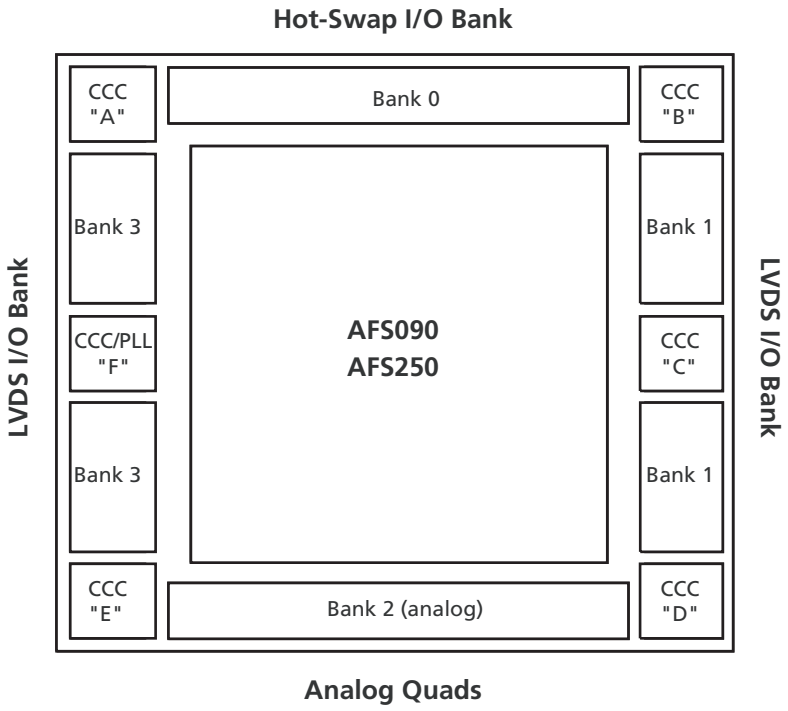


Figure 2-89 • **Naming Conventions of Fusion Devices with Three Digital I/O Banks**

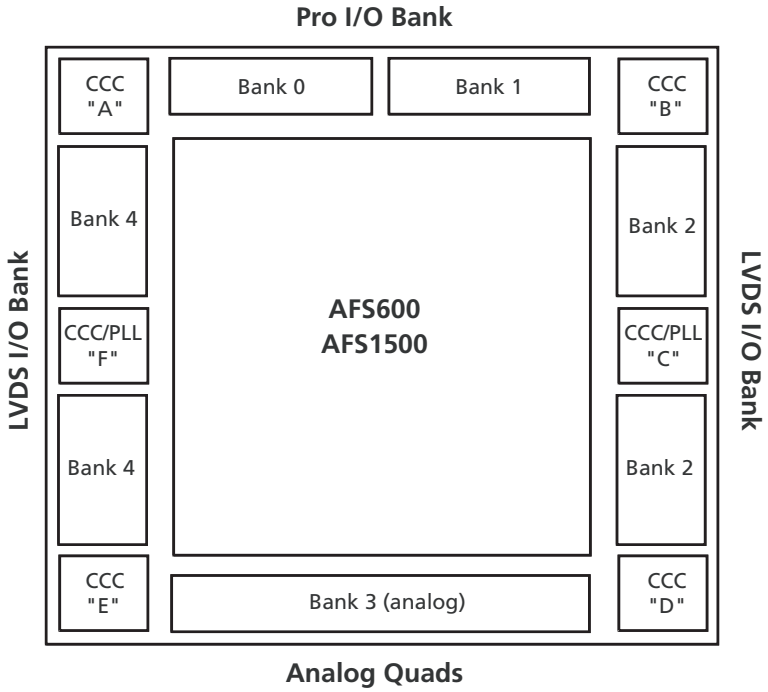


Figure 2-90 • **Naming Conventions of Fusion Devices with Four I/O Banks**

User I/O Characteristics

Timing Model

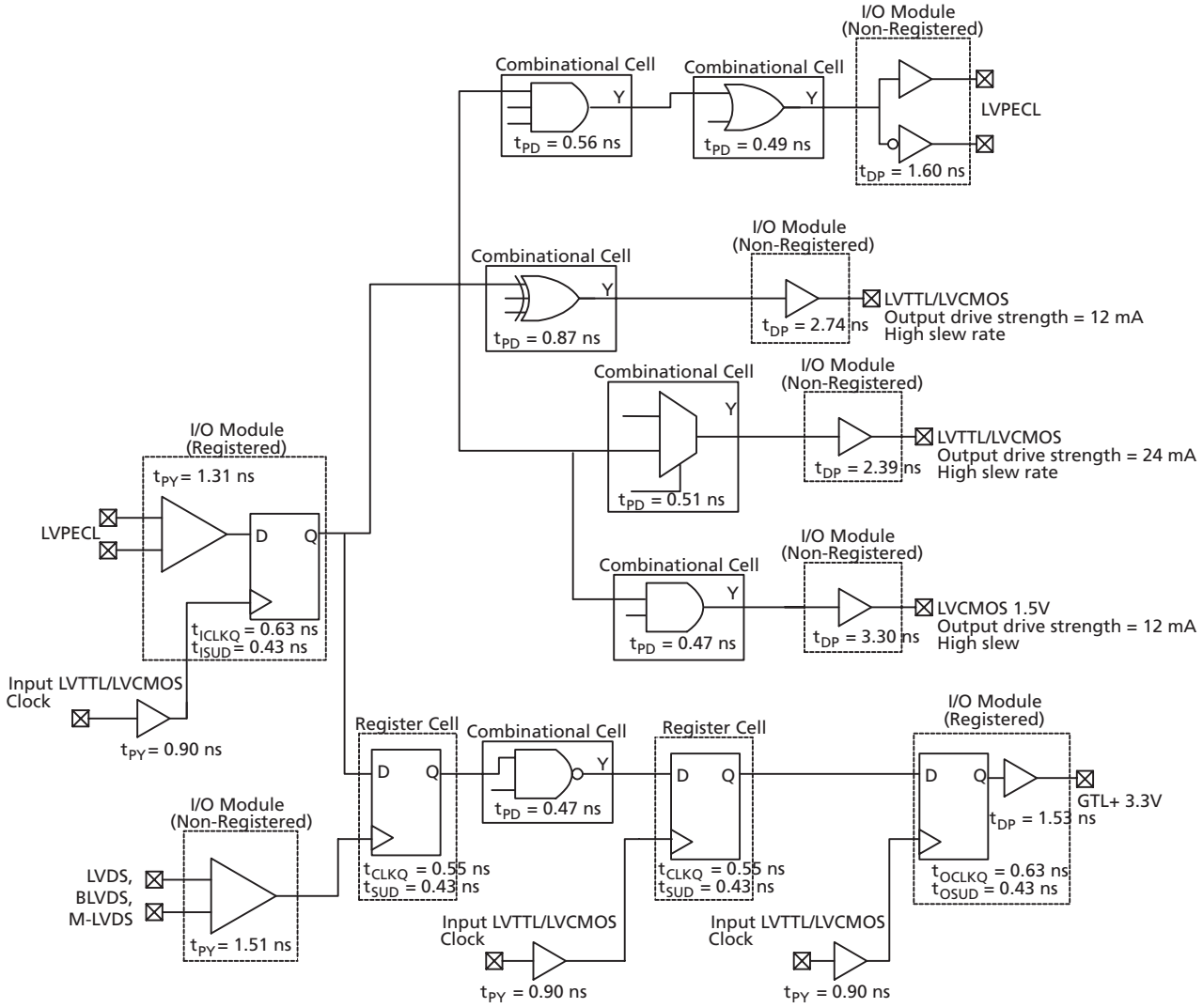
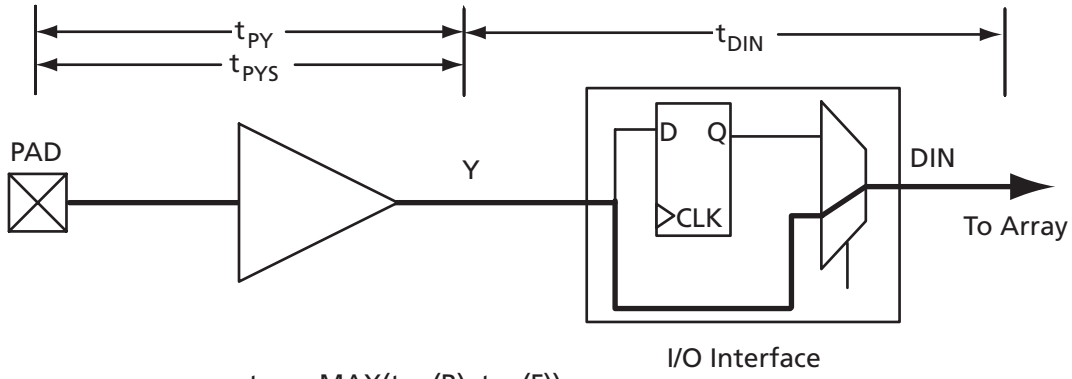


Figure 2-91 • **Timing Model**
Operating Conditions: –2 Speed, Commercial Temperature Range (T_J = 70°C), Worst Case V_{CC} = 1.425 V



$t_{PY} = MAX(t_{PY}(R), t_{PY}(F))$

$t_{PYS} = MAX(t_{PYS}(R), t_{PYS}(F))$

$t_{DIN} = MAX(t_{DIN}(R), t_{DIN}(F))$

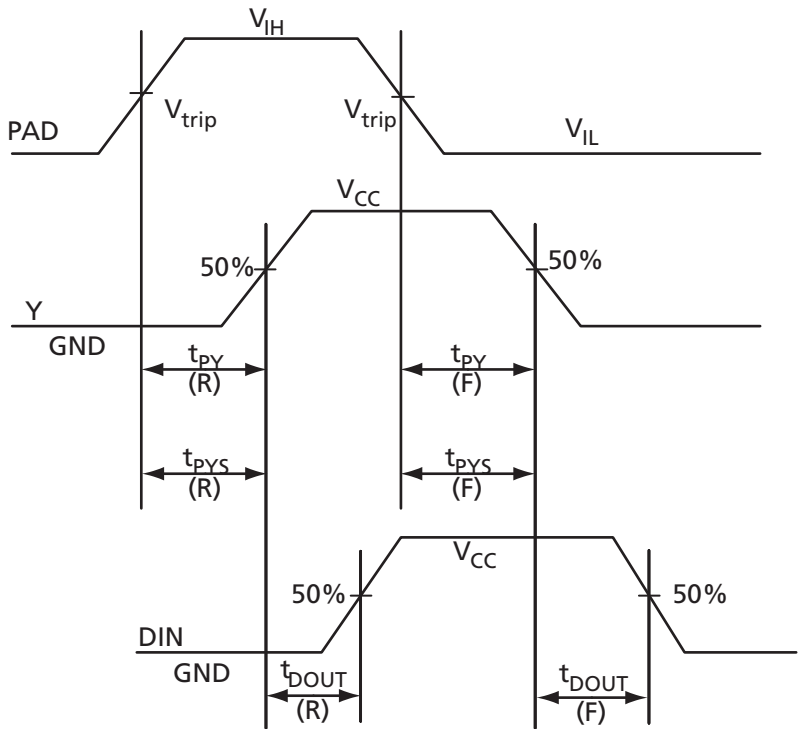


Figure 2-92 • **Input Buffer Timing Model and Delays (example)**

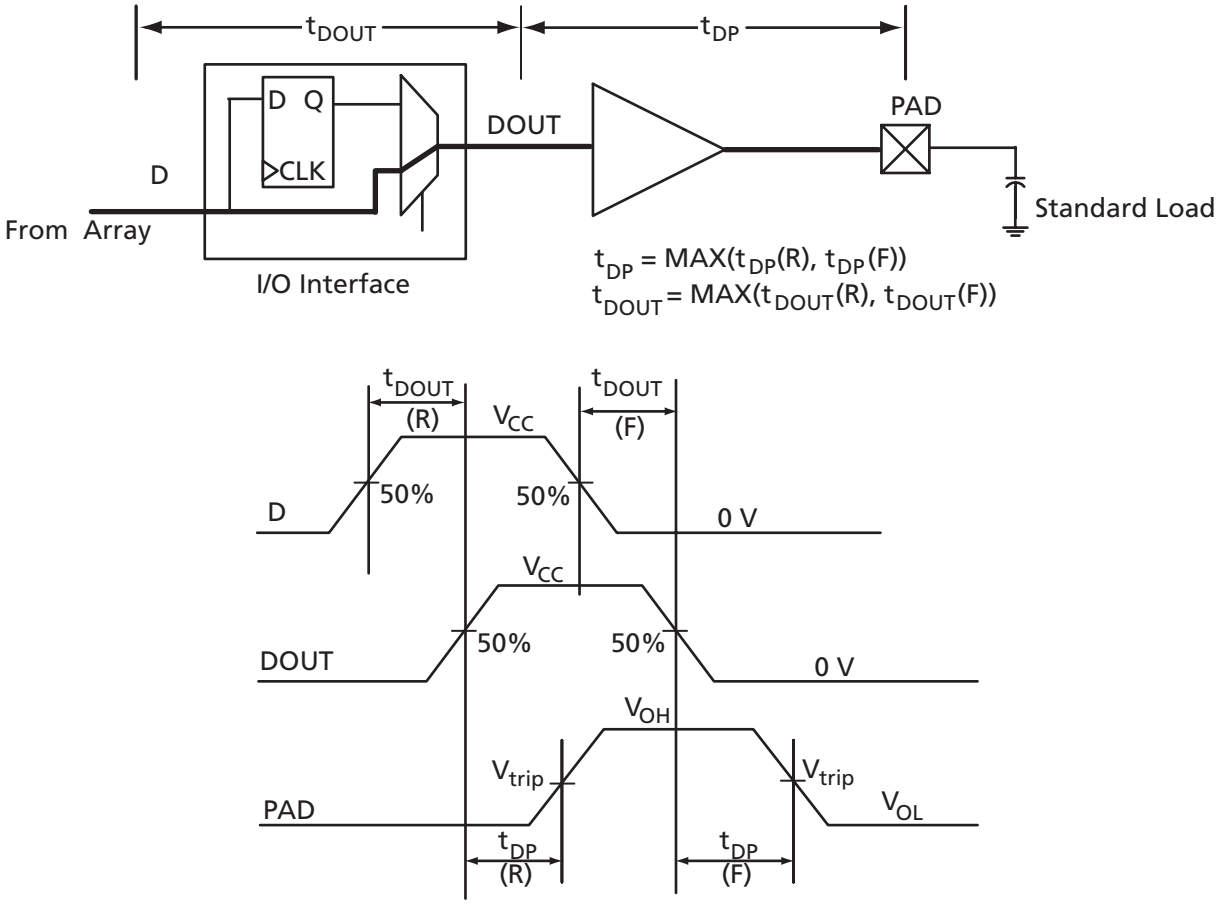


Figure 2-93 • **Output Buffer Model and Delays (example)**

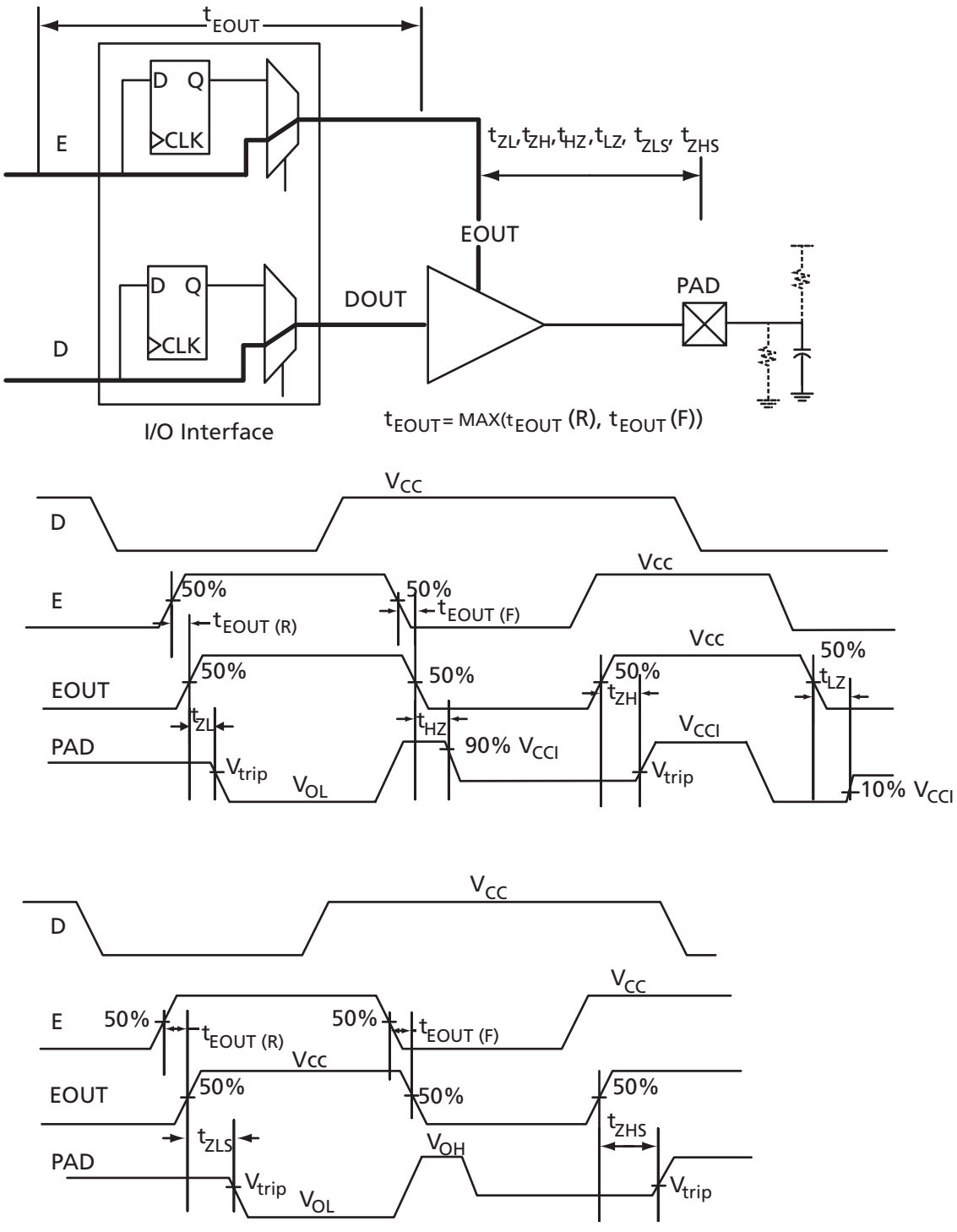


Figure 2-94 • **Tristate Output Buffer Timing Model and Delays (example)**

Overview of I/O Performance

Summary of I/O DC Input and Output Levels – Default I/O Software Settings

Table 2-72 • **Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions**

I/O Standard	Drive Strength	Slew Rate	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
			Min, V	Max, V	Min, V	Max, V	Max, V	Min, V	mA	mA
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
2.5 V LVCMOS	12 mA	High	–0.3	0.7	1.7	3.6	0.7	1.7	12	12
1.8 V LVCMOS	12 mA	High	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	3.6	0.45	V_{CCI} – 0.45	12	12
1.5 V LVCMOS	12 mA	High	–0.3	0.30V_{CCI}	0.7 * V_{CCI}	3.6	0.25 * V_{CCI}	0.75 * V_{CCI}	12	12
3.3 V PCI	Per PCI Specification									
3.3 V PCI-X	Per PCI-X Specification									
3.3 V GTL	25 mA[2]	High	–0.3	V_{REF} – 0.05	V_{REF} + 0.05	3.6	0.4	–	25	25
2.5 V GTL	25 mA[2]	High	–0.3	V_{REF} – 0.05	V_{REF} + 0.05	3.6	0.4	–	25	25
3.3 V GTL+	35 mA	High	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.6	–	51	51
2.5 V GTL+	33 mA	High	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.6	–	40	40
HSTL (I)	8 mA	High	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCI} – 0.4	8	8
HSTL (II)	15 mA[2]	High	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCI} – 0.4	15	15
SSTL2 (I)	15 mA	High	–0.3	V_{REF} – 0.2	V_{REF} + 0.2	3.6	0.54	V_{CCI} – 0.62	15	15
SSTL2 (II)	18 mA	High	–0.3	V_{REF} – 0.2	V_{REF} + 0.2	3.6	0.35	V_{CCI} – 0.43	18	18
SSTL3 (I)	14 mA	High	–0.3	V_{REF} – 0.2	V_{REF} + 0.2	3.6	0.7	V_{CCI} – 1.1	14	14
SSTL3 (II)	21 mA	High	–0.3	V_{REF} – 0.2	V_{REF} + 0.2	3.6	0.5	V_{CCI} – 0.9	21	21

Notes:

1. *Currents are measured at 85°C junction temperature.*
2. *Output drive strength is below JEDEC specification.*

Table 2-73 • **Summary of Maximum and Minimum DC Input Levels Applicable to Commercial and Industrial Conditions**

	Commercial[1]		Industrial[2]	
	I_{IL}	I_{IH}	I_{IL}	I_{IH}
DC I/O Standards	**µA**	**µA**	**µA**	**µA**
3.3 V LVTTL / 3.3 V LVCMOS	10	10	15	15
2.5 V LVCMOS	10	10	15	15
1.8 V LVCMOS	10	10	15	15
1.5 V LVCMOS	10	10	15	15
3.3 V PCI	10	10	15	15
3.3 V PCI-X	10	10	15	15
3.3 V GTL	10	10	15	15
2.5 V GTL	10	10	15	15
3.3 V GTL+	10	10	15	15
2.5 V GTL+	10	10	15	15
HSTL (I)	10	10	15	15
HSTL (II)	10	10	15	15
SSTL2 (I)	10	10	15	15
SSTL2 (II)	10	10	15	15
SSTL3 (I)	10	10	15	15
SSTL3 (II)	10	10	15	15

Notes:

1. *Commercial range (0°C < T_J < 70°C)*
2. *Industrial range (–40°C < T_J < 85°C)*

Summary of I/O Timing Characteristics – Default I/O Software Settings

Table 2-74 • **Summary of AC Measuring Points**

Standard	Input Reference Voltage (V_{REF_TYP})	Board Termination Voltage (V_{TT_REF})	Measuring Trip Point (V_{trip})
3.3 V LVTTL / 3.3 V LVCMOS	–	–	1.4 V
2.5 V LVCMOS	–	–	1.2 V
1.8 V LVCMOS	–	–	0.90 V
1.5 V LVCMOS	–	–	0.75 V
3.3 V PCI	–	–	0.285 * V_{CCI} (RR) 0.615 * V_{CCI} (FF))
3.3 V PCI-X	–	–	0.285 * V_{CCI} (RR) 0.615 * V_{CCI} (FF)
3.3 V GTL	0.8 V	1.2 V	V_{REF}
2.5 V GTL	0.8 V	1.2 V	V_{REF}
3.3 V GTL+	1.0 V	1.5 V	V_{REF}
2.5 V GTL+	1.0 V	1.5 V	V_{REF}
HSTL (I)	0.75 V	0.75 V	V_{REF}
HSTL (II)	0.75 V	0.75 V	V_{REF}
SSTL2 (I)	1.25 V	1.25 V	V_{REF}
SSTL2 (II)	1.25 V	1.25 V	V_{REF}
SSTL3 (I)	1.5 V	1.485 V	V_{REF}
SSTL3 (II)	1.5 V	1.485 V	V_{REF}
LVDS, BLVDS, M-LVDS	–	–	Cross point
LVPECL	–	–	Cross point

Table 2-75 • **I/O AC Parameter Definitions**

Parameter	Definition
t_{DP}	Data to Pad delay through the Output Buffer
t_{PY}	Pad to Data delay through the Input Buffer with Schmitt trigger disabled
t_{DOUT}	Data to Output Buffer delay through the I/O interface
t_{EOUT}	Enable to Output Buffer Tristate Control delay through the I/O interface
t_{DIN}	Input Buffer to Data delay through the I/O interface
t_{PYS}	Pad to Data delay through the Input Buffer with Schmitt trigger enabled
t_{HZ}	Enable to Pad delay through the Output Buffer—high to Z
t_{ZH}	Enable to Pad delay through the Output Buffer—Z to high
t_{LZ}	Enable to Pad delay through the Output Buffer—low to Z
t_{ZL}	Enable to Pad delay through the Output Buffer—Z to low
t_{ZHS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to high
t_{ZLS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to low

Table 2-76 • **Summary of I/O Timing Characteristics – Software Default Settings**
–2 Speed Grade, Commercial-Case Conditions: T_J= 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 3.0 V

I/O Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ohm)	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	35	–	0.49	2.74	0.03	0.90	1.17	0.32	2.79	2.14	2.45	2.70	4.46	3.81	ns
2.5 V LVCMOS	12 mA	High	35	–	0.49	2.80	0.03	1.13	1.24	0.32	2.85	2.61	2.51	2.61	4.52	4.28	ns
1.8 V LVCMOS	12 mA	High	35	–	0.49	2.83	0.03	1.08	1.42	0.32	2.89	2.31	2.79	3.16	4.56	3.98	ns
1.5 V LVCMOS	12 mA	High	35	–	0.49	3.30	0.03	1.27	1.60	0.32	3.36	2.70	2.96	3.27	5.03	4.37	ns
3.3 V PCI	Per PCI spec	High	10	25 [2]	0.49	2.09	0.03	0.78	1.25	0.32	2.13	1.49	2.45	2.70	3.80	3.16	ns
3.3 V PCI-X	Per PCI-X spec	High	10	25 [2]	0.49	2.09	0.03	0.78	1.25	0.32	2.13	1.49	2.45	2.70	3.80	3.16	ns
3.3 V GTL	25 mA	High	10	25	0.49	1.55	0.03	2.19	–	0.32	1.52	1.55	–	–	3.19	3.22	ns
2.5 V GTL	25 mA	High	10	25	0.49	1.59	0.03	1.83	–	0.32	1.61	1.59	–	–	3.28	3.26	ns
3.3 V GTL+	35 mA	High	10	25	0.49	1.53	0.03	1.19	–	0.32	1.56	1.53	–	–	3.23	3.20	ns
2.5 V GTL+	33 mA	High	10	25	0.49	1.65	0.03	1.13	–	0.32	1.68	1.57	–	–	3.35	3.24	ns
HSTL (I)	8 mA	High	20	50	0.49	2.37	0.03	1.59	–	0.32	2.42	2.35	–	–	4.09	4.02	ns
HSTL (II)	15 mA	High	20	25	0.49	2.26	0.03	1.59	–	0.32	2.30	2.03	–	–	3.97	3.70	ns
SSTL2 (I)	15 mA	High	30	50	0.49	1.59	0.03	1.00	–	0.32	1.62	1.38	–	–	3.29	3.05	ns
SSTL2 (II)	18 mA	High	30	25	0.49	1.62	0.03	1.00	–	0.32	1.65	1.32	–	–	3.32	2.99	ns
SSTL3 (I)	14 mA	High	30	50	0.49	1.72	0.03	0.93	–	0.32	1.75	1.37	–	–	3.42	3.04	ns
SSTL3 (II)	21 mA	High	30	25	0.49	1.54	0.03	0.93	–	0.32	1.57	1.25	–	–	3.24	2.92	ns
LVDS, BLVDS, M-LVDS	24 mA	High	–	–	0.49	1.57	0.03	1.51	–	–	–	–	–	–	–	–	ns
LVPECL	24 mA	High	–	–	0.49	1.60	0.03	1.31	–	–	–	–	–	–	–	–	ns

Notes:

1. *For the derating values at specific junction-temperature and voltage-supply levels, refer to Table 3-6 on page 3-6.*
2. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-99 on page 2-141 for connectivity. This resistor is not required during normal operation.*

Detailed I/O DC Characteristics

Table 2-77 • **Input Capacitance**

Symbol	Definition	Conditions	Min.	Max.	Units
C_{IN}	Input capacitance	V_{IN} = 0, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance on the clock pin	V_{IN} = 0, f = 1.0 MHz		8	pF

Table 2-78 • **I/O Output Buffer Maximum Resistances[1]**

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (Ohms)[2]	$R_{PULL\text{-}UP}$ (Ohms)[3]
3.3 V LVTTL / 3.3 V LVCMOS	4 mA	100	300
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
2.5 V LVCMOS	4 mA	100	200
	8 mA	50	100
	12 mA	25	50
	16 mA	20	40
	24 mA	11	22
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
	12 mA	20	22
	16 mA	20	22
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
	6 mA	67	75
	8 mA	33	37
	12 mA	33	37
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75
3.3 V GTL	25 mA	11	–
2.5 V GTL	25 mA	14	–
3.3 V GTL+	35 mA	12	–
2.5 V GTL+	33 mA	15	–
HSTL (I)	8 mA	50	50
HSTL (II)	15 mA	25	25
SSTL2 (I)	15 mA	27	31
SSTL2 (II)	18 mA	13	15
SSTL3 (I)	14 mA	44	69
SSTL3 (II)	21 mA	18	32

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on V_{CCI}, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Actel website at http://www.actel.com/techdocs/models/ibis.html.*
2. $R_{(PULL\text{-}DOWN\text{-}MAX)} = (V_{OLspec}) / I_{OLspec}$
3. $R_{(PULL\text{-}UP\text{-}MAX)} = (V_{CCImax} – V_{OHspec}) / I_{OHspec}$

Table 2-79 • **I/O Weak Pull-Up/Pull-Down Resistances**
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values

	$R_{(WEAK\ PULL\text{-}UP)}$[1] (Ohms)		$R_{(WEAK\ PULL\text{-}DOWN)}$[2] (Ohms)	
V_{CCI}	Min.	Max.	Min.	Max.
3.3 V	10 k	45 k	10 k	45 k
2.5 V	11 k	55 k	12 k	74 k
1.8 V	18 k	70 k	17 k	110 k
1.5 V	19 k	90 k	19 k	140 k

Notes:

1. $R_{(WEAK\ PULL\text{-}DOWN\text{-}MAX)} = (V_{OLspec}) / I_{WEAK\ PULL\text{-}DOWN\text{-}MIN}$
2. $R_{(WEAK\ PULL\text{-}UP\text{-}MAX)} = (V_{CCImax} - V_{OHspec}) / I_{WEAK\ PULL\text{-}UP\text{-}MIN}$

Table 2-80 • **I/O Short Currents I_{OSH}/I_{OSL}**

	Drive Strength	I_{OSH} (mA)*	I_{OSL} (mA)*
3.3 V LVTTL / 3.3 V LVCMOS	4 mA	25	27
	8 mA	51	54
	12 mA	103	109
	16 mA	132	127
	24 mA	268	181
2.5 V LVCMOS	4 mA	16	18
	8 mA	32	37
	12 mA	65	74
	16 mA	83	87
	24 mA	169	124
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
	6 mA	35	44
	8 mA	45	51
	12 mA	91	74
	16 mA	91	74
1.5 V LVCMOS	2 mA	13	16
	4 mA	25	33
	6 mA	32	39
	8 mA	66	55
	12 mA	66	55

Note: **T_J = 100°C*

The length of time an I/O can withstand I_{OSH}/I_{OSL} events depends on the junction temperature. The reliability data below is based on a 3.3 V, 36 mA I/O setting, which is the worst case for this type of analysis.

For example, at 110°C, the short current condition would have to be sustained for more than three months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

Table 2-81 • **Short Current Event Duration Before Failure**

Temperature	Time Before Failure
–40°C	> 20 years
0°C	> 20 years
25°C	> 20 years
70°C	5 years
85°C	2 years
100°C	6 months
110°C	3 months

Table 2-82 • **Schmitt Trigger Input Hysteresis**
Hysteresis Voltage Value (Typ) for Schmitt Mode Input Buffers

Input Buffer Configuration	Hysteresis Value (Typ)
3.3 V LVTTL/LVCMOS / PCI / PCI-X (Schmitt trigger mode)	240 mV
2.5 V LVCMOS (Schmitt trigger mode)	140 mV
1.8 V LVCMOS (Schmitt trigger mode)	80 mV
1.5 V LVCMOS (Schmitt trigger mode)	60 mV

Table 2-83 • **I/O Input Rise Time, Fall Time, and Related I/O Reliability**

Input Buffer	Input Rise/Fall Time (Min.)	Input Rise/Fall Time (Max.)	Reliability
LVTTL/LVCMOS (Schmitt trigger disabled)	No requirement	10 ns*	20 years (110°C)
LVTTL/LVCMOS (Schmitt trigger enabled)	No requirement	No requirement, but input noise voltage cannot exceed Schmitt hysteresis	20 years (110°C)
HSTL/SSTL/GTL	No requirement	10 ns*	10 years (100°C)
LVDS/BLVDS/M-LVDS/LVPECL	No requirement	10 ns*	10 years (100°C)

Note: **The Maximum Input rise/fall time is related only to the noise induced into the input buffer trace. If the noise is low, then the rise time and fall time of input buffers, when Schmitt trigger is disabled, can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Actel recommends signal integrity evaluation/ characterization of the system to ensure that there is no excessive noise coupling into input signals.*

Single-Ended I/O Characteristics

3.3 V LVTTL / 3.3 V LVCMOS

Low-Voltage Transistor-Transistor Logic is a general purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTL input buffer and push-pull output buffer. The 3.3 V LVCMOS standard is supported as part of the 3.3 V LVTTL support.

Table 2-84 • **Minimum and Maximum DC Input and Output Levels**

3.3 V LVTTL / 3.3 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min, V**	**Max, V**	**Min, V**	**Max, V**	**Max, V**	**Min, V**	**mA**	**mA**	**Max, mA[1]**	**Max, mA[1]**	**µA[2]**	**µA[2]**
4 mA	–0.3	0.8	2	3.6	0.4	2.4	4	4	27	25	10	10
8 mA	–0.3	0.8	2	3.6	0.4	2.4	8	8	54	51	10	10
12 mA	–0.3	0.8	2	3.6	0.4	2.4	12	12	109	103	10	10
16 mA	–0.3	0.8	2	3.6	0.4	2.4	16	16	127	132	10	10
24 mA	–0.3	0.8	2	3.6	0.4	2.4	24	24	181	268	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

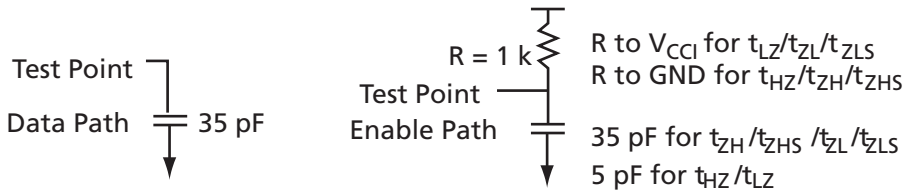


Figure 2-95 • **AC Loading**

Table 2-85 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (Typ) (V)	C_{LOAD} (pF)
0	3.3	1.4	–	35

Note: **Measuring point = V_{trip}. See Table 2-74 on page 2-126 for a complete table of trip points.*

Timing Characteristics

Table 2-86 • **3.3 V LVTTL / 3.3 V LVCMOS Low Slew**
Commercial Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 3.0 V

Drive Strength (mA)	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4mA	Std.	0.66	11.01	0.04	1.20	1.57	0.43	11.21	9.05	2.69	2.44	13.45	11.29	ns
	–1	0.56	9.36	0.04	1.02	1.33	0.36	9.54	7.70	2.29	2.08	11.44	9.60	ns
	–2	0.49	8.22	0.03	0.90	1.17	0.32	8.37	6.76	2.01	1.82	10.04	8.43	ns
8mA	Std.	0.66	7.86	0.04	1.20	1.57	0.43	8.01	6.44	3.04	3.06	10.24	8.68	ns
	–1	0.56	6.69	0.04	1.02	1.33	0.36	6.81	5.48	2.58	2.61	8.71	7.38	ns
	–2	0.49	5.87	0.03	0.90	1.17	0.32	5.98	4.81	2.27	2.29	7.65	6.48	ns
12mA	Std.	0.66	6.03	0.04	1.20	1.57	0.43	6.14	5.02	3.28	3.47	8.37	7.26	ns
	–1	0.56	5.13	0.04	1.02	1.33	0.36	5.22	4.27	2.79	2.95	7.12	6.17	ns
	–2	0.49	4.50	0.03	0.90	1.17	0.32	4.58	3.75	2.45	2.59	6.25	5.42	ns
16mA	Std.	0.66	5.62	0.04	1.20	1.57	0.43	5.72	4.72	3.32	3.58	7.96	6.96	ns
	–1	0.56	4.78	0.04	1.02	1.33	0.36	4.87	4.02	2.83	3.04	6.77	5.92	ns
	–2	0.49	4.20	0.03	0.90	1.17	0.32	4.27	3.53	2.48	2.67	5.94	5.20	ns
24mA	Std.	0.66	5.24	0.04	1.20	1.57	0.43	5.34	4.69	3.39	3.96	7.58	6.93	ns
	–1	0.56	4.46	0.04	1.02	1.33	0.36	4.54	3.99	2.88	3.37	6.44	5.89	ns
	–2	0.49	3.92	0.03	0.90	1.17	0.32	3.99	3.50	2.53	2.96	5.66	5.17	ns

Note: *For the derating values at specific junction-temperature and voltage-supply levels, refer to Table 3-6 on page 3-6.*

Table 2-87 • **3.3 V LVTTL / 3.3 V LVCMOS High Slew**
Commercial Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 3.0

Drive Strength (mA)	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4mA	Std.	0.66	7.88	0.04	1.20	1.57	0.43	8.03	6.70	2.69	2.59	10.26	8.94	ns
	–1	0.56	6.71	0.04	1.02	1.33	0.36	6.83	5.70	2.29	2.20	8.73	7.60	ns
	–2	0.49	5.89	0.03	0.90	1.17	0.32	6.00	5.01	2.01	1.93	7.67	6.67	ns
8mA	Std.	0.66	5.08	0.04	1.20	1.57	0.43	5.17	4.14	3.05	3.21	7.41	6.38	ns
	–1	0.56	4.32	0.04	1.02	1.33	0.36	4.40	3.52	2.59	2.73	6.30	5.43	ns
	–2	0.49	3.79	0.03	0.90	1.17	0.32	3.86	3.09	2.28	2.40	5.53	4.76	ns
12mA	Std.	0.66	3.67	0.04	1.20	1.57	0.43	3.74	2.87	3.28	3.61	5.97	5.11	ns
	–1	0.56	3.12	0.04	1.02	1.33	0.36	3.18	2.44	2.79	3.07	5.08	4.34	ns
	–2	0.49	2.74	0.03	0.90	1.17	0.32	2.79	2.14	2.45	2.70	4.46	3.81	ns
16mA	Std.	0.66	3.46	0.04	1.20	1.57	0.43	3.53	2.61	3.33	3.72	5.76	4.84	ns
	–1	0.56	2.95	0.04	1.02	1.33	0.36	3.00	2.22	2.83	3.17	4.90	4.12	ns
	–2	0.49	2.59	0.03	0.90	1.17	0.32	2.63	1.95	2.49	2.78	4.30	3.62	ns
24mA	Std.	0.66	3.21	0.04	1.20	1.57	0.43	3.27	2.16	3.39	4.13	5.50	4.39	ns
	–1	0.56	2.73	0.04	1.02	1.33	0.36	2.78	1.83	2.88	3.51	4.68	3.74	ns
	–2	0.49	2.39	0.03	0.90	1.17	0.32	2.44	1.61	2.53	3.08	4.11	3.28	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For the derating values at specific junction-temperature and voltage-supply levels, refer to Table 3-6 on page 3-6.*

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general purpose 2.5 V applications. It uses a 5-V-tolerant input buffer and push-pull output buffer.

Table 2-88 • **Minimum and Maximum DC Input and Output Levels**

2.5 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min, V**	**Max, V**	**Min, V**	**Max, V**	**Max, V**	**Min, V**	**mA**	**mA**	**Max, mA[1]**	**Max, mA[1]**	**µA[2]**	**µA[2]**
4 mA	–0.3	0.7	1.7	3.6	0.7	1.7	4	4	18	16	10	10
8 mA	–0.3	0.7	1.7	3.6	0.7	1.7	8	8	37	32	10	10
12 mA	–0.3	0.7	1.7	3.6	0.7	1.7	12	12	74	65	10	10
16 mA	–0.3	0.7	1.7	3.6	0.7	1.7	16	16	87	83	10	10
24 mA	–0.3	0.7	1.7	3.6	0.7	1.7	24	24	124	169	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

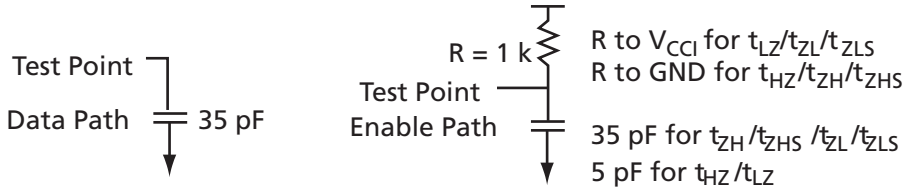


Figure 2-96 • **AC Loading**

Table 2-89 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (Typ) (V)	C_{LOAD} (pF)
0	2.5	1.2	–	35

Note: **Measuring point = V_{trip}. See Table 2-74 on page 2-126 for a complete table of trip points.*

Timing Characteristics

Table 2-90 • **2.5 V LVCMOS Low Slew**
Commercial Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 2.3 V

Drive Strength (mA)	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4mA	Std.	0.66	12.00	0.04	1.51	1.66	0.43	12.23	11.61	2.72	2.20	14.46	13.85	ns
	–1	0.56	10.21	0.04	1.29	1.41	0.36	10.40	9.88	2.31	1.87	12.30	11.78	ns
	–2	0.49	8.96	0.03	1.13	1.24	0.32	9.13	8.67	2.03	1.64	10.80	10.34	ns
8mA	Std.	0.66	8.73	0.04	1.51	1.66	0.43	8.89	8.01	3.10	2.93	11.13	10.25	ns
	–1	0.56	7.43	0.04	1.29	1.41	0.36	7.57	6.82	2.64	2.49	9.47	8.72	ns
	–2	0.49	6.52	0.03	1.13	1.24	0.32	6.64	5.98	2.32	2.19	8.31	7.65	ns
12mA	Std.	0.66	6.77	0.04	1.51	1.66	0.43	6.90	6.11	3.37	3.39	9.14	8.34	ns
	–1	0.56	5.76	0.04	1.29	1.41	0.36	5.87	5.20	2.86	2.89	7.77	7.10	ns
	–2	0.49	5.06	0.03	1.13	1.24	0.32	5.15	4.56	2.51	2.53	6.82	6.23	ns
16mA	Std.	0.66	6.31	0.04	1.51	1.66	0.43	6.42	5.73	3.42	3.52	8.66	7.96	ns
	–1	0.56	5.37	0.04	1.29	1.41	0.36	5.46	4.87	2.91	3.00	7.37	6.77	ns
	–2	0.49	4.71	0.03	1.13	1.24	0.32	4.80	4.28	2.56	2.63	6.47	5.95	ns
24mA	Std.	0.66	5.93	0.04	1.51	1.66	0.43	6.04	5.70	3.49	4.00	8.28	7.94	ns
	–1	0.56	5.05	0.04	1.29	1.41	0.36	5.14	4.85	2.97	3.40	7.04	6.75	ns
	–2	0.49	4.43	0.03	1.13	1.24	0.32	4.51	4.26	2.61	2.99	6.18	5.93	ns

Note: *For the derating values at specific junction-temperature and voltage-supply levels, refer to Table 3-6 on page 3-6.*

Table 2-91 • **2.5 V LVCMOS High Slew**
Commercial Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 2.3 V

Drive Strength (mA)	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4mA	Std.	0.66	8.82	0.04	1.51	1.66	0.43	8.13	8.82	2.72	2.29	10.37	11.05	ns
	–1	0.56	7.50	0.04	1.29	1.41	0.36	6.92	7.50	2.31	1.95	8.82	9.40	ns
	–2	0.49	6.58	0.03	1.13	1.24	0.32	6.07	6.58	2.03	1.71	7.74	8.25	ns
8mA	Std.	0.66	5.27	0.04	1.51	1.66	0.43	5.27	5.27	3.10	3.03	7.50	7.51	ns
	–1	0.56	4.48	0.04	1.29	1.41	0.36	4.48	4.48	2.64	2.58	6.38	6.38	ns
	–2	0.49	3.94	0.03	1.13	1.24	0.32	3.93	3.94	2.32	2.26	5.60	5.61	ns
12mA	Std.	0.66	3.74	0.04	1.51	1.66	0.43	3.81	3.49	3.37	3.49	6.05	5.73	ns
	–1	0.56	3.18	0.04	1.29	1.41	0.36	3.24	2.97	2.86	2.97	5.15	4.87	ns
	–2	0.49	2.80	0.03	1.13	1.24	0.32	2.85	2.61	2.51	2.61	4.52	4.28	ns
16mA	Std.	0.66	3.53	0.04	1.51	1.66	0.43	3.59	3.12	3.42	3.62	5.83	5.35	ns
	–1	0.56	3.00	0.04	1.29	1.41	0.36	3.06	2.65	2.91	3.08	4.96	4.55	ns
	–2	0.49	2.63	0.03	1.13	1.24	0.32	2.68	2.33	2.56	2.71	4.35	4.00	ns
24mA	Std.	0.66	3.26	0.04	1.51	1.66	0.43	3.32	2.48	3.49	4.11	5.56	4.72	ns
	–1	0.56	2.77	0.04	1.29	1.41	0.36	2.83	2.11	2.97	3.49	4.73	4.01	ns
	–2	0.49	2.44	0.03	1.13	1.24	0.32	2.48	1.85	2.61	3.07	4.15	3.52	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For the derating values at specific junction-temperature and voltage-supply levels, refer to Table 3-6 on page 3-6.*

1.8 V LVCMOS

Low-Voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general purpose 1.8 V applications. It uses 1.8 V input buffer and push-pull output buffer.

Table 2-92 • **Minimum and Maximum DC Input and Output Levels**

1.8 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min, V**	**Max, V**	**Min, V**	**Max, V**	**Max, V**	**Min, V**	**mA**	**mA**	**Max, mA[1]**	**Max, mA[1]**	**µA[2]**	**µA[2]**
2 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	3.6	0.45	V_{CCI} – 0.45	2	2	11	9	10	10
4 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	3.6	0.45	V_{CCI} – 0.45	4	4	22	17	10	10
6 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	3.6	0.45	V_{CCI} – 0.45	6	6	44	35	10	10
8 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	3.6	0.45	V_{CCI} – 0.45	8	8	51	45	10	10
12 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	3.6	0.45	V_{CCI} – 0.45	12	12	74	91	10	10
16 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	3.6	0.45	V_{CCI} – 0.45	16	16	74	91	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

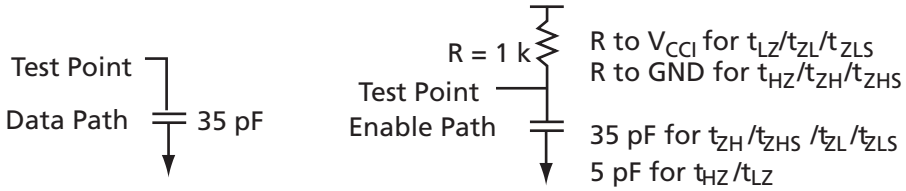


Figure 2-97 • **AC Loading**

Table 2-93 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (Typ) (V)	C_{LOAD} (pF)
0	1.8	0.9	–	35

Note: **Measuring point = V_{trip}. See Table 2-74 on page 2-126 for a complete table of trip points.*

Timing Characteristics

Table 2-94 • **1.8 V LVCMOS Low Slew**
Commercial Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 1.7 V

Drive Strength (mA)	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2mA	Std.	0.66	15.84	0.04	1.45	1.91	0.43	15.65	15.84	2.78	1.58	17.89	18.07	ns
	–1	0.56	13.47	0.04	1.23	1.62	0.36	13.31	13.47	2.37	1.35	15.22	15.37	ns
	–2	0.49	11.83	0.03	1.08	1.42	0.32	11.69	11.83	2.08	1.18	13.36	13.50	ns
4mA	Std.	0.66	11.39	0.04	1.45	1.91	0.43	11.60	10.76	3.26	2.77	13.84	12.99	ns
	–1	0.56	9.69	0.04	1.23	1.62	0.36	9.87	9.15	2.77	2.36	11.77	11.05	ns
	–2	0.49	8.51	0.03	1.08	1.42	0.32	8.66	8.03	2.43	2.07	10.33	9.70	ns
6mA	Std.	0.66	8.97	0.04	1.45	1.91	0.43	9.14	8.10	3.57	3.36	11.37	10.33	ns
	–1	0.56	7.63	0.04	1.23	1.62	0.36	7.77	6.89	3.04	2.86	9.67	8.79	ns
	–2	0.49	6.70	0.03	1.08	1.42	0.32	6.82	6.05	2.66	2.51	8.49	7.72	ns
8mA	Std.	0.66	8.35	0.04	1.45	1.91	0.43	8.50	7.59	3.64	3.52	10.74	9.82	ns
	–1	0.56	7.10	0.04	1.23	1.62	0.36	7.23	6.45	3.10	3.00	9.14	8.35	ns
	–2	0.49	6.24	0.03	1.08	1.42	0.32	6.35	5.66	2.72	2.63	8.02	7.33	ns
12mA	Std.	0.66	7.94	0.04	1.45	1.91	0.43	8.09	7.56	3.74	4.11	10.32	9.80	ns
	–1	0.56	6.75	0.04	1.23	1.62	0.36	6.88	6.43	3.18	3.49	8.78	8.33	ns
	–2	0.49	5.93	0.03	1.08	1.42	0.32	6.04	5.65	2.79	3.07	7.71	7.32	ns
16mA	Std.	0.66	7.94	0.04	1.45	1.91	0.43	8.09	7.56	3.74	4.11	10.32	9.80	ns
	–1	0.56	6.75	0.04	1.23	1.62	0.36	6.88	6.43	3.18	3.49	8.78	8.33	ns
	–2	0.49	5.93	0.03	1.08	1.42	0.32	6.04	5.65	2.79	3.07	7.71	7.32	ns

Note: *For the derating values at specific junction-temperature and voltage-supply levels, refer to Table 3-6 on page 3-6.*

Table 2-95 • **1.8 V LVCMOS High Slew**
Commercial Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 1.7 V

Drive Strength (mA)	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2mA	Std.	0.66	12.10	0.04	1.45	1.91	0.43	9.59	12.10	2.78	1.64	11.83	14.34	ns
	–1	0.56	10.30	0.04	1.23	1.62	0.36	8.16	10.30	2.37	1.39	10.06	12.20	ns
	–2	0.49	9.04	0.03	1.08	1.42	0.32	7.16	9.04	2.08	1.22	8.83	10.71	ns
4mA	Std.	0.66	7.05	0.04	1.45	1.91	0.43	6.20	7.05	3.25	2.86	8.44	9.29	ns
	–1	0.56	6.00	0.04	1.23	1.62	0.36	5.28	6.00	2.76	2.44	7.18	7.90	ns
	–2	0.49	5.27	0.03	1.08	1.42	0.32	4.63	5.27	2.43	2.14	6.30	6.94	ns
6mA	Std.	0.66	4.52	0.04	1.45	1.91	0.43	4.47	4.52	3.57	3.47	6.70	6.76	ns
	–1	0.56	3.85	0.04	1.23	1.62	0.36	3.80	3.85	3.04	2.95	5.70	5.75	ns
	–2	0.49	3.38	0.03	1.08	1.42	0.32	3.33	3.38	2.66	2.59	5.00	5.05	ns
8mA	Std.	0.66	4.12	0.04	1.45	1.91	0.43	4.20	3.99	3.63	3.62	6.43	6.23	ns
	–1	0.56	3.51	0.04	1.23	1.62	0.36	3.57	3.40	3.09	3.08	5.47	5.30	ns
	–2	0.49	3.08	0.03	1.08	1.42	0.32	3.14	2.98	2.71	2.71	4.81	4.65	ns
12mA	Std.	0.66	3.80	0.04	1.45	1.91	0.43	3.87	3.09	3.73	4.24	6.10	5.32	ns
	–1	0.56	3.23	0.04	1.23	1.62	0.36	3.29	2.63	3.18	3.60	5.19	4.53	ns
	–2	0.49	2.83	0.03	1.08	1.42	0.32	2.89	2.31	2.79	3.16	4.56	3.98	ns
16mA	Std.	0.66	3.80	0.04	1.45	1.91	0.43	3.87	3.09	3.73	4.24	6.10	5.32	ns
	–1	0.56	3.23	0.04	1.23	1.62	0.36	3.29	2.63	3.18	3.60	5.19	4.53	ns
	–2	0.49	2.83	0.03	1.08	1.42	0.32	2.89	2.31	2.79	3.16	4.56	3.98	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For the derating values at specific junction-temperature and voltage-supply levels, refer to Table 3-6 on page 3-6.*

1.5 V LVCMOS (JESD8-11)

Low-voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general purpose 1.5 V applications. It uses a 1.5 V input buffer and push-pull output buffer.

Table 2-96 • **Minimum and Maximum DC Input and Output Levels**

1.5 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min, V**	**Max, V**	**Min, V**	**Max, V**	**Max, V**	**Min, V**	**mA**	**mA**	**Max, mA[1]**	**Max, mA[1]**	**µA[2]**	**µA[2]**
2 mA	–0.3	0.30 * V_{CCI}	0.7 * V_{CCI}	3.6	0.25 * V_{CCI}	0.75 * V_{CCI}	2	2	16	13	10	10
4 mA	–0.3	0.30 * V_{CCI}	0.7 * V_{CCI}	3.6	0.25 * V_{CCI}	0.75 * V_{CCI}	4	4	33	25	10	10
6 mA	–0.3	0.30 * V_{CCI}	0.7 * V_{CCI}	3.6	0.25 * V_{CCI}	0.75 * V_{CCI}	6	6	39	32	10	10
8 mA	–0.3	0.30 * V_{CCI}	0.7 * V_{CCI}	3.6	0.25 * V_{CCI}	0.75 * V_{CCI}	8	8	55	66	10	10
12 mA	–0.3	0.30 * V_{CCI}	0.7 * V_{CCI}	3.6	0.25 * V_{CCI}	0.75 * V_{CCI}	12	12	55	66	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

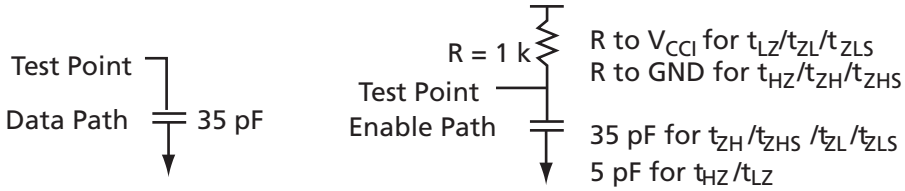


Figure 2-98 • **AC Loading**

Table 2-97 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (Typ) (V)	C_{LOAD} (pF)
0	1.5	0.75	–	35

Note: **Measuring point = V_{trip}. See Table 2-74 on page 2-126 for a complete table of trip points.*

Timing Characteristics

Table 2-98 • **1.5 V LVCMOS Low Slew**
Commercial Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 1.4 V

Drive Strength (mA)	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2mA	Std.	0.66	14.11	0.04	1.70	2.14	0.43	14.37	13.14	3.40	2.68	16.61	15.37	ns
	–1	0.56	12.00	0.04	1.44	1.82	0.36	12.22	11.17	2.90	2.28	14.13	13.08	ns
	–2	0.49	10.54	0.03	1.27	1.60	0.32	10.73	9.81	2.54	2.00	12.40	11.48	ns
4mA	Std.	0.66	11.23	0.04	1.70	2.14	0.43	11.44	9.87	3.77	3.36	13.68	12.10	ns
	–1	0.56	9.55	0.04	1.44	1.82	0.36	9.73	8.39	3.21	2.86	11.63	10.29	ns
	–2	0.49	8.39	0.03	1.27	1.60	0.32	8.54	7.37	2.81	2.51	10.21	9.04	ns
6mA	Std.	0.66	10.45	0.04	1.70	2.14	0.43	10.65	9.24	3.84	3.55	12.88	11.48	ns
	–1	0.56	8.89	0.04	1.44	1.82	0.36	9.06	7.86	3.27	3.02	10.96	9.76	ns
	–2	0.49	7.81	0.03	1.27	1.60	0.32	7.95	6.90	2.87	2.65	9.62	8.57	ns
8mA	Std.	0.66	10.02	0.04	1.70	2.14	0.43	10.20	9.23	3.97	4.22	12.44	11.47	ns
	–1	0.56	8.52	0.04	1.44	1.82	0.36	8.68	7.85	3.38	3.59	10.58	9.75	ns
	–2	0.49	7.48	0.03	1.27	1.60	0.32	7.62	6.89	2.97	3.15	9.29	8.56	ns
12mA	Std.	0.66	10.02	0.04	1.70	2.14	0.43	10.20	9.23	3.97	4.22	12.44	11.47	ns
	–1	0.56	8.52	0.04	1.44	1.82	0.36	8.68	7.85	3.38	3.59	10.58	9.75	ns
	–2	0.49	7.48	0.03	1.27	1.60	0.32	7.62	6.89	2.97	3.15	9.29	8.56	ns

Note: *For the derating values at specific junction-temperature and voltage-supply levels, refer to Table 3-6 on page 3-6.*

Table 2-99 • **1.5 V LVCMOS High Slew**
Commercial Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 1.4 V

Drive Strength (mA)	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2mA	Std.	0.66	8.53	0.04	1.70	2.14	0.43	7.26	8.53	3.39	2.79	9.50	10.77	ns
	–1	0.56	7.26	0.04	1.44	1.82	0.36	6.18	7.26	2.89	2.37	8.08	9.16	ns
	–2	0.49	6.37	0.03	1.27	1.60	0.32	5.42	6.37	2.53	2.08	7.09	8.04	ns
4mA	Std.	0.66	5.41	0.04	1.70	2.14	0.43	5.22	5.41	3.75	3.48	7.45	7.65	ns
	–1	0.56	4.60	0.04	1.44	1.82	0.36	4.44	4.60	3.19	2.96	6.34	6.50	ns
	–2	0.49	4.04	0.03	1.27	1.60	0.32	3.89	4.04	2.80	2.60	5.56	5.71	ns
6mA	Std.	0.66	4.80	0.04	1.70	2.14	0.43	4.89	4.75	3.83	3.67	7.13	6.98	ns
	–1	0.56	4.09	0.04	1.44	1.82	0.36	4.16	4.04	3.26	3.12	6.06	5.94	ns
	–2	0.49	3.59	0.03	1.27	1.60	0.32	3.65	3.54	2.86	2.74	5.32	5.21	ns
8mA	Std.	0.66	4.42	0.04	1.70	2.14	0.43	4.50	3.62	3.96	4.37	6.74	5.86	ns
	–1	0.56	3.76	0.04	1.44	1.82	0.36	3.83	3.08	3.37	3.72	5.73	4.98	ns
	–2	0.49	3.30	0.03	1.27	1.60	0.32	3.36	2.70	2.96	3.27	5.03	4.37	ns
12mA	Std.	0.66	4.42	0.04	1.70	2.14	0.43	4.50	3.62	3.96	4.37	6.74	5.86	ns
	–1	0.56	3.76	0.04	1.44	1.82	0.36	3.83	3.08	3.37	3.72	5.73	4.98	ns
	–2	0.49	3.30	0.03	1.27	1.60	0.32	3.36	2.70	2.96	3.27	5.03	4.37	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For the derating values at specific junction-temperature and voltage-supply levels, refer to Table 3-6 on page 3-6.*

3.3 V PCI, 3.3 V PCI-X

Peripheral Component Interface for 3.3 V standard specifies support for 33 MHz and 66 MHz PCI Bus applications.

Table 2-100 • **Minimum and Maximum DC Input and Output Levels**

3.3 V PCI/PCI-X	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min, V**	**Max, V**	**Min, V**	**Max, V**	**Max, V**	**Min, V**	**mA**	**mA**	**Max, mA[1]**	**Max, mA[1]**	**µA[2]**	**µA[2]**
Per PCI specification	Per PCI curves										10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

AC loadings are defined per the PCI/PCI-X specifications for the data path; Actel loadings for enable path characterization are described in Figure 2-99.

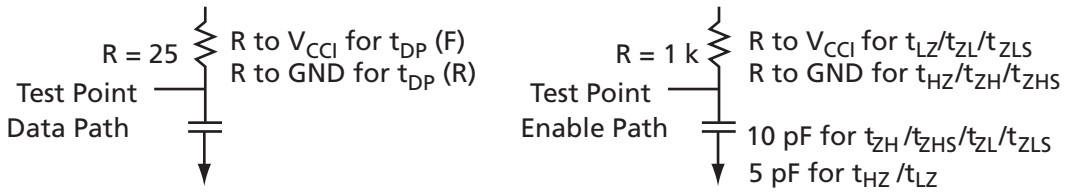


Figure 2-99 • **AC Loading**

AC loading are defined per PCI/PCI-X specifications for the data path; Actel loading for tristate is described in Table 2-101.

Table 2-101 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (Typ) (V)	C_{LOAD} (pF)
0	3.3	0.285 * V_{CCI} for $t_{DP(R)}$ 0.615 * V_{CCI} for $t_{DP(F)}$	–	10

Note: **Measuring point = V_{trip}. See Table 2-74 on page 2-126 for a complete table of trip points.*

Timing Characteristics

Table 2-102 • **3.3 V PCI/PCI-X**
Commercial Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 3.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.66	2.81	0.04	1.05	1.67	0.43	2.86	2.00	3.28	3.61	5.09	4.23	ns
–1	0.56	2.39	0.04	0.89	1.42	0.36	2.43	1.70	2.79	3.07	4.33	3.60	ns
–2	0.49	2.09	0.03	0.78	1.25	0.32	2.13	1.49	2.45	2.70	3.80	3.16	ns

Note: *For the derating values at specific junction-temperature and voltage-supply levels, refer to Table 3-6 on page 3-6.*

Voltage Referenced I/O Characteristics

3.3 V GTL

Gunning Transceiver Logic is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open drain output buffer. The V_{CCI} pin should be connected to 3.3 V.

Table 2-103 • **Minimum and Maximum DC Input and Output Levels**

3.3 V GTL	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min, V**	**Max, V**	**Min, V**	**Max, V**	**Max, V**	**Min, V**	**mA**	**mA**	**Max, mA[1]**	**Max, mA[1]**	**µA[2]**	**µA[2]**
25 mA[3]	–0.3	V_{REF} – 0.05	V_{REF} + 0.05	3.6	0.4	–	25	25	181	268	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Output drive strength is below JEDEC specification.*

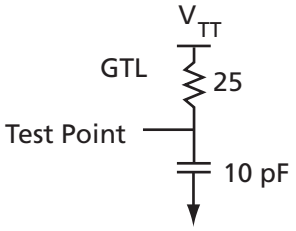


Figure 2-100 • **AC Loading**

Table 2-104 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (Typ) (V)	V_{TT} (Typ) (V)	C_{LOAD} (pF)
V_{REF} - 0.05	V_{REF} + 0.05	0.8	0.8	1.2	10

Note: **Measuring point = V_{trip}. See Table 2-74 on page 2-126 for a complete table of trip points.*

Timing Characteristics

Table 2-105 • **3.3 V GTL**
Commercial Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 3.0 V V_{REF} = 0.8 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.66	2.08	0.04	2.93	0.43	2.04	2.08			4.27	4.31	ns
–1	0.56	1.77	0.04	2.50	0.36	1.73	1.77			3.63	3.67	ns
–2	0.49	1.55	0.03	2.19	0.32	1.52	1.55			3.19	3.22	ns

Note: *For the derating values at specific junction-temperature and voltage-supply levels, refer to Table 3-6 on page 3-6.*

2.5 V GTL

Gunning Transceiver Logic is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open drain output buffer. The V_{CCI} pin should be connected to 2.5 V.

Table 2-106 • **Minimum and Maximum DC Input and Output Levels**

2.5 GTL	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min, V**	**Max, V**	**Min, V**	**Max, V**	**Max, V**	**Min, V**	**mA**	**mA**	**Max, mA[1]**	**Max, mA[1]**	**µA[2]**	**µA[2]**
25 mA[3]	–0.3	V_{REF} – 0.05	V_{REF} + 0.05	3.6	0.4	–	25	25	124	169	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Output drive strength is below JEDEC specification.*

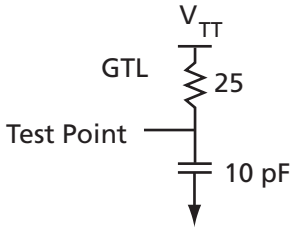


Figure 2-101 • **AC Loading**

Table 2-107 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (Typ) (V)	V_{TT} (Typ) (V)	C_{LOAD} (pF)
V_{REF} - 0.05	V_{REF} + 0.05	0.8	0.8	1.2	10

Note: **Measuring point = V_{trip}. See Table 2-74 on page 2-126 for a complete table of trip points.*

Timing Characteristics

Table 2-108 • **2.5 V GTL**
Commercial Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 3.0 V V_{REF} = 0.8 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.66	2.13	0.04	2.46	0.43	2.16	2.13			4.40	4.36	ns
–1	0.56	1.81	0.04	2.09	0.36	1.84	1.81			3.74	3.71	ns
–2	0.49	1.59	0.03	1.83	0.32	1.61	1.59			3.28	3.26	ns

Note: *For the derating values at specific junction-temperature and voltage-supply levels, refer to Table 3-6 on page 3-6.*

3.3 V GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open drain output buffer. The V_{CCI} pin should be connected to 3.3 V.

Table 2-109 • **Minimum and Maximum DC Input and Output Levels**

3.3 V GTL+	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min, V**	**Max, V**	**Min, V**	**Max, V**	**Max, V**	**Min, V**	**mA**	**mA**	**Max, mA[1]**	**Max, mA[1]**	**µA[2]**	**µA[2]**
35 mA	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.6	–	35	35	181	268	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

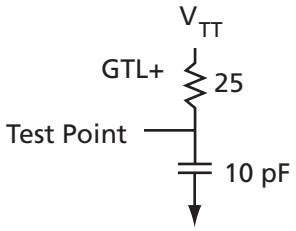


Figure 2-102 • **AC Loading**

Table 2-110 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (Typ) (V)	V_{TT} (Typ) (V)	C_{LOAD} (pF)
V_{REF} – 0.1	V_{REF} + 0.1	1.0	1.0	1.5	10

Note: **Measuring point = V_{trip}. See Table 2-74 on page 2-126 for a complete table of trip points.*

Timing Characteristics

Table 2-111 • **3.3 V GTL+**
Commercial Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 3.0 V, V_{REF} = 1.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.66	2.06	0.04	1.59	0.43	2.09	2.06			4.33	4.29	ns
–1	0.56	1.75	0.04	1.35	0.36	1.78	1.75			3.68	3.65	ns
–2	0.49	1.53	0.03	1.19	0.32	1.56	1.53			3.23	3.20	ns

Note: *For the derating values at specific junction-temperature and voltage-supply levels, refer to Table 3-6 on page 3-6.*

2.5 V GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open drain output buffer. The V_{CCI} pin should be connected to 2.5 V.

Table 2-112 • **Minimum and Maximum DC Input and Output Levels**

2.5 V GTL+	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min, V**	**Max, V**	**Min, V**	**Max, V**	**Max, V**	**Min, V**	**mA**	**mA**	**Max, mA[1]**	**Max, mA[1]**	**µA[2]**	**µA[2]**
33 mA	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.6	–	33	33	124	169	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

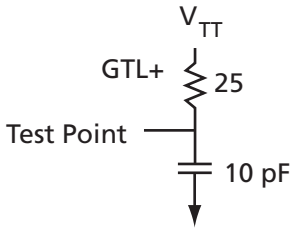


Figure 2-103 • **AC Loading**

Table 2-113 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (Typ) (V)	V_{TT} (Typ) (V)	C_{LOAD} (pF)
V_{REF} - 0.1	V_{REF} + 0.1	1.0	1.0	1.5	10

Note: **Measuring point = V_{trip}. See Table 2-74 on page 2-126 for a complete table of trip points.*

Timing Characteristics

Table 2-114 • **2.5 V GTL+**
Commercial Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 2.3 V, V_{REF} = 1.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.66	2.21	0.04	1.59	0.43	2.25	2.10			4.48	4.34	ns
–1	0.56	1.88	0.04	1.35	0.36	1.91	1.79			3.81	3.69	ns
–2	0.49	1.65	0.03	1.19	0.32	1.68	1.57			3.35	3.24	ns

Note: *For the derating values at specific junction-temperature and voltage-supply levels, refer to Table 3-6 on page 3-6.*

HSTL Class I

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). Fusion devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-115 • **Minimum and Maximum DC Input and Output Levels**

HSTL Class I	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min, V**	**Max, V**	**Min, V**	**Max, V**	**Max, V**	**Min, V**	**mA**	**mA**	**Max, mA[1]**	**Max, mA[1]**	**µA[2]**	**µA[2]**
8 mA	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCI} – 0.4	8	8	39	32	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

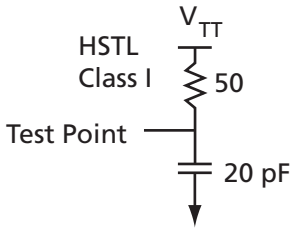


Figure 2-104 • **AC Loading**

Table 2-116 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (Typ) (V)	V_{TT} (Typ) (V)	C_{LOAD} (pF)
V_{REF} – 0.1	V_{REF} + 0.1	0.75	0.75	0.75	20

Note: **Measuring point = V_{trip}. See Table 2-74 on page 2-126 for a complete table of trip points.*

Timing Characteristics

Table 2-117 • **HSTL Class I**
Commercial Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 1.4 V, V_{REF} = 0.75 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.66	3.18	0.04	2.12	0.43	3.24	3.14			5.47	5.38	ns
–1	0.56	2.70	0.04	1.81	0.36	2.75	2.67			4.66	4.58	ns
–2	0.49	2.37	0.03	1.59	0.32	2.42	2.35			4.09	4.02	ns

Note: *For the derating values at specific junction-temperature and voltage-supply levels, refer to Table 3-6 on page 3-6.*

HSTL Class II

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). Fusion devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-118 • **Minimum and Maximum DC Input and Output Levels**

HSTL Class II	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min, V**	**Max, V**	**Min, V**	**Max, V**	**Max, V**	**Min, V**	**mA**	**mA**	**Max, mA[1]**	**Max, mA[1]**	**µA[2]**	**µA[2]**
15 mA[3]	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCI} – 0.4	15	15	55	66	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Output drive strength is below JEDEC specification.*

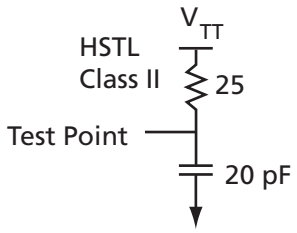


Figure 2-105 • **AC Loading**

Table 2-119 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (Typ) (V)	V_{TT} (Typ) (V)	C_{LOAD} (pF)
V_{REF} – 0.1	V_{REF} + 0.1	0.75	0.75	0.75	20

Note: **Measuring point = V_{trip}. See Table 2-74 on page 2-126 for a complete table of trip points.*

Timing Characteristics

Table 2-120 • **HSTL Class II**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 1.4 V, V_{REF} = 0.75 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.66	3.02	0.04	2.12	0.43	3.08	2.71			5.32	4.95	ns
–1	0.56	2.57	0.04	1.81	0.36	2.62	2.31			4.52	4.21	ns
–2	0.49	2.26	0.03	1.59	0.32	2.30	2.03			3.97	3.70	ns

Note: *For the derating values at specific junction-temperature and voltage-supply levels, refer to Table 3-6 on page 3-6.*

SSTL2 Class I

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). Fusion devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-121 • **Minimum and Maximum DC Input and Output Levels**

SSTL2 Class I	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min, V	Max, V	Min, V	Max, V	Max, V	Min, V	mA	mA	Max, mA[1]	Max, mA[1]	µA[2]	µA[2]
15 mA	–0.3	V_{REF} – 0.2	V_{REF} + 0.2	3.6	0.54	V_{CCI} – 0.62	15	15	87	83	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

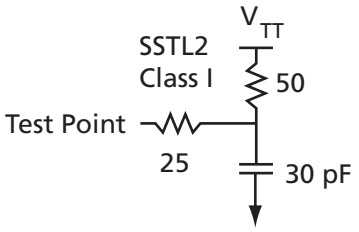


Figure 2-106 • **AC Loading**

Table 2-122 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (Typ) (V)	V_{TT} (Typ) (V)	C_{LOAD} (pF)
V_{REF} – 0.2	V_{REF} + 0.2	1.25	1.25	1.25	30

Note: **Measuring point = V_{trip}. See Table 2-74 on page 2-126 for a complete table of trip points.*

Timing Characteristics

Table 2-123 • **SSTL 2 Class I**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 2.3 V, V_{REF} = 1.25 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.66	2.13	0.04	1.33	0.43	2.17	1.85			4.40	4.08	ns
–1	0.56	1.81	0.04	1.14	0.36	1.84	1.57			3.74	3.47	ns
–2	0.49	1.59	0.03	1.00	0.32	1.62	1.38			3.29	3.05	ns

Note: *For the derating values at specific junction-temperature and voltage-supply levels, refer to Table 3-6 on page 3-6.*

SSTL2 Class II

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). Fusion devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-124 • **Minimum and Maximum DC Input and Output Levels**

SSTL2 Class II	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min, V**	**Max, V**	**Min, V**	**Max, V**	**Max, V**	**Min, V**	**mA**	**mA**	**Max, mA[1]**	**Max, mA[1]**	**µA[2]**	**µA[2]**
18 mA	–0.3	V_{REF} – 0.2	V_{REF} + 0.2	3.6	0.35	V_{CCI} – 0.43	18	18	124	169	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

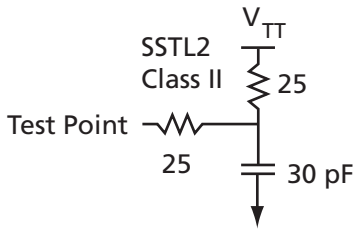


Figure 2-107 • **AC Loading**

Table 2-125 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (Typ) (V)	V_{TT} (Typ) (V)	C_{LOAD} (pF)
V_{REF} – 0.2	V_{REF} + 0.2	1.25	1.25	1.25	30

Note: **Measuring point = V_{trip}. See Table 2-74 on page 2-126 for a complete table of trip points.*

Timing Characteristics

Table 2-126 • **SSTL 2 Class II**
Commercial Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 2.3 V, V_{REF} = 1.25 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.66	2.17	0.04	1.33	0.43	2.21	1.77			4.44	4.01	ns
–1	0.56	1.84	0.04	1.14	0.36	1.88	1.51			3.78	3.41	ns
–2	0.49	1.62	0.03	1.00	0.32	1.65	1.32			3.32	2.99	ns

Note: *For the derating values at specific junction-temperature and voltage-supply levels, refer to Table 3-6 on page 3-6.*

SSTL3 Class I

Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). Fusion devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-127 • **Minimum and Maximum DC Input and Output Levels**

SSTL3 Class I	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min, V**	**Max, V**	**Min, V**	**Max, V**	**Max, V**	**Min, V**	**mA**	**mA**	**Max, mA[1]**	**Max, mA[1]**	**µA[2]**	**µA[2]**
14 mA	–0.3	V_{REF} – 0.2	V_{REF} + 0.2	3.6	0.7	V_{CCI} – 1.1	14	14	54	51	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

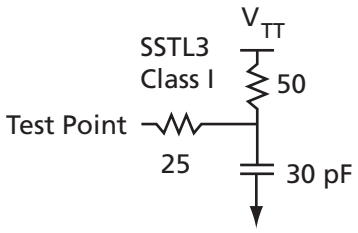


Figure 2-108 • **AC Loading**

Table 2-128 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (Typ) (V)	V_{TT} (Typ) (V)	C_{LOAD} (pF)
V_{REF} – 0.2	V_{REF} + 0.2	1.5	1.5	1.485	30

Note: **Measuring point = V_{trip}. See Table 2-74 on page 2-126 for a complete table of trip points.*

Timing Characteristics

Table 2-129 • **SSTL3 Class I**
Commercial Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 3.0 V, V_{REF} = 1.5 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.66	2.31	0.04	1.25	0.43	2.35	1.84			4.59	4.07	ns
–1	0.56	1.96	0.04	1.06	0.36	2.00	1.56			3.90	3.46	ns
–2	0.49	1.72	0.03	0.93	0.32	1.75	1.37			3.42	3.04	ns

Note: *For the derating values at specific junction-temperature and voltage-supply levels, refer to Table 3-6 on page 3-6.*

SSTL3 Class II

Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). Fusion devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-130 • **Minimum and Maximum DC Input and Output Levels**

SSTL3 Class II	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min, V**	**Max, V**	**Min, V**	**Max, V**	**Max, V**	**Min, V**	**mA**	**mA**	**Max, mA[1]**	**Max, mA[1]**	**µA[2]**	**µA[2]**
21 mA	–0.3	V_{REF} – 0.2	V_{REF} + 0.2	3.6	0.5	V_{CCI} – 0.9	21	21	109	103	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

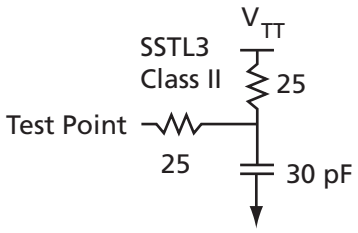


Figure 2-109 • **AC Loading**

Table 2-131 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (Typ) (V)	V_{TT} (Typ) (V)	C_{LOAD} (pF)
V_{REF} – 0.2	V_{REF} + 0.2	1.5	1.5	1.485	30

Note: **Measuring point = V_{trip}. See Table 2-74 on page 2-126 for a complete table of trip points.*

Timing Characteristics

Table 2-132 • **SSTL3- Class II**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 3.0 V, V_{REF} = 1.5 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.66	2.07	0.04	1.25	0.43	2.10	1.67			4.34	3.91	ns
–1	0.56	1.76	0.04	1.06	0.36	1.79	1.42			3.69	3.32	ns
–2	0.49	1.54	0.03	0.93	0.32	1.57	1.25			3.24	2.92	ns

Note: *For the derating values at specific junction-temperature and voltage-supply levels, refer to Table 3-6 on page 3-6.*

Differential I/O Characteristics

Configuration of the I/O modules as a differential pair is handled by the Actel Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and Double Data Rate (DDR). However, there is no support for bidirectional I/Os or tristates with these standards.

LVDS

Low-Voltage Differential Signal (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard. It requires that one data bit is carried through two signal lines; so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-110. The building blocks of the LVDS transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation, because the output standard specifications are different.

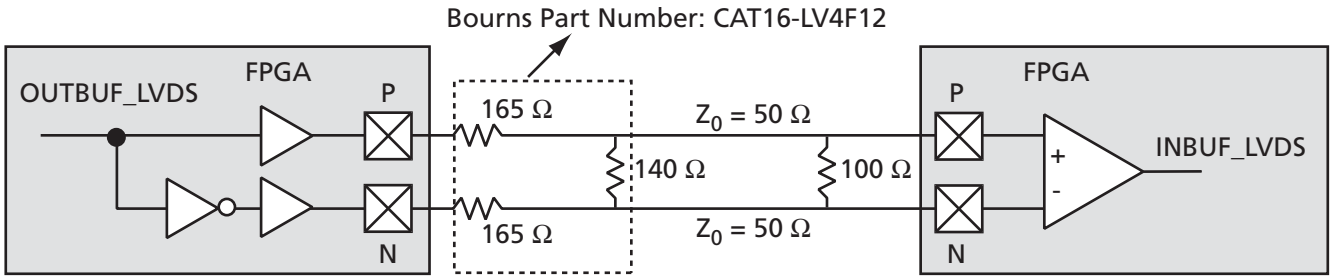


Figure 2-110 • **LVDS Circuit Diagram and Board-Level Implementation**

Table 2-133 • **Minimum and Maximum DC Input and Output Levels**

DC Parameter	Description	Min.	Typ.	Max.	Units
V_{CCI}	Supply Voltage	2.375	2.5	2.625	V
V_{OL}	Output Low Voltage	0.9	1.075	1.25	V
V_{OH}	Output High Voltage	1.25	1.425	1.6	V
V_I	Input Voltage	0		2.925	V
V_{ODIFF}	Differential Output Voltage	250	350	450	mV
V_{OCM}	Output Common Mode Voltage	1.125	1.25	1.375	V
V_{ICM}	Input Common Mode Voltage	0.05	1.25	2.35	V
V_{IDIFF}	Input Differential Voltage	100	350		mV

Notes:

1. *+/- 5%*
2. *Differential input voltage = +/-350 mV*

Table 2-134 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (Typ) (V)
1.075	1.325	Cross point	–

Note: **Measuring point = V_{trip}. See Table 2-74 on page 2-126 for a complete table of trip points.*

Timing Characteristics

Table 2-135 • **LVDS**
Commercial Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 2.3 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.66	2.10	0.04	2.02	ns
–1	0.56	1.79	0.04	1.72	ns
–2	0.49	1.57	0.03	1.51	ns

Note: *For the derating values at specific junction-temperature and voltage-supply levels, refer to Table 3-6 on page 3-6.*

BLVDS/M-LVDS

Bus LVDS (BLVDS) and Multi-Point LVDS (M-LVDS) specifications extend the existing LVDS standard to high-performance multi-point bus applications. Multidrop and multi-point bus configurations may contain any combination of drivers, receivers and transceivers. Actel LVDS drivers provide the higher drive current required by BLVDS and M-LVDS to accommodate the loading. The driver requires series terminations for better signal quality and to control voltage swing. Termination is also required at both ends of the bus since the driver can be located anywhere on the bus. These configurations can be implemented using TRIBUF_LVDS and BIBUF_LVDS macros along with appropriate terminations. Multi-point designs using Actel LVDS macros can achieve up to 200 MHz with a maximum of 20 loads. A sample application is given in Figure 2-111. The input and output buffer delays are available in the LVDS section in Table 2-135.

Example: For a bus consisting of 20 equidistant loads, the following terminations provide the required differential voltage, in worst case Industrial operating conditions, at the farthest receiver: R_S = 60 Ω and R_T = 70 Ω, given Z_0 = 50 Ω (2") and a Z_{stub} = 50 Ω (~1.5").

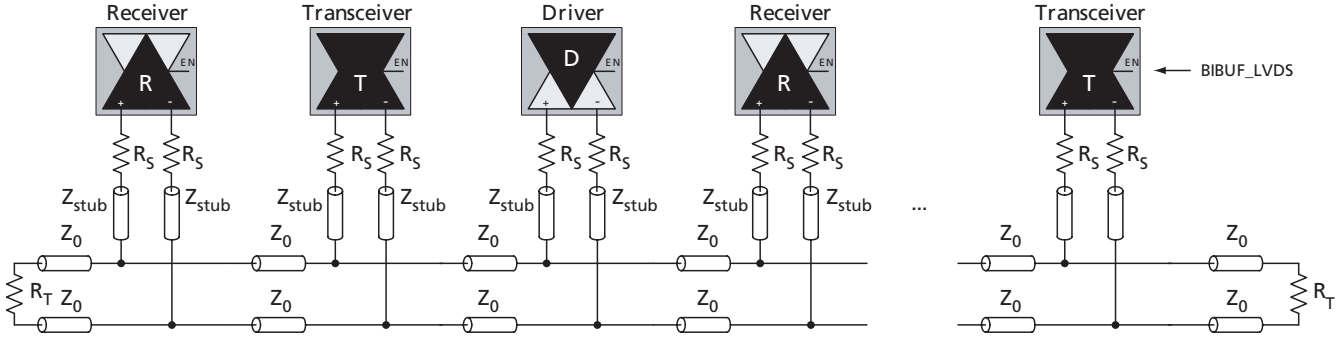


Figure 2-111 • **BLVDS/M-LVDS Multi-Point Application Using LVDS I/O Buffers**

LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit is carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-112. The building blocks of the LVPECL transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVDS implementation, because the output standard specifications are different.

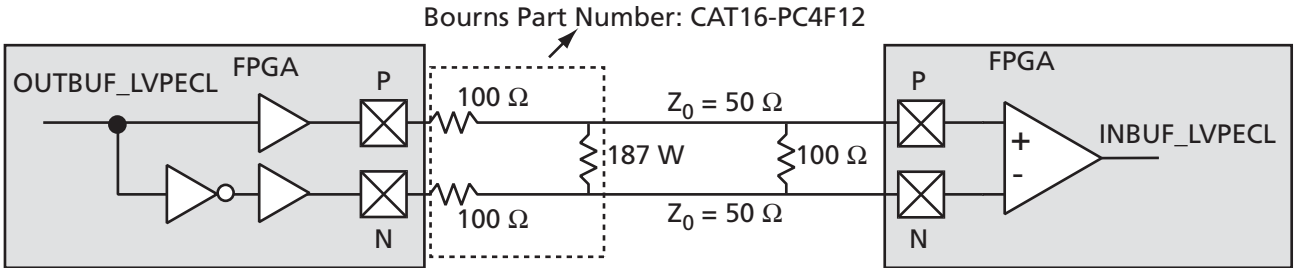


Figure 2-112 • **LVPECL Circuit Diagram and Board-Level Implementation**

Table 2-136 • **Minimum and Maximum DC Input and Output Levels**

DC Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
V_{CCI}	Supply Voltage	3.0		3.3		3.6		V
V_{OL}	Output Low Voltage	0.96	1.27	1.06	1.43	1.30	1.57	V
V_{OH}	Output High Voltage	1.8	2.11	1.92	2.28	2.13	2.41	V
V_{IL}, V_{IH}	Input Low, Input High voltages	0	3.3	0	3.6	0	3.9	V
V_{ODIFF}	Differential Output Voltage	0.625	0.97	0.625	0.97	0.625	0.97	V
V_{OCM}	Output Common Mode Voltage	1.762	1.98	1.762	1.98	1.762	1.98	V
V_{ICM}	Input Common Mode Voltage	1.01	2.57	1.01	2.57	1.01	2.57	V
V_{IDIFF}	Input Differential Voltage	300		300		300		mV

Table 2-137 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (Typ) (V)
1.64	1.94	Cross point	–

Note: **Measuring point = V_{trip}. See Table 2-74 on page 2-126 for a complete table of trip points.*

Timing Characteristics

Table 2-138 • **LVPECL**
Commercial Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 3.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.66	2.14	0.04	1.75	ns
–1	0.56	1.82	0.04	1.49	ns
–2	0.49	1.60	0.03	1.31	ns

Note: *For the derating values at specific junction-temperature and voltage-supply levels, refer to Table 3-6 on page 3-6.*

I/O Register Specifications

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

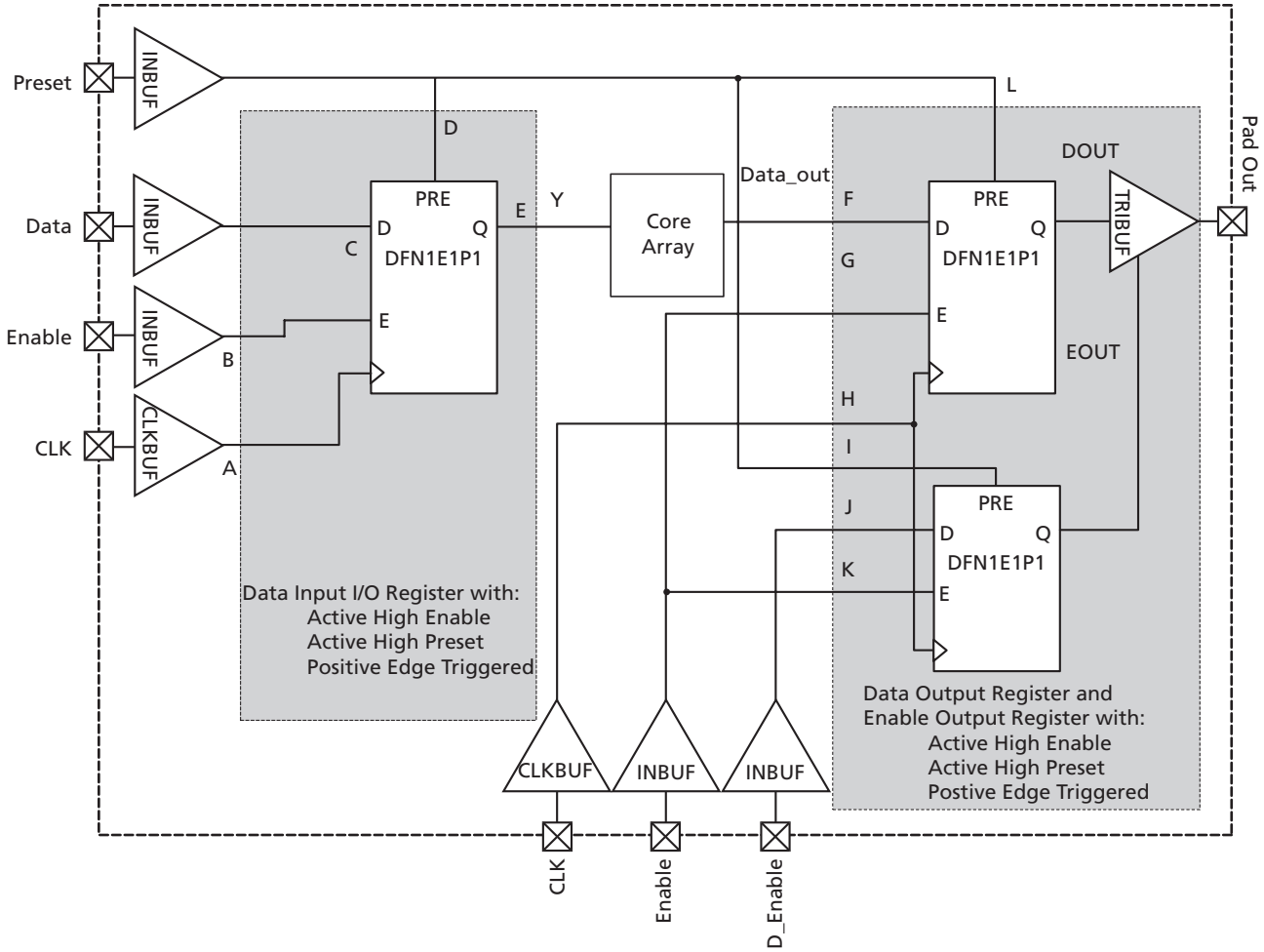


Figure 2-113 • **Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset**

Table 2-139 • **Parameter Definition and Measuring Nodes**

Parameter Name	Parameter Definition	Measuring Nodes (From, To)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	H, DOUT
t_{OSUD}	Data Setup time for the Output Data Register	F, H
t_{OHD}	Data Hold time for the Output Data Register	F, H
t_{OSUE}	Enable Setup time for the Output Data Register	G, H
t_{OHE}	Enable Hold time for the Output Data Register	G, H
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L,DOUT
$t_{OREMPRE}$	Asynchronous Preset removal time for the Output Data Register	L, H
$t_{ORECPRE}$	Asynchronous Preset Recovery time for the Output Data Register	L, H
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
t_{OESUD}	Data Setup time for the Output Enable Register	J, H
t_{OEHD}	Data Hold time for the Output Enable Register	J, H
t_{OESUE}	Enable Setup time for the Output Enable Register	K, H
t_{OEHE}	Enable Hold time for the Output Enable Register	K, H
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
$t_{OEREMPRE}$	Asynchronous Preset Removal time for the Output Enable Register	I, H
$t_{OERECPRE}$	Asynchronous Preset Recovery time for the Output Enable Register	I, H
t_{ICLKQ}	Clock-to-Q of the Input Data Register	A, E
t_{ISUD}	Data Setup time for the Input Data Register	C, A
t_{IHD}	Data Hold time for the Input Data Register	C, A
t_{ISUE}	Enable Setup time for the Input Data Register	B, A
t_{IHE}	Enable Hold time for the Input Data Register	B, A
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
$t_{IREMPRE}$	Asynchronous Preset Removal time for the Input Data Register	D, A
$t_{IRECPRE}$	Asynchronous Preset Recovery time for the Input Data Register	D, A

Note: **See Figure 2-113 on page 2-155 for more information.*

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

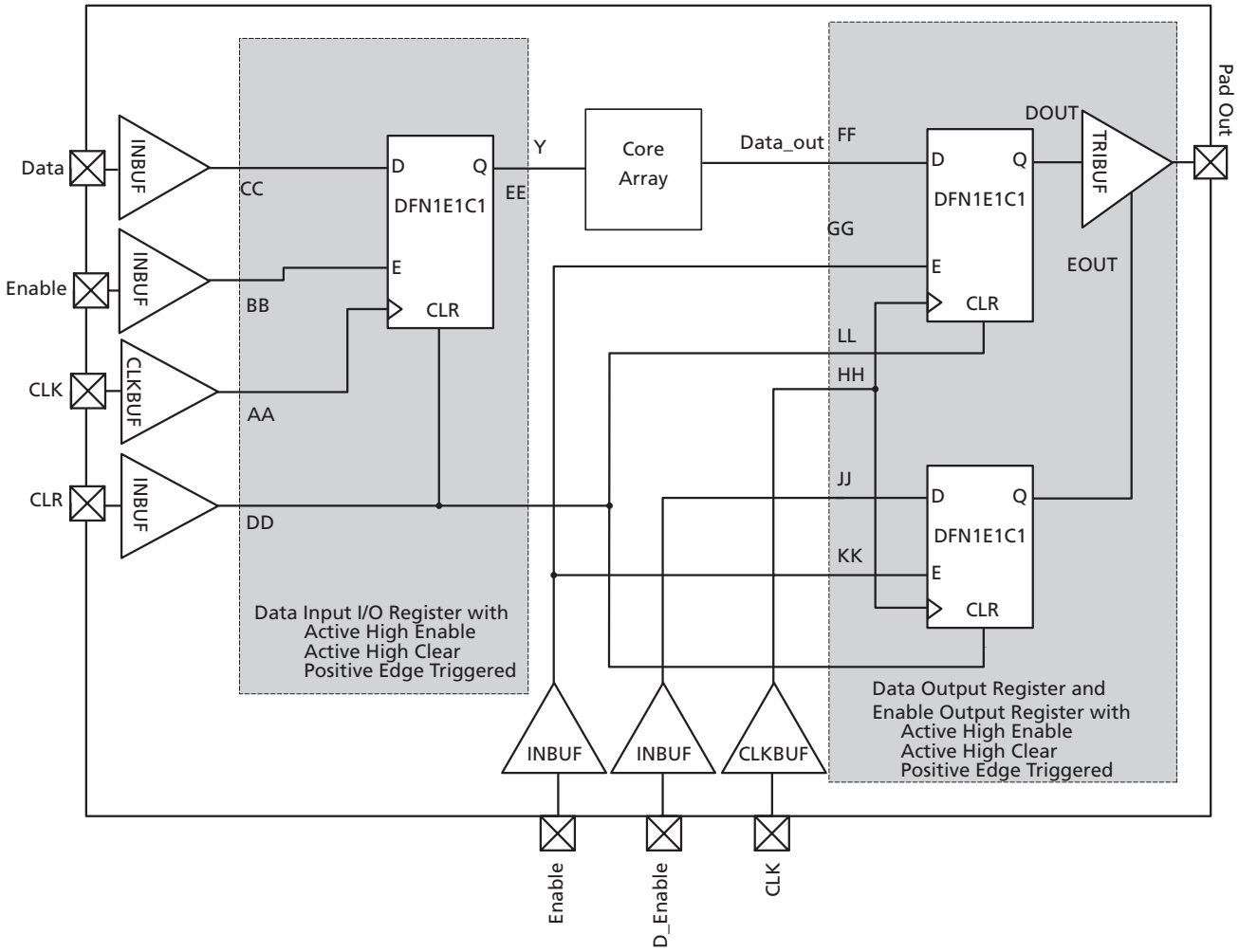


Figure 2-114 • **Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear**

Table 2-140 • **Parameter Definition and Measuring Nodes**

Parameter Name	Parameter Definition	Measuring Nodes (From, To)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	HH, DOUT
t_{OSUD}	Data Setup time for the Output Data Register	FF, HH
t_{OHD}	Data Hold time for the Output Data Register	FF, HH
t_{OSUE}	Enable Setup time for the Output Data Register	GG, HH
t_{OHE}	Enable Hold time for the Output Data Register	GG, HH
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	LL, DOUT
$t_{OREMCLR}$	Asynchronous Clear Removal time for the Output Data Register	LL, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery time for the Output Data Register	LL, HH
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	HH, EOUT
t_{OESUD}	Data Setup time for the Output Enable Register	JJ, HH
t_{OEHD}	Data Hold time for the Output Enable Register	JJ, HH
t_{OESUE}	Enable Setup time for the Output Enable Register	KK, HH
t_{OEHE}	Enable Hold time for the Output Enable Register	KK, HH
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	II, EOUT
$t_{OEREMCLR}$	Asynchronous Clear Removal time for the Output Enable Register	II, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery time for the Output Enable Register	II, HH
t_{ICLKQ}	Clock-to-Q of the Input Data Register	AA, EE
t_{ISUD}	Data Setup time for the Input Data Register	CC, AA
t_{IHD}	Data Hold time for the Input Data Register	CC, AA
t_{ISUE}	Enable Setup time for the Input Data Register	BB, AA
t_{IHE}	Enable Hold time for the Input Data Register	BB, AA
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	DD, EE
$t_{IREMCLR}$	Asynchronous Clear Removal time for the Input Data Register	DD, AA
$t_{IRECCLR}$	Asynchronous Clear Recovery time for the Input Data Register	DD, AA

Note: **See Figure 2-114 on page 2-157 for more information.*

Input Register

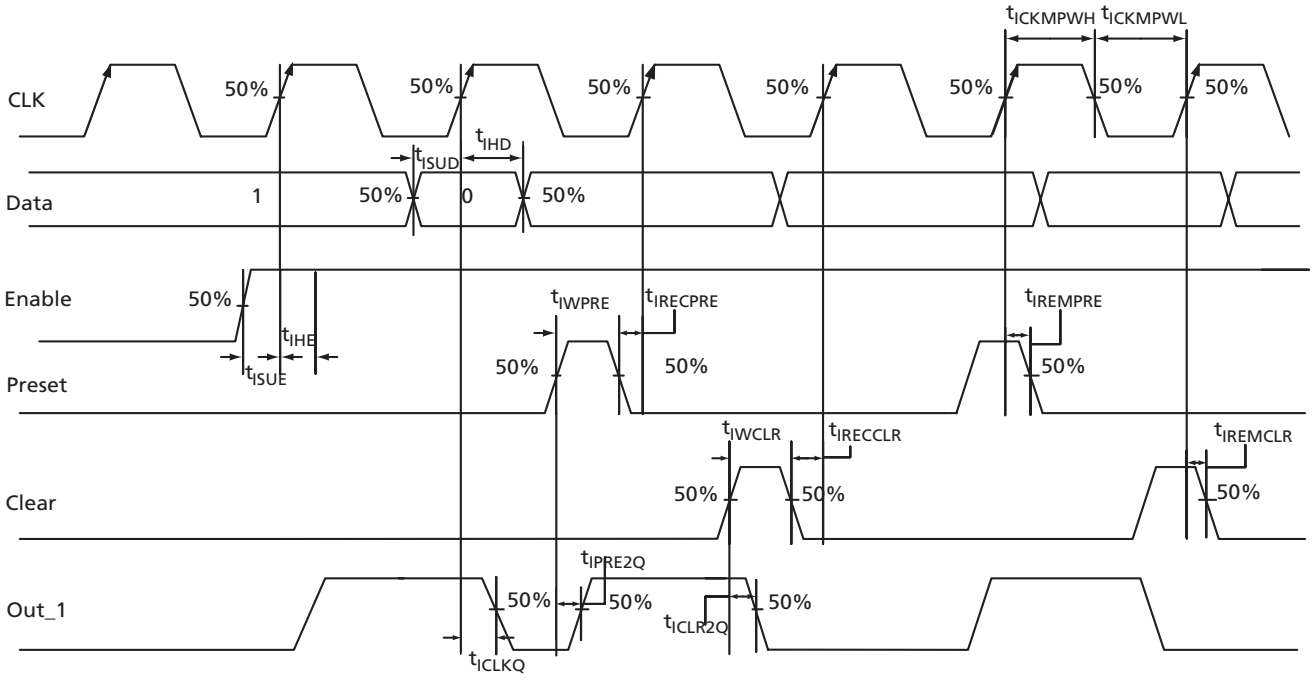


Figure 2-115 • **Input Register Timing Diagram**

Timing Characteristics

Table 2-141 • **Input Data Register Propagation Delays**
Commercial Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.63	0.71	0.84	ns
t_{ISUD}	Data Setup time for the Input Data Register	0.43	0.49	0.57	ns
t_{IHD}	Data Hold time for the Input Data Register	0.00	0.00	0.00	ns
t_{ISUE}	Enable Setup time for the Input Data Register	0.43	0.49	0.57	ns
t_{IHE}	Enable Hold time for the Input Data Register	0.00	0.00	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.63	0.71	0.84	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.45	0.51	0.60	ns
$t_{IREMCLR}$	Asynchronous Clear Removal time for the Input Data Register	0.00	0.00	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery time for the Input Data Register	0.22	0.25	0.30	ns
$t_{IREMPRE}$	Asynchronous Preset Removal time for the Input Data Register	0.00	0.00	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery time for the Input Data Register	0.22	0.25	0.30	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.25	0.28	0.33	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.25	0.28	0.33	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width High for the Input Data Register	0.36	0.41	0.48	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width Low for the Input Data Register	0.41	0.46	0.54	ns

Note: *For the derating values at specific junction-temperature and voltage-supply levels, refer to Table 3-6 on page 3-6.*

Output Register

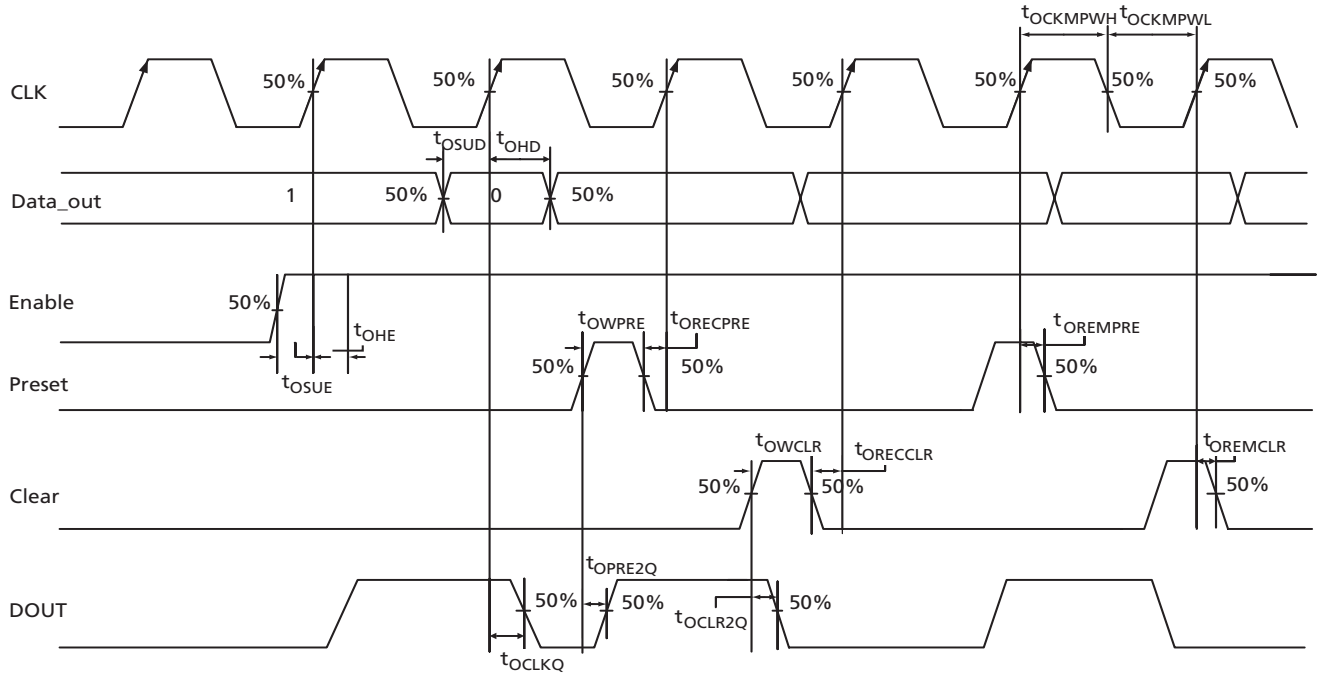


Figure 2-116 • **Output Register Timing Diagram**

Timing Characteristics

Table 2-142 • **Output Data Register Propagation Delays**
Commercial Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.63	0.71	0.84	ns
t_{OSUD}	Data Setup time for the Output Data Register	0.43	0.49	0.57	ns
t_{OHD}	Data Hold time for the Output Data Register	0.00	0.00	0.00	ns
t_{OSUE}	Enable Setup time for the Output Data Register	0.43	0.49	0.57	ns
t_{OHE}	Enable Hold time for the Output Data Register	0.00	0.00	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	0.63	0.71	0.84	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	0.45	0.51	0.60	ns
$t_{OREMCLR}$	Asynchronous Clear Removal time for the Output Data Register	0.00	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery time for the Output Data Register	0.22	0.25	0.30	ns
$t_{OREMPRE}$	Asynchronous Preset Removal time for the Output Data Register	0.00	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery time for the Output Data Register	0.22	0.25	0.30	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.25	0.28	0.33	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.25	0.28	0.33	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width High for the Output Data Register	0.36	0.41	0.48	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width Low for the Output Data Register	0.41	0.46	0.54	ns

Note: *For the derating values at specific junction-temperature and voltage-supply levels, refer to Table 3-6 on page 3-6.*

Output Enable Register

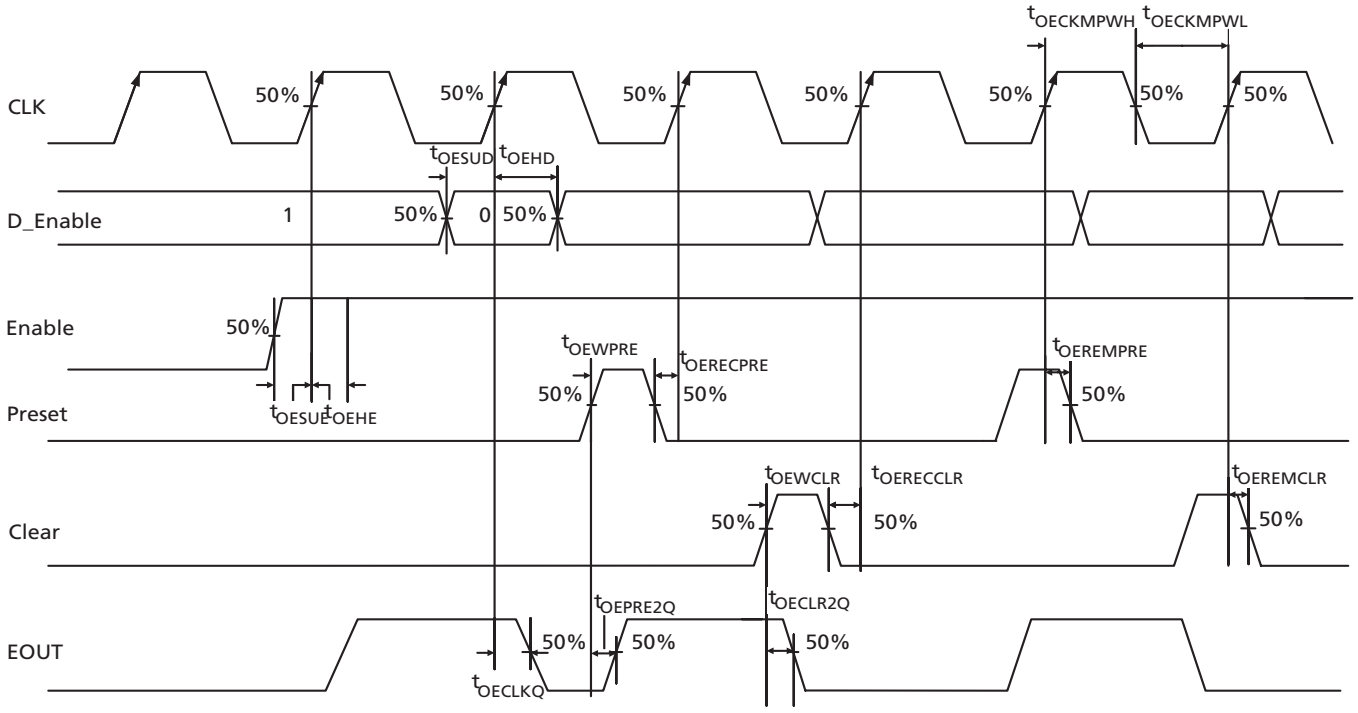


Figure 2-117 • **Output Enable Register Timing Diagram**

Timing Characteristics

Table 2-143 • **Output Enable Register Propagation Delays**
Commercial Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	0.63	0.71	0.84	ns
t_{OESUD}	Data Setup time for the Output Enable Register	0.43	0.49	0.57	ns
t_{OEHD}	Data Hold time for the Output Enable Register	0.00	0.00	0.00	ns
t_{OESUE}	Enable Setup time for the Output Enable Register	0.43	0.49	0.57	ns
t_{OEHE}	Enable Hold time for the Output Enable Register	0.00	0.00	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	0.63	0.71	0.84	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	0.45	0.51	0.60	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal time for the Output Enable Register	0.00	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery time for the Output Enable Register	0.22	0.25	0.30	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal time for the Output Enable Register	0.00	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery time for the Output Enable Register	0.22	0.25	0.30	ns
t_{OEWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.25	0.28	0.33	ns
t_{OEWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.25	0.28	0.33	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width High for the Output Enable Register	0.36	0.41	0.48	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width Low for the Output Enable Register	0.41	0.46	0.54	ns

Note: *For the derating values at specific junction-temperature and voltage-supply levels, refer to Table 3-6 on page 3-6.*

DDR Module Specifications

Input DDR Module

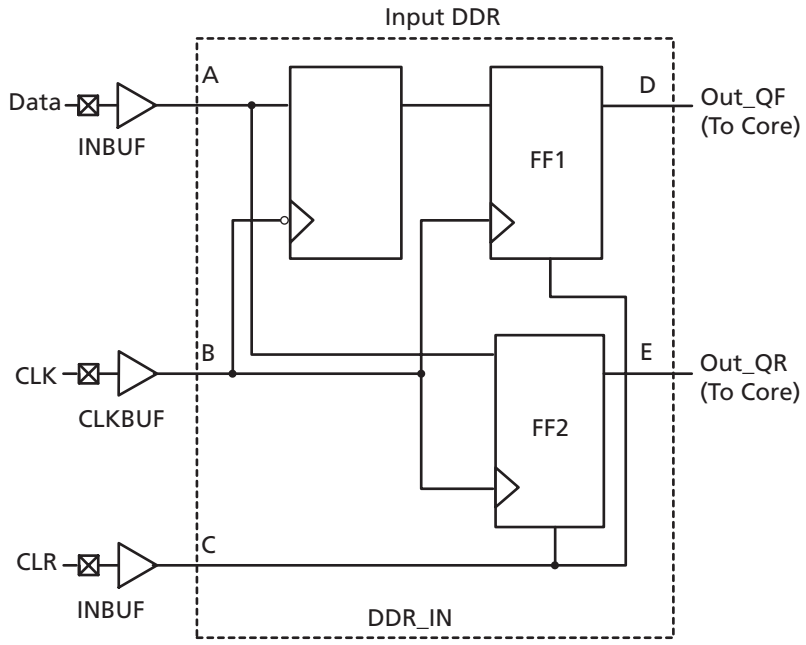


Figure 2-118 • **Input DDR Timing Model**

Table 2-144 • **Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (From, To)
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR	B, D
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF	B, E
$t_{DDRISUD}$	Data Setup time of DDR input	A, B
t_{DDRIHD}	Data Hold time of DDR input	A, B
$t_{DDRICLR2Q1}$	Clear-to-Out Out_QR	C, D
$t_{DDRICLR2Q2}$	Clear-to-Out Out_QF	C, E
$t_{DDRIREMCLR}$	Clear Removal	C, B
$t_{DDRIRECCLR}$	Clear Recovery	C, B

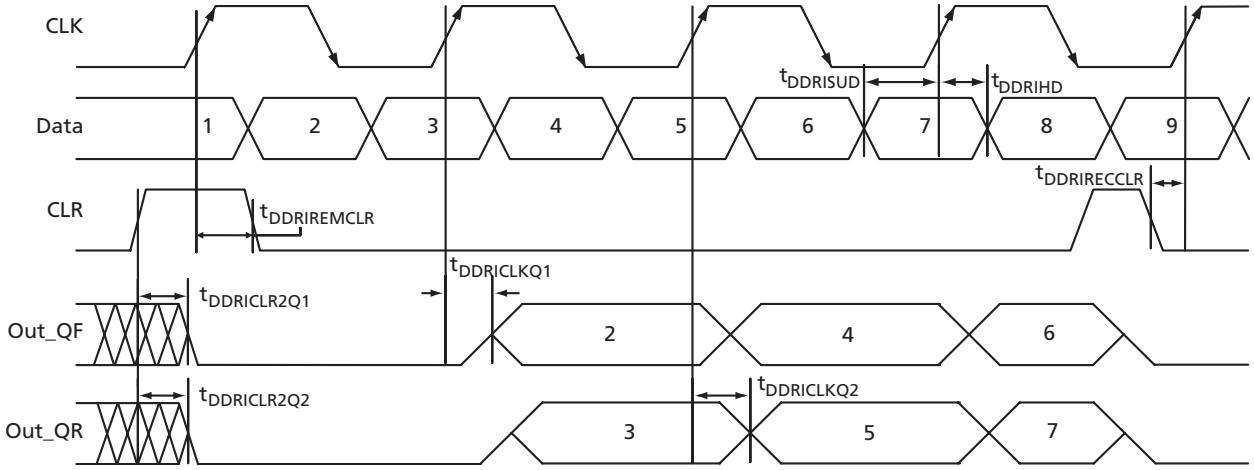


Figure 2-119 • **Input DDR Timing Diagram**

Timing Characteristics

Table 2-145 • **Input DDR Propagation Delays**
Commercial Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V

Parameter	Description	–2	–1	Std.	Units
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR for Input DDR	0.63	0.71	0.84	ns
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF for Input DDR	0.57	0.65	0.76	ns
$t_{DDRISUD}$	Data Setup for Input DDR	0.53	0.61	0.71	ns
t_{DDRIHD}	Data Hold for Input DDR	0.00	0.00	0.00	ns
$t_{DDRICLR2Q1}$	Asynchronous Clear to Out Out_QR for Input DDR	0.57	0.65	0.76	ns
$t_{DDRICLR2Q2}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.57	0.65	0.76	ns
$t_{DDRIREMCLR}$	Asynchronous Clear Removal time for Input DDR	0.00	0.00	0.00	ns
$t_{DDRIRECCLR}$	Asynchronous Clear Recovery time for Input DDR	0.22	0.25	0.30	ns
$t_{DDRIWCLR}$	Asynchronous Clear Minimum Pulse Width for Input DDR				ns
$t_{DDRICKMPWH}$	Clock Minimum Pulse Width High for Input DDR				ns
$t_{DDRICKMPWL}$	Clock Minimum Pulse Width Low for Input DDR				ns
$F_{DDRIMAX}$	Maximum Frequency for Input DDR				MHz

Note: *For the derating values at specific junction-temperature and voltage-supply levels, refer to Table 3-6 on page 3-6.*

Output DDR

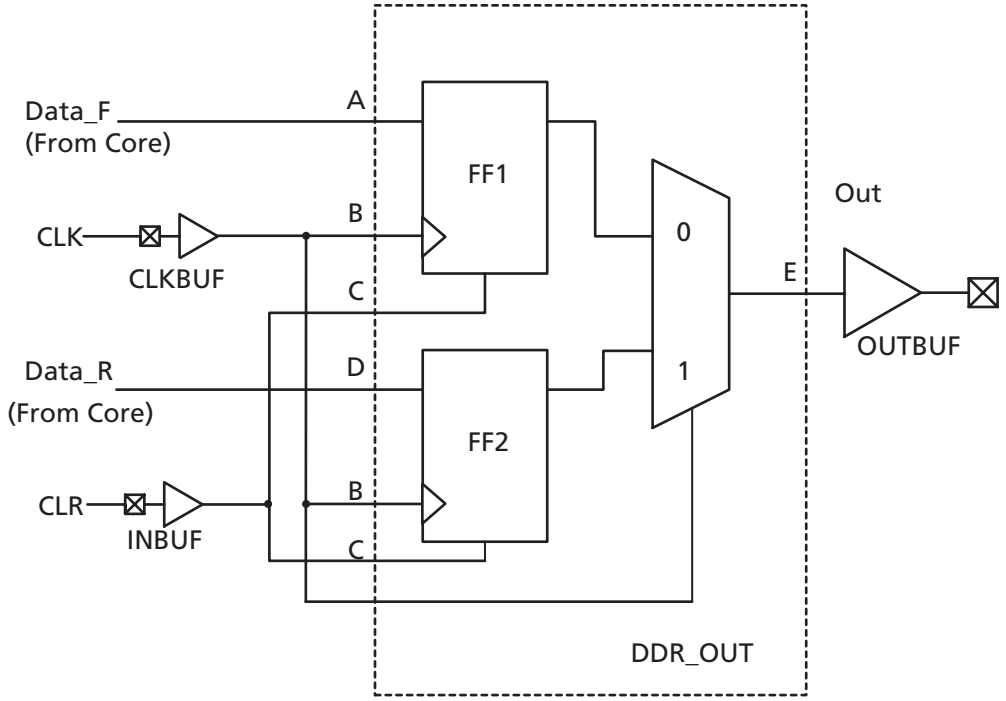


Figure 2-120 • **Output DDR Timing Model**

Table 2-146 • **Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (From, To)
$t_{DDROCLKQ}$	Clock-to-Out	B, E
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out	C, E
$t_{DDROREMCLR}$	Clear Removal	C, B
$t_{DDRORECCLR}$	Clear Recovery	C, B
$t_{DDROSUD1}$	Data Setup Data_F	A, B
$t_{DDROSUD2}$	Data Setup Data_R	D, B
$t_{DDROHD1}$	Data Hold Data_F	A, B
$t_{DDROHD2}$	Data Hold Data_R	D, B

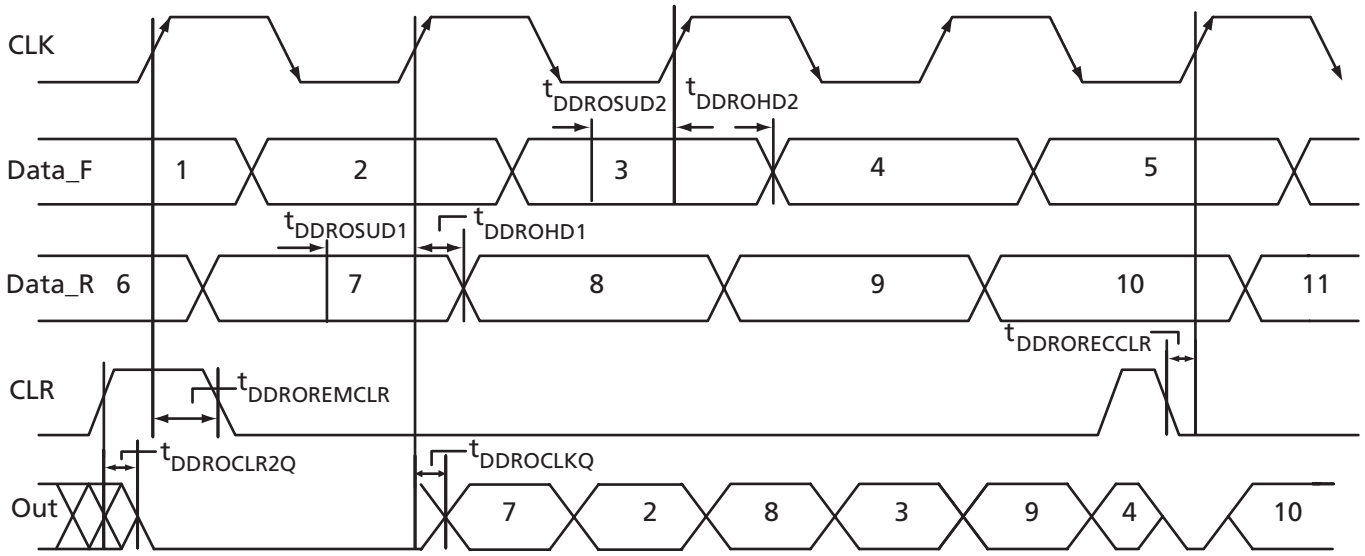


Figure 2-121 • **Output DDR Timing Diagram**

Timing Characteristics

Table 2-147 • **Output DDR Propagation Delays**
Commercial Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V

Parameter	Description	–2	–1	Std.	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	0.63	0.71	0.84	ns
$t_{DDROSUD1}$	Data_F Data Setup for Output DDR	0.43	0.49	0.57	ns
$t_{DDROSUD2}$	Data_R Data Setup for Output DDR	0.43	0.49	0.57	ns
$t_{DDROHD1}$	Data_F Data Hold for Output DDR	0.00	0.00	0.00	ns
$t_{DDROHD2}$	Data_R Data Hold for Output DDR	0.00	0.00	0.00	ns
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out for Output DDR	0.57	0.65	0.76	ns
$t_{DDROREMCLR}$	Asynchronous Clear Removal time for Output DDR	0.00	0.00	0.00	ns
$t_{DDRORECCLR}$	Asynchronous Clear Recovery time for Output DDR	0.22	0.25	0.30	ns
$t_{DDROWCLR1}$	Asynchronous Clear Minimum Pulse Width for Output DDR				ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width High for the Output DDR				ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width Low for the Output DDR				ns
F_{DDOMAX}	Maximum Frequency for the Output DDR				MHz

Note: *For the derating values at specific junction-temperature and voltage-supply levels, refer to Table 3-6 on page 3-6.*

Pin Descriptions

Supply Pins

GND **Ground**

Ground supply voltage to the core, I/O outputs, and I/O logic.

GNDQ **Ground (quiet)**

Quiet ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package, and improves input signal integrity. GNDQ needs to always be connected on the board to GND.

ADCGNDREF **Analog Reference Ground**

Analog ground reference used by the ADC. This pad should be connected to a quiet analog ground.

GNDA **Ground (analog)**

Quiet ground supply voltage to the Analog Block of the Fusion devices. The use of a separate analog ground helps isolate the analog functionality of the Fusion device from any digital switching noise.

GNDAQ **Ground (analog quiet)**

Quiet ground supply voltage to the analog I/O of the Fusion devices. The use of a separate analog ground helps isolate the analog functionality of the Fusion device from any digital switching noise.

GNDNVM **Flash Memory Ground**

Ground supply used by the Fusion device's Flash memory block module(s).

GNDOSC **Oscillator Ground**

Ground supply for both integrated RC oscillator and crystal oscillator circuit.

V_{CC15A} **Analog Power Supply (1.5 V)**

1.5 V clean analog power supply input for use by the 1.5 V portion of the analog circuitry.

V_{CC33A} **Analog Power Supply (3.3 V)**

3.3 V clean analog power supply input for use by the 3.3 V portion of the analog circuitry.

V_{CC33N} **Negative 3.3 V output**

VOLTAGE CONVERTER OUTPUT is the –3.3 V output from the voltage converter. A 2.2 µF capacitor must be connected from this pin to ground.

$V_{CC33PMP}$ **Analog Power Supply (3.3 V)**

3.3 V clean analog power supply input for use by the analog charge pump.

V_{CCNVM} **Flash Memory Block Power Supply (1.5 V)**

1.5 V power supply used by the Fusion device's Flash memory block module(s).

V_{CCOSC} **Oscillator Power Supply (3.3 V)**

Power supply for both integrated RC oscillator and crystal oscillator circuit.

V_{CC} **Core Supply Voltage**

Supply voltage to the FPGA core, nominal 1.5 V. V_{CC} is also required for powering the JTAG state machine in addition to V_{JTAG}. Even when a Fusion device is in bypass mode in a JTAG chain of interconnected devices, both V_{CC} and V_{JTAG} must remain powered to allow JTAG signals to pass through the Fusion device.

V_{CCI}Bx **I/O Supply Voltage**

Supply voltage to the bank's I/O output buffers and I/O logic. Bx is the I/O bank number. There are either 4 (AFS090 and AFS250) or 5 (AFS600 and AFS1500) I/O banks on the Fusion devices plus a dedicated V_{JTAG} bank.

Each bank can have a separate V_{CCI} connection. All I/Os in a bank will run off the same V_{CCI}Bx supply. V_{CCI} can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V nominal voltage. Unused I/O banks should have their corresponding V_{CCI} pins tied to GND.

VMVx **I/O Supply Voltage (quiet)**

Quiet supply voltage to the input buffers of each I/O bank. X is the bank number. Within the package, the VMV plane is decoupled from the simultaneous switching noise originated from the output buffer V_{CCI} domain. This minimizes the noise transfer within the package, and improves input signal integrity. Each bank must have at least one VMV connection. All I/Os in a bank run off the same VMVx supply. VMV is used to provide a quiet supply voltage to the input buffers of each I/O bank. VMVx can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V nominal voltage. Unused I/O banks should have their corresponding VMV pins tied to GND. VMV and V_{CCI} should be at the same voltage within a given I/O bank. Used VMV pins must be connected to the corresponding V_{CCI} pins of the same bank (i.e., VMV0 to V_{CCI}B0, VMV1 to V_{CCI}B1, etc.).

$V_{CCPLA/B}$ **PLL Supply Voltage**

Supply voltage to analog PLL, nominal 1.5 V, where A and B refer to the PLL. The AFS090 and AFS250 each have a single PLL. The AFS600 and AFS1500 devices each have two PLLs. If unused, $V_{CCPLA/B}$ should be tied to GND.

V_{COMPLF} PLL Ground8

Ground to analog PLL, where A and B refer to the PLL. The AFS090 and AFS250 each have a single PLL. The AFS600 and AFS1500 devices each have two PLLs. Unused V_{COMPLF} pin should be connected to GND.

V_{JTAG} JTAG Supply Voltage

Fusion devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). Isolating the JTAG power supply in a separate I/O bank gives greater flexibility with supply selection and simplifies power supply and printed circuit board design. If the JTAG interface is not used nor planned to be used, the V_{JTAG} pin together with the TRST pin could be tied to GND. It should be noted that V_{CC} is required to be powered for JTAG operation; V_{JTAG} alone is insufficient. If a Fusion device is in a JTAG chain of interconnected boards, and it is desired to power down the board containing the Fusion device, this may be done provided both V_{JTAG} and V_{CC} to the Fusion part remain powered; otherwise, JTAG signals will not be able to transition the Fusion device, even in bypass mode.

V_{PUMP} Programming Supply Voltage

Fusion devices support single-voltage ISP programming of the configuration Flash and FlashROM. For programming, V_{PUMP} should be 3.3 V nominal. During normal device operation, V_{PUMP} can be left floating or can be tied (pulled up) to any voltage between 0 V and 3.6 V.

User-Defined Supply Pins

V_{REF} I/O Voltage Reference

Reference voltage for I/O minibanks. Both the AFS600 (north bank only) and AFS1500 (all digital I/O banks) support Actel Pro I/O. These I/O banks support voltage reference standard I/O. The V_{REF} pins are configured by the user from regular I/Os, and any I/O in a bank, except JTAG I/Os, which can be designated as the voltage reference I/O. Only certain I/O standards require a voltage reference – HSTL (I) and (II), SSTL2 (I) and (II), SSTL3 (I) and (II), and GTL/GTL+. One VREF pin can support the number of I/Os available in its minibank.

VAREF Analog Reference Voltage

Analog reference voltage to be used by analog to digital converter. The Fusion device provides a 2.56 V internal reference voltage that can be used by the ADC. Optionally this voltage can be configured to be brought out on this pin for use by the system. The pin in this can would either open or 2.56 V output.

If a different reference voltage is required, it can be supplied on this pin and used by the ADC. The valid range of values that can be supplied to the ADC is between 1. 0 V and 3.3 V.

User Pins

I/O User Input/Output

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output signal levels are compatible with the I/O standard selected. Unused I/O pins are configured as inputs with pull-up resistors.

During programming, I/Os become tristated and weakly pulled up to V_{CCI}. With V_{CCI}, VMV and V_{CC} supplies continuously powered-up, and the device transitions from programming to operating mode, the I/Os get instantly configured to the desired user configuration.

Axy Analog Input/Output

Analog I/O pin where x is the analog pad type (C = current pad, G = Gate driver pad, T = Temperature pad, V = Voltage pad) and y is the Analog Quad number (0 to 9).

ATRTNx Temperature Monitor Return

AT RETURN are the returns for the temperature sensors. The cathode terminal of the external diodes should be connected to these pins. There is 1 analog return pin for every two analog quads. The x in the ATRTNx designator indicates the quad pairing (x = 0 for AQ1 and AQ2, x = 1 for AQ2 and AQ3..., x = 4 for AQ8 and AQ9). These signals that drive these pins are called out as ATRETUNxy in the software (where x and y refer to the quads that share the return signal).

GL Globals

GL I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as Pro I/Os, since they have identical capabilities. Unused GL pins are configured as inputs with pull-up resistors. See more detailed descriptions of global I/O connectivity in the "Clock Conditioning Circuits" section on page 2-22.

Refer to the "User I/O Naming Convention" section on page 2-118 for a description of naming of global pins.

JTAG Pins

Fusion devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). V_{CC} must also be powered in order for the JTAG state machine to operate even if the device is in bypass mode; V_{JTAG} alone is insufficient. Both V_{JTAG} and V_{CC} to the Fusion part must be supplied to allow JTAG signals to transition the Fusion device. Isolating the JTAG power supply.

in a separate I/O bank gives greater flexibility with supply selection and simplifies power supply and printed circuit board design. If the JTAG interface is not used nor planned to be used, the V_{JTAG} pin together with the TRST pin could be tied to GND.

TCK Test Clock

Test clock input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/down resistor. If JTAG is not used, Actel recommends tying off TCK to GND or V_{JTAG} through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state.

Note that to operate at all V_{JTAG} voltages, 500 Ω to 1 kΩ will satisfy the requirements. Refer to Table 2-148 for more information.

Table 2-148 • **Recommended Tie-Off Values for the TCK and TRST Pins**

V_{JTAG}	Tie Off Resistance[2, 3]
V_{JTAG} at 3.3 V	200 Ω to 1 kΩ
V_{JTAG} at 2.5 V	200 Ω to 1 kΩ
V_{JTAG} at 1.8 V	500 Ω to 1 kΩ
V_{JTAG} at 1.5 V	500 Ω to 1 kΩ

Notes:

1. *Equivalent parallel resistance if more than one device is on JTAG chain.*
2. *The TCK pin can be pulled-up/down.*
3. *The TRST pin can only be pulled-down.*

Note that to operate at all V_{JTAG} voltages, 500 Ω to 1 kΩ will satisfy the requirements.

TDI Test Data Input

Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.

TDO Test Data Output

Serial output for JTAG boundary scan, ISP, and UJTAG usage.

TMS Test Mode Select

The TMS pin controls the use of the IEEE1532 boundary scan pins (TCK,TDI, TDO, TRST). There is an internal weak pull-up resistor on the TMS pin.

TRST Boundary Scan Reset Pin

The TRST pin functions as an active low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor could be included to ensure the TAP is held in reset mode. The resistor values must be chosen from Table 2-148 and must satisfy the parallel resistance value requirement. The values in Table 2-148 correspond to the resistor recommended when a single device is used and to the equivalent parallel resistor when multiple devices are connected via a JTAG chain.

In critical applications, an upset in the JTAG circuit could allow entering an undesired JTAG state. In such cases, Actel recommends tying off TRST to GND through a resistor placed close to the FPGA pin.

Note that to operate at all V_{JTAG} voltages, 500 Ω to 1 kΩ will satisfy the requirements.

Special Function Pins

NC No Connect

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

DC Don't Connect

This pin should not be connected to any signals on the printed circuit board (PCB). These pins should be left un-connected.

NCAP Negative Capacitor

NEGATIVE CAPACITOR is where the negative terminal of the charge pump capacitor is connected.

PCAP Positive Capacitor

POSITIVE CAPACITOR is where the positive terminal of the charge pump capacitor is connected.

PUB Power Up Bar

PUSH BUTTON is the connection for the external momentary switch which is used to turn on the 1.5 V voltage regulator.

PTBASE Pass Transistor Base

PASS TRANSISTOR BASE is the control signal of the voltage regulator. This pin should be connected to the base of the external pass transistor used with the 1.5 V internal voltage regulator.

PTEM Pass Transistor Emitter

PASS TRANSISTOR EMITTER is the feedback input of the voltage regulator.

This pin should be connected to the Emitter of the external pass transistor used with the 1.5 V internal voltage regulator.

$V_{CC33ACAP}$ Analog Power Filter

Analog power pin for the analog power supply low pass filter. An external 1 µF capacitor should be connected between this pin and ground.

XTAL1 Crystal Oscillator Circuit Input

Input to crystal oscillator circuit. Pin for connecting external crystal, ceramic resonator, RC network, or external clock input. When using an external crystal or ceramic oscillator external capacitors are also recommended (< 2 MHz 100 pF, > 2 MHz – 15 pF).

If using external RC network or clock input, XTAL1 should be used and XTAL2 left unconnected.

XTAL2 Crystal Oscillator Circuit Input

Input to crystal oscillator circuit. Pin for connecting external crystal, ceramic resonator, RC network, or external clock input. When using an external crystal or ceramic oscillator external capacitors are also recommended (<2 MHz 100 pF, >2 MHz – 15 pF).

If using external RC network or clock input, XTAL1 should be used and XTAL2 left unconnected.

Software Tools and Programming

Overview of Tools Flow

The Fusion family of FPGAs is fully supported by both Actel Libero IDE and Designer FPGA Development software. Actel Libero IDE is an integrated design manager that seamlessly integrates design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Additionally, Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment (see the *Libero IDE flow diagram* located on the Actel website). Libero IDE includes Synplify® AE from Synplicity®, ViewDraw® AE from Mentor Graphics®, Model*Sim*® HDL Simulator from Mentor Graphics, WaveFormer Lite™ AE from SynaptiCAD®, PALACE™ AE Physical Synthesis from Magma Design Automation™, and Designer software from Actel.

Actel Designer software is a place-and-route tool and provides a comprehensive suite of back-end support tools for FPGA development. The Designer software includes the following:

- SmartTime – a world-class integrated static timing analyzer and constraints editor that supports timing-driven place-and-route
- NetlistViewer – a design netlist schematic viewer
- ChipPlanner – a graphical floorplanning viewer and editor
- SmartPower – a sophisticated power analysis environment that gives designers the ability to quickly determine the power consumption of an FPGA or its components
- PinEditor – a graphical application for editing pin assignments and I/O attributes
- I/O Attribute Editor – displays all assigned and unassigned I/O macros and their attributes in a spreadsheet format

With the Designer software, a user can lock the design pins before layout while minimally impacting the results of place-and-route. Additionally, the Actel back-annotation flow is compatible with all the major simulators. Included in the Designer software is SmartGen core generator, which easily creates commonly used logic functions for implementation into your Fusion-based schematic or HDL design.

Actel Designer software is compatible with the most popular FPGA design entry and verification tools from EDA vendors, such as Cadence®, Magma®, Mentor Graphics, Synopsys, and Synplicity. The Designer software is available for both the Windows® and UNIX operating systems.

CoreMP7 Software Tools

CoreConsole is the Intellectual Property Deployment Platform (IDP) that assists the developer in programming the soft ARM (CoreMP7) core onto M7 Fusion devices. CoreConsole provides the seamless environment to work with Libero IDE and Designer FPGA development software tools concurrently.

Security

Fusion devices have a built-in 128-bit AES decryption core. The decryption core facilitates secure, in-system programming of the FPGA core array fabric and the FlashROM. The FlashROM and the FPGA core fabric can be programmed independently from each other, allowing the FlashROM to be updated without the need for change to the FPGA core fabric. The AES master key is stored in on-chip nonvolatile memory (Flash). The AES master key can be preloaded into parts in a secure programming environment (such as the Actel in-house programming center) and then "blank" parts can be shipped to an untrusted programming or manufacturing center for final personalization with an AES encrypted bitstream. Late stage product changes or personalization can be implemented easily and securely by simply sending a STAPL file with AES encrypted data. Secure remote field updates over public networks (such as the Internet) are possible by sending and programming a STAPL file with AES encrypted data. For more information, refer to the *Fusion Security* application note.

128-Bit AES Decryption

The 128-bit AES standard (FIPS-192) block cipher is the National Institute of Standards and Technology (NIST) replacement for the DES (Data Encryption Standard

FIPS46-2). AES has been designed to protect sensitive government information well into the 21st century. It replaces the aging DES, which NIST adopted in 1977 as a Federal Information Processing Standard used by federal agencies to protect sensitive, unclassified information. The 128-bit AES standard has $3.4x10^{38}$ possible 128-bit key variants, and it has been estimated that it would take 1,000 trillion years to crack 128-bit AES cipher text using exhaustive techniques. Keys are stored (securely) in Fusion devices in nonvolatile Flash memory. All programming files sent to the device can be authenticated by the part prior to programming to ensure that bad programming data is not loaded into the part that may possibly damage it. All programming verification is performed on-chip, ensuring that the contents of Fusion devices remain secure.

AES decryption can also be used on the 1,024-bit FlashROM to allow for secure remote updates of the FlashROM contents. This allows for easy, secure support for subscription model products.

AES for Flash Memory

AES decryption can also be used on the Flash memory blocks. This allows for the secure update of the Flash memory blocks. During runtime, the encrypted data can be clocked in via the JTAG interface. The data can be passed through the internal AES decryption engine, the decrypted data can then be stored in the Flash memory block.

Programming

Programming can be performed using various programming tools, such as Silicon Sculptor II (BP Micro Systems) or FlashPro3 (Actel).

The user can generate *.stp programming files from the Designer software and can use these files to program a device.

Fusion devices can be programmed in system.

ISP

Fusion devices support IEEE 1532 ISP via JTAG and require a single V_{PUMP} voltage of 3.3 V during programming. In addition, programming via a Microcontroller (MCU) in a target system can be achieved.

JTAG IEEE 1532

Programming with IEEE 1532

Fusion devices support the JTAG-based IEEE1532 standard for ISP. As part of this support, when a Fusion device is in an unprogrammed state, all user I/O pins are disabled. This is achieved by keeping the global IO_EN signal deactivated, which also has the effect of disabling the input buffers. Consequently, the SAMPLE instruction will have no effect while the Fusion device is in this unprogrammed state—different behavior from that of the ProASIC^{PLUS}® device family. This is done because SAMPLE is defined in the IEEE1532 specification as a noninvasive instruction. If the input buffers were to be enabled by SAMPLE temporarily turning on the I/Os, then it would not truly be a noninvasive instruction.

Boundary Scan

Fusion devices are compatible with IEEE Standard 1149.1, which defines a hardware architecture and the set of mechanisms for boundary scan testing. The basic Fusion boundary scan logic circuit is composed of the test access port (TAP) controller, test data registers, and instruction register (Figure 2-122 on page 2-171). This circuit supports all mandatory IEEE 1149.1 instructions (EXTEST, SAMPLE/PRELOAD, and BYPASS) and the optional IDCODE instruction (Table 2-150 on page 2-171).

Each test section is accessed through the TAP, which has five associated pins: TCK (test clock input), TDI, TDO (test data input and output), TMS (test mode selector), and TRST (test reset input). TMS, TDI, and TRST are equipped with pull-up resistors to ensure proper operation when no input data is supplied to them. These pins are dedicated for boundary scan test usage. Refer to the "JTAG Pins" section on page 2-167 for pull-up/down recommendations for TDO and TCK pins. The TAP controller is a 4-bit state machine (16 states) that operates as shown in Figure 2-122 on page 2-171. The 1s and 0s represent the values that must be present at TMS at a rising edge of TCK for the given state transition to occur. IR and DR indicate that the instruction register or the data register is operating in that state.

Table 2-149 • **TRST and TCK Pull-Down Recommendations**

V_{JTAG}	Tie-off Resistance*
V_{JTAG} at 3.3 V	200 Ω to 1 kΩ
V_{JTAG} at 2.5 V	200 Ω to 1 kΩ
V_{JTAG} at 1.8 V	500 Ω to 1 kΩ
V_{JTAG} at 1.5 V	500 Ω to 1 kΩ

Note: **Equivalent parallel resistance if more than one device is on JTAG chain.*

The TAP controller receives two control inputs (TMS and TCK) and generates control and clock signals for the rest of the test logic architecture. On power-up, the TAP controller enters the Test-Logic-Reset state. To guarantee a reset of the controller from any of the possible states, TMS must remain high for five TCK cycles. The TRST pin may also be used to asynchronously place the TAP controller in the Test-Logic-Reset state.

Fusion devices support three types of test data registers: bypass, device identification, and boundary scan. The bypass register is selected when no other register needs to be accessed in a device. This speeds up test data transfer to other devices in a test data path. The 32-bit

device identification register is a shift register with four fields (LSB, ID number, part number, and version). The boundary scan register observes and controls the state of each I/O pin. Each I/O cell has three boundary scan register cells, each with a serial-in, serial-out, parallel-in, and parallel-out pin.

The serial pins are used to serially connect all the boundary scan register cells in a device into a boundary scan register chain, which starts at the TDI pin and ends at the TDO pin. The parallel ports are connected to the internal core logic I/O tile and the input, output, and control ports of an I/O buffer to capture and load data into the register to control or observe the logic state of each I/O.

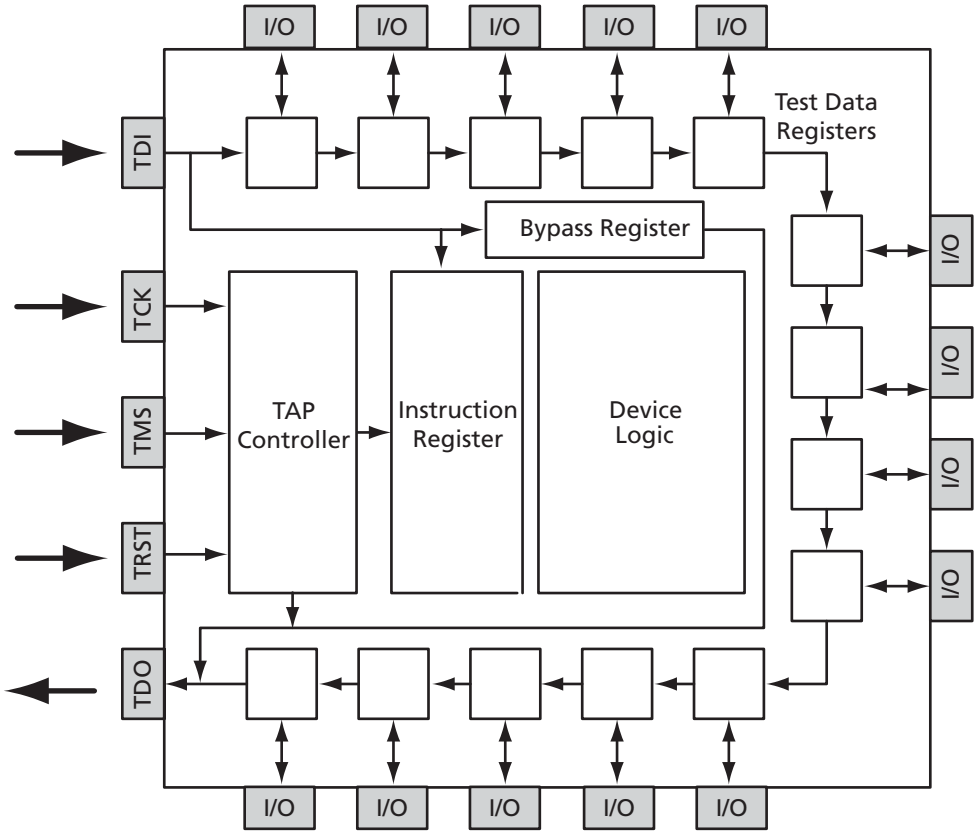


Figure 2-122 • **Boundary Scan Chain in Fusion**

Table 2-150 • **Boundary Scan Opcodes**

	Hex Opcode
EXTEST	00
HIGHZ	07
USERCODE	0E
SAMPLE/PRELOAD	01
IDCODE	0F
CLAMP	05
BYPASS	FF

IEEE 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected, refer to the I/O Timing characteristics for more details.

Table 2-151 • **JTAG 1532**
Commercial Case Conditions: T_J = 70°C, V_{CC} = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{DISU}	Test Data Input Setup Time				ns
t_{DIHD}	Test Data Input Hold Time				ns
t_{TMSSU}	Test Mode Select Setup Time				ns
t_{TMDHD}	Test Mode Select Hold Time				ns
t_{TCK2Q}	Clock to Q (Data Out)				ns
t_{RSTB2Q}	Reset to Q (Data Out)				ns
F_{TCKMAX}	TCK maximum frequency	20	20	20	MHz
$t_{TRSTREM}$	ResetB Removal time				ns
$t_{TRSTREC}$	ResetB Recovery time				ns
$t_{TRSTMPW}$	ResetB minimum pulse				ns

Note: *For the derating values at specific junction-temperature and voltage-supply levels, refer to Table 3-6 on page 3-6.*