Real-Time Clock in Actel Fusion™ FPGAs

Introduction

Real-time clocks are used in a wide variety of applications. For example, a real-time clock can be used to timestamp particular transactions done by ATM machines or vending machines, such as data transfers. Real-time clocks can also be used to record the active run/on time for appliances, industrial machinery, and similar devices.

Common requirements for real-time clocks include the following capabilities:

- Presetting the real-time clock at any time
- Tracking the time when the application is in sleep mode

The Actel Fusion FPGAs provide the means to easily implement a real-time clock within the FPGA with both of the above-mentioned capabilities. The analog block of Fusion FPGAs contains a real-time counter (RTC) that runs off the analog 3.3 V supply. The RTC block in Fusion devices contains a 40-bit counter along with a 40-bit match register and a control register that oversees the functionality of the counter. Figure 1 illustrates an example of implementation of the match for real-time clock. The clock to the counter is provided by an external crystal. The crystal clock is pre-scaled (divided by 128) internally before entering the counter. As a result, if the crystal clock is chosen to be 32.768 kHz, bit 7 of the counter will toggle at a rate of 1 Hz (1 second) and the whole counter equates to just over 136 years of elapsed timekeeping.

The RTC of Fusion FPGAs provides the following capabilities:

- FPGA fabric can read from and write to the 40-bit count register of RTC.
- FPGA fabric can read from and write to the 40-bit match register.
- The overall match output or individual match bits are available to the FPGA fabric.
- FPGA fabric can read from and write to the RTC control register. This enables the user to perform count enable/disable or counter reset dynamically during normal operation.

These characteristics and capabilities of the Fusion RTC make this block an ideal choice for applications using a real-time clock. By using the RTC block of Fusion devices, the real-time clock application can be integrated into the FPGA, reducing the cost/size of the application hardware.

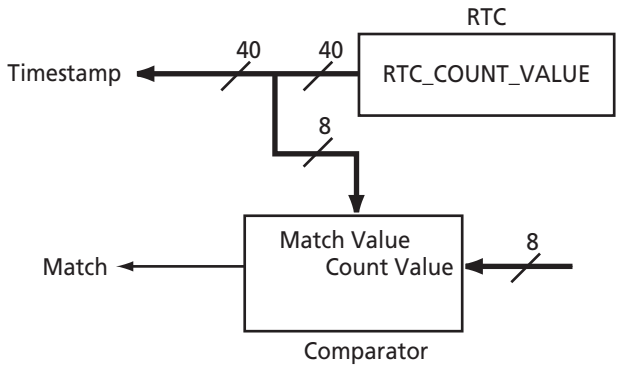

Figure 1 • **Generating Match Signal from RTC Register Content**

Implementation

If the crystal oscillator, driving the RTC block of Fusion FPGAs, is set to 32.768 kHz, bit 7 of the RTC block will toggle at the rate of 1 Hz. The contents of the first byte of the RTC count register can be accessed using the SmartGen IP. Bit 7 of the RTC creates a 1 Hz periodic signal for the FPGA fabric. This signal can drive specific counters, implemented in the FPGA fabric by users, in which the seconds, minutes, hours, days, months, or years reside.

Real-Time Clock Preset

The register inside the FPGA fabric holding the real-time clock value can be preset (written) to a user-defined value at any time. Furthermore, the RTC count register can be preset to a user-defined value if needed, using SmartGen IP. Real-time clock implementations in which only bit 7 of the RTC is used to create 1 Hz pulses to the FPGA fabric do not need to write into the RTC. In such applications, presetting the clock only requires writing into the FPGA fabric registers in which the time is stored.

Real-Time Clock in Sleep Mode

In many low power applications, the FPGA fabric enters and exits sleep mode by powering down the 1.5 V supply to the FPGA fabric. The RTC block is powered by the external 3.3 V supply, and therefore it keeps counting during sleep mode. Consequently, the content of the RTC provides information of the elapsed time in sleep mode.

If a user application requires the real-time clock to be automatically updated after exiting sleep mode, the current real-time should be stored in the embedded Flash memory before entering sleep mode. When the 1.5 V supply to the FPGA fabric is powered up again, the last content of the real-time clock registers is retrieved from the embedded Flash memory and adjusted based on the elapsed time extracted from RTC. Then the updated time can be preset into the FPGA fabric registers and the real-time clock continues to operate as normal based on the 1 Hz pulses coming from RTC.

Figure 2 illustrates block diagram implementation of a complete real-time clock system with sleep mode and preset features.

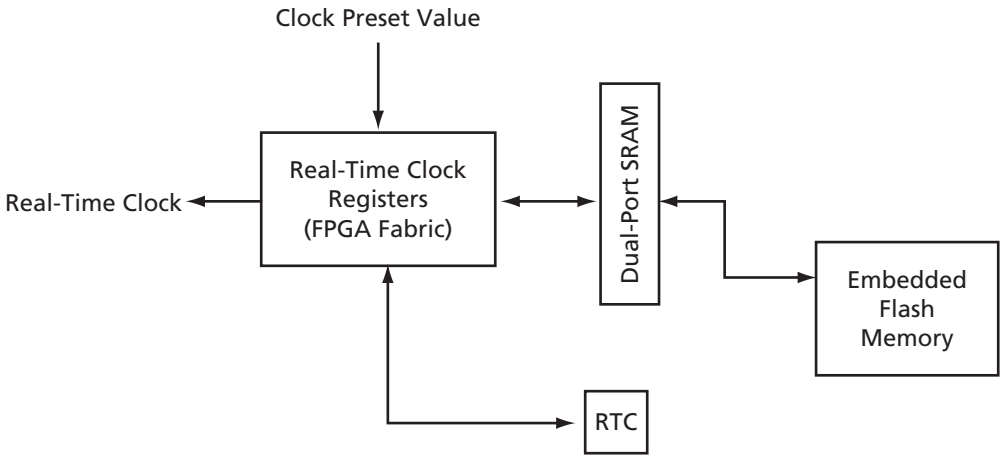

Figure 2 • **Block Diagram of Real-Time Clock System Implementation**

Conclusion

The Actel Fusion FPGAs contain a real time counter, which can be simply converted to a real-time clock. The counter is powered by a 3.3 V supply and therefore operates independently from the FPGA fabric power supply. This separation allows the RTC to control the power supply to the FPGA core, enabling a robust sleep mode capability. The RTC block in Fusion FPGAs allows designers to integrate a complete real-time clock application with the desired set of features into the FPGA.

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