Using Fusion FIFO for Generating Periodic Waveforms

The Actel Fusion™ family of Programmable System Chips (PSC) contains a robust collection of embedded memories including Flash memory, FlashROM, and RAM/FIFO blocks. The RAM/FIFO memory blocks include a dedicated FIFO controller to generate internal addresses and external flag logic (FULL, EMPTY, AFULL, AEMPTY).

In addition to the conventional flags, data, and address ports, Fusion FIFO blocks include two input pins: FSTOP and ESTOP. FSTOP is an active high signal used to stop the FIFO write-address counter when the FIFO is full (FULL flag is high). Similarly, the active high ESTOP signal stops the FIFO read counter from counting once the FIFO is empty (i.e., EMPTY flag goes high). When ESTOP is low, the read counter will roll over to the top (i.e. address '0') and start counting. If the ESTOP input is low, when the FIFO counter hits the bottom of the FIFO, the EMPTY flag becomes active for only one clock cycle. On the next cycle, when the read counter rolls over to the top, the flag is cleared.

Fusion devices support between 256 kbytes and 1 Mbyte embedded Flash memory. Fusion embedded Flash memory combines fast access times (60 ns random access and 10 ns access in Read-Ahead mode) with a configurable 8-, 16-, or 32-bit data path, enabling high-speed operation without wait states. Each page has 128 bytes; 32 pages comprise one sector.

By combining the FIFO blocks and Flash memory blocks, a periodic pattern/waveform can be generated. This is done by using the ESTOP to write into the FIFO once from the Flash block, then the contents can be read repeatedly.

FIFO Initialization

As mentioned earlier, the FIFO blocks need be written once (initialized) with the data before the periodic reading starts. The initialization data can be provided to the FIFO by internal logic, embedded Flash memory or external storage devices however, it recommended to use the embedded Flash memory. Refer to the Fusion Mixed Signal FPGA datasheet for more information on embedded Flash memory. The Sine Table on the Actel website is used to generate half-cycle of sine wave. This Sine Table requires 1024x8 memory.

Creating a FIFO Block

The FIFO macro, FIFO4K18, can be instantiated directly from the Fusion macro library. After instantiation of the macro, designers must bind all the ports of the FIFO4K18 macro to the rest of the design or terminate them to appropriate logic based on the desired configuration and/or functionality of the FIFO block. This approach can be tedious and prone to errors. Actel recommends that designers use SmartGen core generator, integrated in the Actel Libero® Integrated Design Environment (IDE) software, to create FIFO blocks. SmartGen instantiates the FIFO macro from the library and connects all the ports appropriately based on user's entry. Refer to the *Fusion, ProASIC3E, and ProASIC3 Macro Library Guide* for more information.

To create a FIFO with disabled ESTOP, users should check the **Continue counting Read Counter after FIFO is empty option** as shown in Figure 1 on page 2.

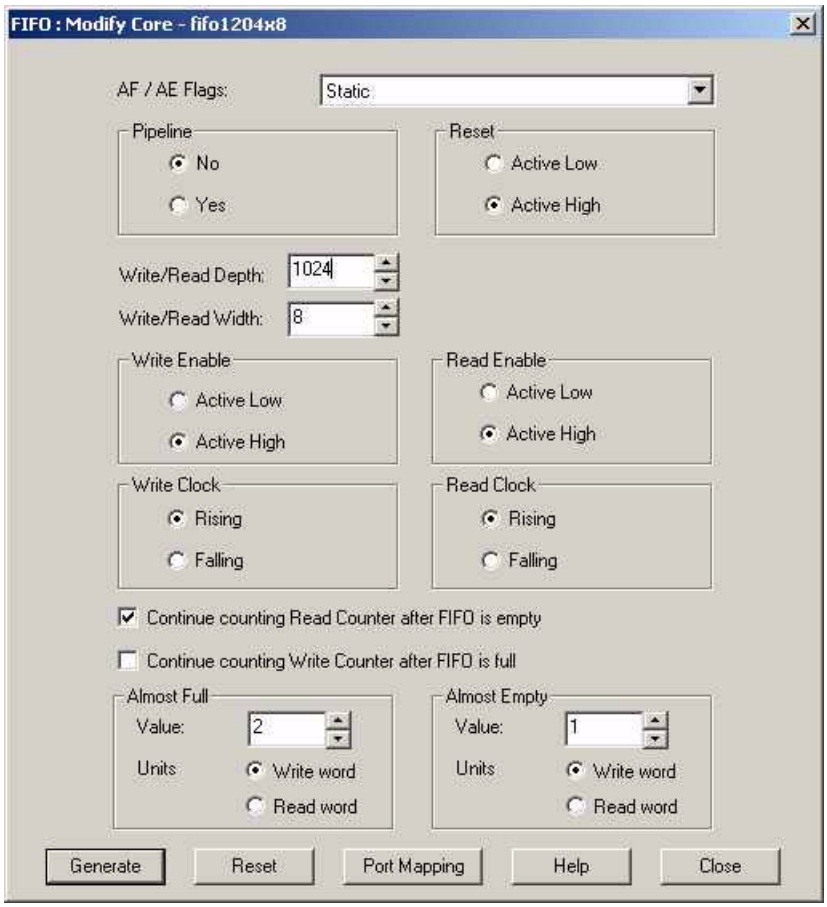

Figure 1 • **SmartGen GUI During Fusion FIFO Generation**

Waveform Generator Design

Two essential building blocks of a complete waveform generator design are the initialization block and FIFO. As mentioned in the "FIFO Initialization" section on page 1, there are various solutions to initialize the FIFO block. Figure 2 illustrates the block diagram for a waveform generator design using Embedded Flash memory to initialize Fusion FIFO. The initialization block includes the Embedded Flash memory, where the half cycle of the Sine Table content is stored.

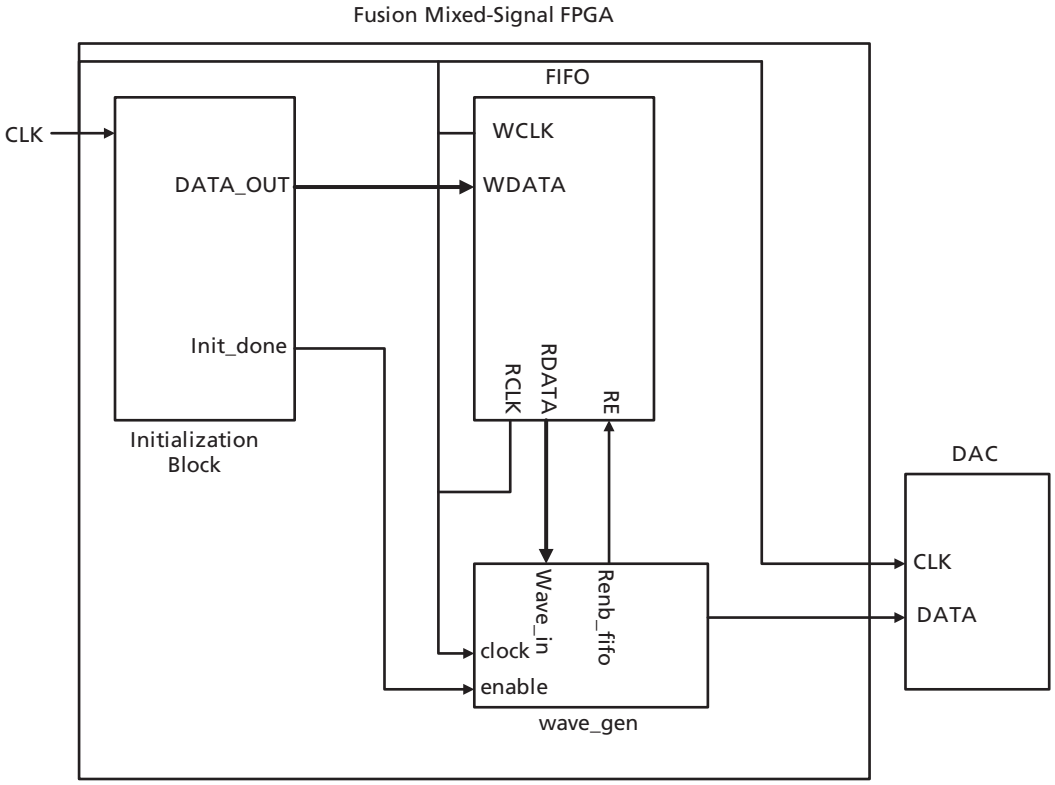

Figure 2 • **Block Diagram of the Waveform Generator**

The Wave_Gen block shown in Figure 2 on page 3 reads the waveform data points and sends it out of the FPGA to be converted into an analog waveform. The structure and functionality of Wave_Gen block depends entirely to the waveform type (sine wave, square wave, etc.) and the format of the data stored in the FIFO (two data points per row, half or full cycle, etc.). The Sine Table on the Actel website contains the initialization data for half of a cycle of a sine wave. If this table is used to initialize FIFO blocks, the contents of the FIFO should be read twice to generate a full cycle of periodic sine wave. The following is an example of the Wave_Gen block in VHDL that uses the half-cycle data, which is stored in the FIFO, and transmits a full sine wave data to the external D/A. The Wave_Gen design in this example, enabled at the end of initialization, reads through the FIFO block (half-cycle sine wave) and changes the sign (+/-) of the read data alternatively at the end of each half-cycle to generate a full-cycle sine wave.

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity wave_gen is
   port( clock, reset_n, enable, empty: in std_logic;
         wave_in : in  std_logic_vector(7 downto 0);
         renb_fifo : out std_logic;
         wave_out: out std_logic_vector( 8 downto 0 ));
end;

architecture behave of wave_gen is
   type state_type is ( pos_cycle, neg_cycle);
   signal current_state, next_state: state_type;
   signal current_sign, next_sign: std_logic;
begin

   process( clock, reset_n )
   begin
      if reset_n = '0' then
         current_state <= pos_cycle;
         current_sign <= '0';
      elsif rising_edge( clock ) then
         if enable = '1' then
         if (empty = '1') then
            current_state <= next_state;
            current_sign <= next_sign;
            end if;
         end if;
      end if;
   end process;

process(current_state)
```

```
begin
   case current_state is
      when pos_cycle =>
         next_state <= neg_cycle;
         next_sign <= '1';
            when neg_cycle =>
         next_state <= pos_cycle;
         next_sign <= '0';
            when others =>
         next_state <= pos_cycle;
         next_sign <= '0';
   end case;
end process;

process(clock, reset_n)
begin
   if (reset_n = '0') then
      wave_out <= (others => '0');
   elsif rising_edge( clock ) then
      wave_out <= current_sign & wave_in;
   end if;
end process;

process (enable, reset_n)
begin
if (reset_n = '0' or enable = '0') then
   renb_fifo <= '0';
else
   renb_fifo <= '1';
end if;
end process;

end;
```

Related Documents

Application Notes

Fusion FlashROM (FROM)
www.actel.com/documents/Fusion_FROM_AN.pdf

User's Guides

Fusion, ProASIC3E, and ProASIC3 Macro Library Guide
www.actel.com/documents/pa3_libguide_ug.pdf

http://www.actel.com

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