ProASIC3®E Flash Family FPGAs

with Optional Soft ARM® Support

FlashLock

Features and Benefits

High Capacity

- 600 k to 3 Million System Gates
- 108 k to 504 kbits of True Dual-Port SRAM
- Up to 616 User I/Os

Reprogrammable Flash Technology

- 130-nm, 7-Layer Metal (6 Copper), Flash-Based CMOS Process
- Live At Power-Up (LAPU) Level 0 Support
- Single-Chip Solution
- Retains Programmed Design When Powered Off

On-Chip User Nonvolatile Memory

- 1 kbit of FlashROM with Synchronous Interfacing

High Performance

- 350 MHz System Performance
- 3.3 V, 66 MHz 64-Bit PCI

In-System Programming (ISP) and Security

- Secure ISP Using On-Chip 128-Bit Advanced Encryption Standard (AES) Decryption via JTAG (IEEE1532-compliant)
- FlashLock® to Secure FPGA Contents

Low Power

- 1.5 V Core Voltage for Low Power
- Support for 1.5-V-Only Systems
- Low-Impedance Flash Switches

High-Performance Routing Hierarchy

- Segmented, Hierarchical Routing and Clock Structure
- Ultra-Fast Local and Long-Line Network
- Enhanced High-Speed, Very-Long-Line Network
- High-Performance, Low-Skew Global Network
- Architecture Supports Ultra-High Utilization

Pro (Professional) I/O

- 700 Mbps DDR, LVDS-Capable I/Os
- 1.5 V, 1.8 V, 2.5 V, and 3.3 V Mixed-Voltage Operation
- Bank-Selectable I/O Voltages – Up to 8 Banks per Chip
- Single-Ended I/O Standards: LVTTL, LVCMOS 3.3 V/ 2.5 V/1.8 V/1.5 V, 3.3 V PCI/ 3.3 V PCI-X, and LVCMOS 2.5 V/5.0 V Input
- Differential I/O Standards: LVPECL, LVDS, BLVDS, and M-LVDS
- Voltage-Referenced I/O Standards: GTL+ 2.5 V/3.3 V, GTL 2.5 V/3.3 V, HSTL Class I and II, SSTL2 Class I and II, SSTL3 Class I and II
- I/O Registers on Input, Output, and Enable Paths
- Hot-Swappable and Cold Sparing I/Os
- Programmable Output Slew Rate and Drive Strength
- Programmable Input Delay
- Schmitt-Trigger Option on Single-Ended Inputs
- Weak Pull-Up/Down
- IEEE1149.1 (JTAG) Boundary Scan Test
- Pin-Compatible Packages Across the ProASIC3E Family

Clock Conditioning Circuit (CCC) and PLL

- Six CCC Blocks, Each with an Integrated PLL
- Flexible Phase-Shift, Multiply/Divide, and Delay Capabilities
- Wide Input Frequency Range (1.5 MHz to 350 MHz)

SRAMs and FIFOs

- Variable-Aspect Ratio 4,608-Bit RAM Blocks (x1, x2, x4, x9, x18 Organizations Available)
- True Dual-Port SRAM (except x18)
- 24 SRAM and FIFO Configurations with Synchronous Operation up to 350 MHz

Soft ARM7™ Core Support in M7 ProASIC3E Devices

- CoreMP7Sd (with debug) and CoreMP7S (without debug)

Table 1 • **ProASIC3E Product Family**

ProASIC3E Devices	**A3PE600**	**A3PE1500**	**A3PE3000**
ARM-Enabled ProASIC3E Devices[1]	**M7A3PE600**	**M7A3PE1500**	**M7A3PE3000**
System Gates	600 k	1.5 M	3 M
VersaTiles (D-Flip-Flops)	13,824	38,400	75,264
RAM kbits (1,024 bits)	108	270	504
4,608 Bit Blocks	24	60	112
FlashROM Bits	1 k	1 k	1 k
Secure (AES) ISP	Yes	Yes	Yes
CCCs with Integrated PLLs[2]	6	6	6
VersaNet Globals[3]	18	18	18
I/O Banks	8	8	8
Maximum User I/Os	270	439	616
Package Pins PQFP FBGA	 PQ208 FG256, FG484	 PQ208 FG484, FG676	 PQ208 FG484, FG896

Notes:

1. *Refer to the CoreMP7 datasheet for more information.*
2. *The PQ208 package has six CCCs and two PLLs.*
3. *Six chip (main) and three quadrant global networks are available.*
4. *For devices supporting lower densities, refer to the ProASIC3 Flash FPGAs datasheet.*

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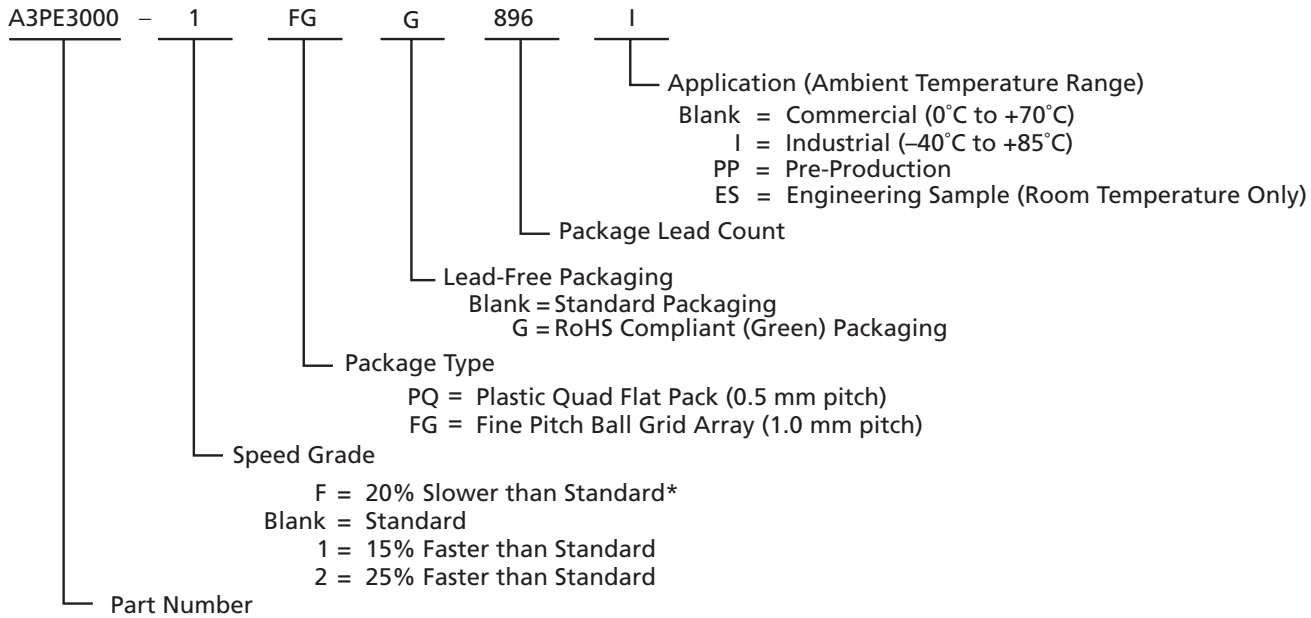
I/Os Per Package[1]

ProASIC3E Devices	A3PE600		A3PE1500 [3]		A3PE3000 [3]	
ARM-Enabled ProASIC3E Devices	M7A3PE600		M7A3PE1500		M7A3PE3000	
	I/O Types					
Package	Single-Ended I/O[1]	Differential I/O Pairs	Single-Ended I/O[1]	Differential I/O Pairs	Single-Ended I/O[1]	Differential I/O Pairs
PQ208	147	65	147	65	147	65
FG256	165	79	–	–	–	–
FG484	270	135	280	136	280	136
FG676	–	–	439	209	–	–
FG896	–	–	–	–	616	300

Notes:

1. *When considering migrating your design to lower or higher density devices, refer to the "Package Pin Assignments" section on page 4-1 to ensure complying with design and board migration requirements.*
2. *Each used differential I/O pair reduces the number of single-ended I/Os available by two.*
3. *For A3PE1500 and A3PE3000 devices, the usage of certain I/O standards is limited:*
   – SSTL3(I) and (II): up to 40 I/Os per north or south bank
   – LVPECL / GTL+ 3.3 V / GTL 3.3 V: up to 48 I/Os per north or south bank
   – SSTL2(I) and (II) / GTL+ 2.5 V/ GTL 2.5 V: up to 72 I/Os per north or south bank
4. *FG256 and FG484 are footprint-compatible packages.*
5. *When using voltage-referenced I/O standards, one I/O pin should be assigned as a voltage-referenced pin (V_{REF}) per minibank (group of I/Os). Refer to the "I/O Banks and I/O Standards Compatibility" section on page 2-28 for more information about V_{REF} and the use of minibanks.*

ProASIC3E Ordering Information



ProASIC3E Devices

A3PE600 = 600,000 System Gates
A3PE1500 = 1,500,000 System Gates
A3PE3000 = 3,000,000 System Gates

ARM-Enabled ProASIC3E Devices

M7A3PE600 = 600,000 System Gates
M7A3PE1500 = 1,500,000 System Gates
M7A3PE3000 = 3,000,000 System Gates

Note: **–F Speed Grade – DC and switching based only on simulation. The characteristics are subject to change after establishing FPGA specifications. Some restrictions might be added and will be reflected in future revisions of this document. This speed grade is only supported in commercial temperature range.*

Temperature Grade Offerings

Package	A3PE600 M7A3PE600	A3PE1500 M7A3PE1500	A3PE3000 M7A3PE3000
PQ208	C, I	C, I	C, I
FG256	C, I	–	–
FG484	C, I	C, I	C, I
FG676	–	C, I	–
FG896	–	–	C, I

Note: *C = Commercial Temperature Range: 0°C to 70°C Ambient*
I = Industrial Temperature Range: –40°C to 85°C Ambient

Speed Grade and Temperature Grade Matrix

Temperature Grade	–F [1]	Std.	–1	–2
C[2]	✓	✓	✓	✓
I[3]	–	✓	✓	✓

Notes:

1. *DC and switching characteristics for –F speed grade targets based only on simulation. The characteristics provided for –F speed grade are subject to change after establishing FPGA specifications. Some restrictions might be added and will be reflected in future revisions of this document. The –F speed grade is only supported in commercial temperature range.*
2. *C = Commercial Temperature Range: 0°C to 70°C Ambient*
3. *I = Industrial Temperature Range: –40°C to 85°C Ambient*

Datasheet references made to ProASIC3E devices also apply to ARM-enabled ProASIC3E devices. The part numbers start with M7.

Contact your local Actel representative for device availability (http://www.actel.com/contact/offices/index.html).

Table of Contents

Introduction and Overview

General Description

ProASIC3E, the third-generation family of Actel Flash FPGAs, offers performance, density, and features beyond those of the ProASIC[PLUS]® family. The nonvolatile Flash technology gives ProASIC3E devices the advantage of being a secure, low-power, single-chip solution that is live at power-up. ProASIC3E is reprogrammable and offers time-to-market benefits at an ASIC-level unit cost. These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

ProASIC3E devices offer 1 kbit of on-chip, programmable, nonvolatile FlashROM memory storage as well as clock conditioning circuitry based on six integrated phase-locked loops (PLLs). ProASIC3E devices have up to 3 million system gates, supported with up to 504 kbits of true dual-port SRAM and up to 616 user I/Os.

All ProASIC3E devices support the ARM7 soft IP core, and the ARM-enabled devices have Actel ordering numbers that begin with M7A3PE.

Flash Advantages

Reduced Cost of Ownership

Advantages to the designer extend beyond low-unit cost, performance, and ease of use. Unlike SRAM-based FPGAs, the Flash-based ProASIC3E devices allow for all functionality to be live at power-up; no external boot PROM is required. On-board security mechanisms prevent access to all the programming information and enable secure remote updates of the FPGA logic. Designers can perform secure remote in-system reprogramming to support future design iterations and field upgrades with confidence that valuable intellectual property (IP) cannot be compromised or copied. Secure ISP can be performed using the industry-standard AES algorithm. The ProASIC3E family device architecture mitigates the need for ASIC migration at higher user volumes. This makes the ProASIC3E family a cost-effective ASIC replacement solution, especially for applications in the consumer, networking/communications, computing, and avionics markets.

Security

The nonvolatile, Flash-based ProASIC3E devices require no boot PROM, so there is no vulnerable external bitstream that can be easily copied. ProASIC3E devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile, Flash programming can offer.

ProASIC3E devices utilize a 128-bit Flash-based lock and a separate AES key to secure programmed intellectual property and configuration data. In addition, all FlashROM data in the ProASIC3E devices can be encrypted prior to loading, using the industry-leading AES-128 (FIPS192) bit block cipher encryption standard. The AES standard was adopted by the National Institute of Standards and Technology (NIST) in 2000, and replaces the 1977 DES standard. ProASIC3E devices have a built-in AES decryption engine and a Flash-based AES key that make them the most comprehensive programmable logic device security solution available today. ProASIC3E devices with AES-based security allow for secure, remote field updates over public networks such as the Internet, and ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves. The contents of a programmed ProASIC3E device cannot be read back, although secure design verification is possible.

Security, built into the FPGA fabric, is an inherent component of the ProASIC3E family. The Flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. ProASIC3E, with FlashLock and AES security, is unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected and secure, making remote ISP possible. A ProASIC3E device provides the most impenetrable security for programmable logic designs.

Single Chip

Flash-based FPGAs store the configuration information in on-chip Flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, Flash-based ProASIC3E FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load the device configuration data. This reduces bill-of-materials costs and printed circuit board (PCB) area, and increases security and system reliability.

Live at Power-Up

The Actel Flash-based ProASIC3E devices support Level 0 of the live at power-up (LAPU) classification standard. This feature helps in system component initialization, execution of critical tasks before the processor wakes up, setup and configuration of memory blocks, clock generation, and bus activity management. The LAPU feature of Flash-based ProASIC3E devices greatly simplifies total system design and reduces total system cost, often eliminating the need for Complex Programmable Logic Devices (CPLDs) and clock generation PLLs that are used for this purpose in a system. In addition, glitches and brownouts in system power will not corrupt the ProASIC3E device's Flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based ProASIC3E devices simplify total system design, and reduce cost and design risk, while increasing system reliability and improving system initialization time.

Refer to the "I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)" section on page 3-3.

Firm Errors

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. These errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not exist in the configuration memory of ProASIC3E Flash-based FPGAs. Once it is programmed, the Flash cell configuration element of ProASIC3E FPGAs cannot be altered by high-energy neutrons and is therefore immune to them. Recoverable (or soft) errors occur in the user data SRAM of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Low Power

Flash-based ProASIC3E devices exhibit power characteristics similar to an ASIC, making them an ideal choice for power-sensitive applications. ProASIC3E devices have only a very limited power-on current surge, and no high-current transition period, both of which occur on many FPGAs.

ProASIC3E devices also have low dynamic power consumption to further maximize power savings.

Advanced Flash Technology

The ProASIC3E family offers many benefits, including nonvolatility and reprogrammability through an advanced Flash-based, 130-nm LVCMOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant Flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

Advanced Architecture

The proprietary ProASIC3E architecture provides granularity comparable to standard-cell ASICs. The ProASIC3E device consists of five distinct and programmable architectural features (Figure 1-1 on page 1-3):

- FPGA VersaTiles
- Dedicated FlashROM memory
- Dedicated SRAM/FIFO memory
- Extensive clock conditioning circuitry (CCC) and PLLs
- Pro I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function or as a D-flip-flop (with or without enable), or as a latch by programming the appropriate Flash switch interconnections. The versatility of the ProASIC3E core tile as either a three-input look-up-table (LUT) equivalent or as a D-flip-flop/latch with enable allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the Actel ProASIC families of Flash-based FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

In addition, extensive on-chip programming circuitry allows for rapid, single-voltage (3.3 V) programming of the ProASIC3E devices via an IEEE 1532 JTAG interface.

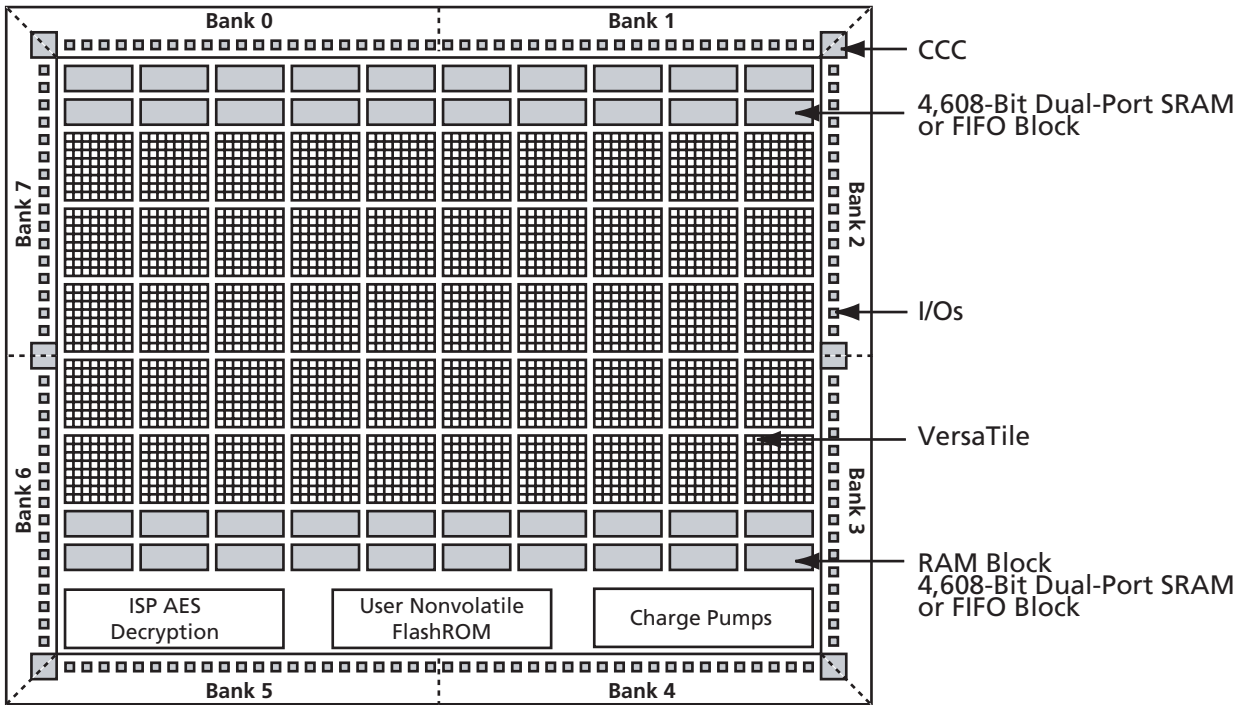


Figure 1-1 • **Device Architecture Overview**

VersaTiles

The ProASIC3E core consists of VersaTiles, which have been enhanced from the ProASIC[PLUS] core tiles. The ProASIC3E VersaTile supports the following:

- All three-input logic functions – LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set

Refer to Figure 1-2 for VersaTile configurations.

For more information about VersaTiles, refer to the "VersaTile" section on page 2-2.

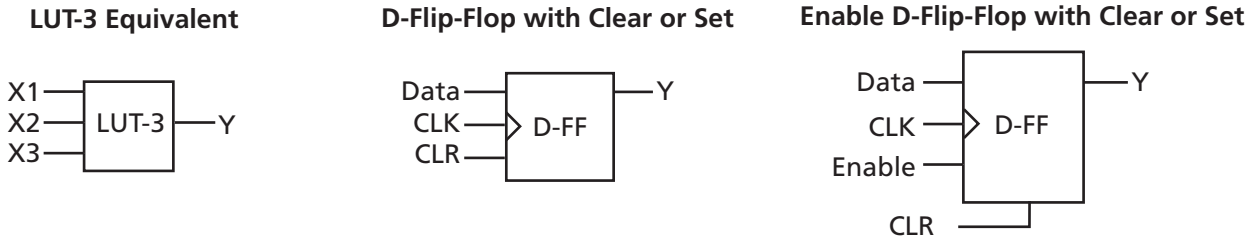


Figure 1-2 • **VersaTile Configurations**

User Nonvolatile FlashROM

Actel ProASIC3E devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard ProASIC3E IEEE 1532 JTAG programming interface. The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to securely load data over public networks, such as security keys stored in the FlashROM for a user design.

The FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can ONLY be programmed from the JTAG interface, and cannot be programmed from the internal logic array.

The FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

The Actel ProASIC3E development software solutions, Libero® Integrated Design Environment (IDE) and Designer v6.1 or later, have extensive support for the FlashROM memory. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. The second part allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Actel Libero IDE and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

SRAM and FIFO

ProASIC3E devices have embedded SRAM blocks along the north and south sides of the device. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256x18, 512x9, 1kx4, 2kx2, or 4kx1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode), using the UJTAG macro. For more information, refer to the application note, *UJTAG Applications in ProASIC3/E Devices*.

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost-Empty (AEMPTY) and Almost-Full (AFULL) flags in addition to the normal Empty and Full flags. The embedded FIFO control unit contains the counters necessary for the generation of the read and write address pointers. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

PLL and Clock Conditioning Circuitry (CCC)

ProASIC3E devices provide designers with very flexible clock conditioning capabilities. Each member of the ProASIC3E family contains six CCCs, each with an integrated PLL.

The six CCC blocks are located in the four corners and the centers of the east and west sides.

To maximize user I/Os, only the center east and west PLLs are available in devices using the PQ208 package. However, all six CCC blocks are still usable; the four corner CCCs allow simple clock delay operations as well as clock spine access (refer to the "Clock Conditioning Circuits" section on page 2-13 for more information).

The inputs of the six CCC blocks are accessible from the FPGA core or from one of several I/O inputs located near the CCC that have dedicated connections to the CCC block.

The CCC block has the following key features:

- Wide input frequency range (f_{IN_CCC}) = 1.5 MHz to 350 MHz
- Output frequency range (f_{OUT_CCC}) = 0.75 MHz to 350 MHz
- Clock delay adjustment via programmable and fixed delays from –7.56 ns to +11.12 ns
- Two programmable delay types; refer to Figure 2-16 on page 2-17, Table 2-4 on page 2-18, and the "Features Supported on Every I/O" section on page 2-31 for more information.
- Clock skew minimization
- Clock frequency synthesis

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°. Output phase shift depends on the output divider configuration.
- Output duty cycle = 50% ± 1.5% or better
- Low output jitter: worst case < 2.5% × clock period peak-to-peak period jitter when single global network used
- Maximum acquisition time = 150 µs
- Low power consumption of 5 mW
- Exceptional tolerance to input period jitter – allowable input jitter is up to 1.5 ns
- Four precise phases; maximum misalignment between adjacent phases of 40 ps × (350 MHz / f_{OUT_CCC})

Global Clocking

ProASIC3E devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there is a comprehensive global clock distribution network.

Each VersaTile input and output port has access to nine VersaNets: six chip (main) and three quadrant global networks (Figure 2-9 on page 2-9). The VersaNets can be driven by the CCC or directly accessed from the core via multiplexers (MUXes). The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high-fanout nets.

Pro I/Os with Advanced I/O Standards

The ProASIC3E family of FPGAs features a flexible I/O structure, supporting a range of voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V). ProASIC3E FPGAs support 19 different I/O standards, including single-ended, differential, and voltage-referenced. For more information, see Table 2-23 on page 2-49.

The I/Os are organized into banks, with eight banks per device (two per side). The configuration of these banks determines the I/O standards supported (see Table 2-14 on page 2-30 for more information). Each I/O bank is subdivided into V_{REF} minibanks, which are used by voltage-referenced I/Os. V_{REF} minibanks contain 8 to 18 I/Os. All the I/Os in a given minibank share a common V_{REF} line. Therefore, if any I/O in a given V_{REF} minibank is configured as a V_{REF} pin, the remaining I/Os in that minibank will be able to use that reference voltage.

Each I/O module contains several input, output, and enable registers (Figure 2-23 on page 2-33). These registers allow the implementation of the following:

- Single-Data-Rate applications (e.g., PCI 66 MHz, bidirectional SSTL 2 and 3, Class I and II)
- Double-Data-Rate applications (e.g., DDR LVDS, BLVDS, and M-LVDS I/O for point-to-point communications and DDR 200 MHz SRAM using bidirectional HSTL Class II – "DDR Module Specifications" section on page 3-56)

ProASIC3E banks support M-LVDS with 20 multi-drop points.

Related Documents

Application Notes

ProASIC3/E I/O Usage Guide
http://www.actel.com/documents/PA3_E_IO_AN.pdf
In-System Programming (ISP) in ProASIC3/E Using FlashPro3
http://www.actel.com/documents/PA3_E_ISP_AN.pdf
ProASIC3/E FlashROM
http://www.actel.com/documents/PA3_E_FROM_AN.pdf
ProASIC3/E Security
http://www.actel.com/documents/PA3_E_Security_AN.pdf
ProASIC3/E SRAM/FIFO Blocks
http://www.actel.com/documents/PA3_E_SRAMFIFO_AN.pdf
Programming a ProASIC3/E Using a Microprocessor
http://www.actel.com/documents/PA3_E_Microprocessor_AN.pdf
UJTAG Applications in ProASIC3/E Devices
http://www.actel.com/documents/PA3_E_UJTAG_AN.pdf
Using DDR for ProASIC3/E Devices
http://www.actel.com/documents/PA3_E_DDR_AN.pdf
Using Global Resources in Actel ProASIC3/E Devices
http://www.actel.com/documents/PA3_E_Global_AN.pdf
Power-Up/Down Behavior of ProASIC3/E Devices
http://www.actel.com/documents/ProASIC3_E_PowerUp_AN.pdf

For additional ProASIC3E application notes, go to http://www.actel.com/techdocs/appnotes/products.aspx.

User's Guides

SmartGen Cores Reference Guide
http://www.actel.com/documents/genguide_ug.pdf
Designer User's Guide
http://www.actel.com/documents/designer_ug.pdf
Fusion and ProASIC3/E Macro Library Guide
http://www.actel.com/documents/pa3_libguide_ug.pdf