ProASIC3/E Production FPGAs

Features and Advantages

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Introduction

Over the past decade, field-programmable gate arrays (FPGAs) have achieved widespread adoption across an expanding array of applications. By offering a universal silicon platform that can be quickly programmed for a specific application and reprogrammed with each iteration of a design, these highly flexible devices have quickly become an essential prototyping tool for many design teams and have frequently been used in low- to medium-volume applications.

Despite this success, however, FPGAs have yet to achieve widespread adoption in high-volume applications. When engineers are ready to migrate designs to higher volume production levels, standard-cell-based application-specific integrated circuits (ASICs) have typically offered the lowest cost alternative. ASIC technology's low unit cost, high performance, and low power consumption have proved formidable advantages in these higher volume environments. But as ASIC manufacturers have migrated to sub-quarter-micron process technologies and non-recurring expenses (NREs) have rapidly increased, those traditional cost advantages have evaporated.

Today, by leveraging the advantages of the latest semiconductor processes and using innovative architectures, FPGAs not only offer unit costs comparable to traditional ASICs, but match or exceed many of the power, security, reliability, live-at-power-up, and performance advantages historically accorded only to ASICs (Figure 1).

Fabricated with Flash technology, the Actel Flash-based ProASIC3/E devices are the first FPGAs to deliver all of these capabilities. ProASIC3/E devices offer designers a secure, high-performance, low-power, programmable, single-chip solution that is live at power-up, and available at ASIC-like price points.

What do designers look for in a "production FPGA"? The ideal silicon solution would offer the following seven basic features:

- Single-chip
- Affordable integration of multiple system functions with no NRE costs
- Live at power-up
- Intellectual property (IP) security
- Low power
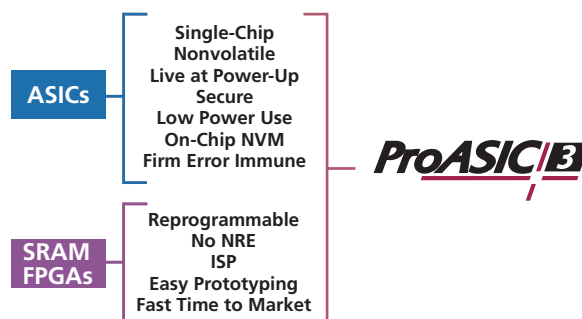- Reprogrammable and customizable
- Rapid time-to-market

Figure 1: **ProASIC3 – Best of Both ASIC and SRAM FPGA Worlds**

Cost-Optimized Architecture

To achieve the ideal silicon solution, the ProASIC3/E product line employs a proprietary architecture comprised of the following components (Figure 2):

- FPGA VersaTiles
- Dedicated FlashROM (FROM) nonvolatile memory (NVM)
- Dedicated SRAM/FIFO memory
- Extensive clock conditioning circuitry (CCC) and phase-locked loop (PLL) features
- Pro I/O structure
- FPGA VersaNet globals
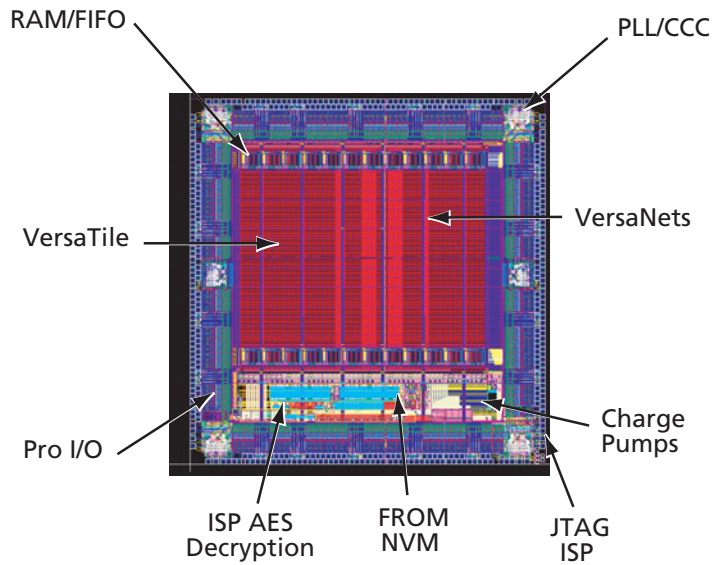- JTAG ISP/UJTAG port
- AES decryption mechanism

Figure 2: **ProASIC3/E Architecture**

Lower density devices in the product family address the "value" FPGA market segment, while the higher density parts are targeted at applications requiring a full-featured FPGA.

For the value-based FPGA market segment, the ProASIC3 devices offer extended logic density and I/Os. Most devices have support for additional I/O standards, SRAM, and a PLL. For higher end applications, the PA3 product line adds enhanced features such as high-density logic, SRAM and I/Os, advanced I/O standards, and up to six PLLs (Table 1).

Table 1: **ProASIC3 and ProASIC3E Features**

	ProASIC3 Value FPGAs	**ProASIC3E Enhanced Features**
System Gates	30 k to 1 M	600 k to 3 M
VersaTiles (D-Flip-Flop)	768 to 24,576	13,824 to 75,264
RAM kbits	Up to 144 k	108 k to 504 k
4,608-Bit Blocks	Up to 32	24 to 112
User FlashROM Bits	1 k	1 k
Secure (AES) ISP	Yes	Yes
PLLs (except A3P030)	1	6
VersaNet Globals	6 to 18	18
I/O Standards	Single-ended and differential	Single-ended, differential, and voltage-referenced
I/O Banks (+ JTAG)	Up to 4	8
I/Os Supported (single-ended)	79 to 288	147 to 616

Flash Technology

The key to these density, performance, and security improvements over traditional SRAM-based FPGAs is the use of an advanced Flash-based LVCMOS process with seven metal layers. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant Flash switches allows for industry-leading, high logic utilization without compromising device routability or performance.

The ProASIC3/E Flash-based FPGA devices are based on a Flash programming element that uses a two-transistor structure (Figure 3).
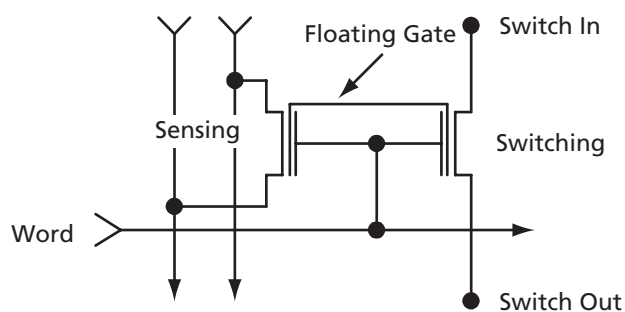
Figure 3: **ProASIC3/E Flash-Based Switch**

Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Unlike SRAM-based FPGAs that often fail to place-and-route at approximately 70% utilization, maximum core utilization is possible for virtually any design in the Flash FPGA architecture. In addition, extensive on-chip programming circuitry allows for rapid (3.3 V) single-voltage programming of the ProASIC3/E devices via an IEEE1532 JTAG interface.

This structure differs from SRAM-based FPGAs that require four to six transistors to make a single programming element. This difference carries significant advantage when comparing die area of the devices. In a given process, FPGAs based on a Flash programming element will be smaller than the SRAM FPGAs. As a result, SRAM-based FPGAs must be fabricated on a smaller, more expensive and power-hungry process technology to offer a comparable cost.

The use of Flash technology as the foundation for the ProASIC3/E devices offers a number of additional advantages over traditional SRAM-based FPGAs, including lower system cost due to fewer external components, availability of user nonvolatile memory, higher levels of security, lower power consumption, live-at-power-up capability, and firm-error immunity.

Product Features

VersaTile

The ProASIC3/E FPGA devices feature a fine-grained architecture similar to gate arrays, utilizing VersaTiles as core cells. Each VersaTile can be configured as a three-input logic function or a D-flip-flop or latch (with or without enable) by programming the appropriate Flash switch interconnections. The versatility of the ProASIC3/E core tile permits efficient use of the FPGA fabric. Unique to the Actel Flash-based FPGA families, the VersaTile capability supports a higher utilization rate than comparable SRAM FPGA cells due to the flexibility of their usage as a register or latch. The ProASIC3/E core can also handle register-intensive applications easily. In addition, since all input signals of a VersaTile can be inverted and the output can be connected to both ultra-fast local and efficient very-long line routing resources, it simplifies technology mapping and netlist optimizations.

User Nonvolatile Memory (NVM)

One of the primary distinctions between SRAM-based FPGAs and Actel ProASIC3/E FPGA technology is the addition of 1,024 bits of dedicated nonvolatile FlashROM (FROM) memory on each ProASIC3/E device. This embedded memory offers designers a unique capability as the FROM can be read, modified, and written using the IEEE1532 JTAG (or UJTAG) interface. The FROM is still secure since it can be configured to be read only from the FPGA core. The FROM is physically organized as 8x128 bit pages and logically organized as eight pages of 16 bytes. Pages can be individually programmed (erased and written) and on-chip AES decryption can be used selectively to load data (such as security keys stored in the FROM for a user's design) securely over public networks.

The FROM may be programmed via the JTAG programming interface, and its contents can be read back both through the JTAG interface or via the FPGA core. Additionally the FROM content can be programmed without erasing the FPGA core.

This unprecedented feature is an enabling technology in many applications. The FROM is well suited for a variety of system applications including Internet protocol (IP) addressing (wireless or fixed), system-calibration settings, device serialization and/or inventory control, asset management tracking, subscription-based business models (e.g., set-top boxes), secure key storage, date stamping, version management, and general-purpose Flash memory for on-the-fly updates.

Designers are able to quickly generate data for the FROM using the Actel FlashPoint tools as part of the Libero® Integrated Design Environment (IDE) and Designer software tools. These tools provide comprehensive programming file support in cases of differing FROM contents. As an example, designers may employ these tools to automatically generate sequential programming files for applications requiring a unique serial number in each part or the inclusion of static data for system version control.

SRAM and FIFO

The ProASIC3/E FPGA devices offer extensive memory resources that can be used as either RAM or FIFO. The memory blocks operate strictly in synchronous mode for both read and write operations, meeting the needs of high-performance designs. The read and write clocks are completely independent, and each may operate at any desired frequency less than or equal to 350 MHz.

The ProASIC3/E memory includes up to 504 kbits arranged as 4,608-bit embedded memory blocks. This allows many aspect ratios in the following arrangements supported by the ACTgen software tool:

- True dual-port RAM – two read, two write or one read / one write
- Two-port RAM – one read and one write
- Sync write, sync pipelined, and nonpipelined read

The ProASIC3/E memory block includes dedicated FIFO control logic to generate internal addresses and external flag logic (FULL, EMPTY, Almost-Full (AFULL), and Almost-Empty (AEMPTY)). The FIFO support includes decoder, FIFO control via the built-in flag logic, and programmability of FIFO depth and Flash threshold. The FIFO support in the ProASIC3/E devices helps minimize design effort, saves logic space for user implementation, and is useful in a variety of applications. Once the FIFO reaches an empty or full state, it can be configured to continue counting. This feature could enable the generation of a periodic waveform/pattern by writing into the FIFO once and reading the contents over and over again.

Clock Conditioning Circuitry (CCC) and PLLs

ProASIC3/E devices also provide designers with advanced and very flexible clock conditioning capabilities. Each member of the ProASIC3/E product line contains six CCCs, most with PLL blocks (Figure 4).
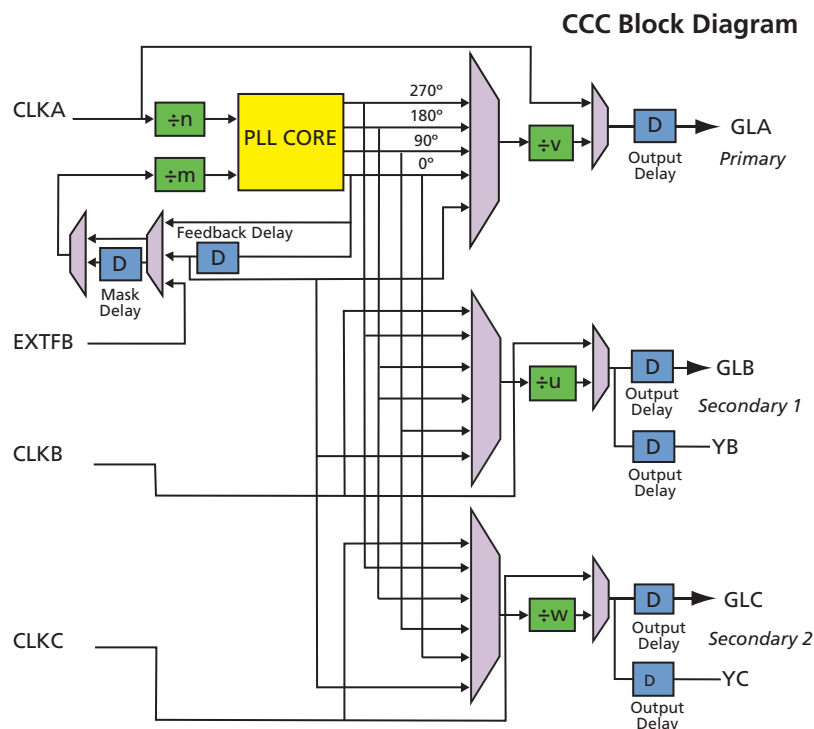
CCC Block Diagram

Figure 4: **Clock Conditioning Circuitry (Not all CCCs contain a PLL)**

The inputs of the six CCC blocks are accessible from the FPGA core or from one of several I/O inputs located by the CCC that have dedicated connections to the CCC block. The CCC block has a wide input and output frequency range, clock phase adjustment via programmable delay, clock skew minimization, and clock frequency synthesis.

The PLL inside the CCC supports an input frequency range as low as 1.5 MHz and an output (VCO) frequency range of 24 MHz to 350 MHz. It also includes output phase shift of 0°, 90°, 180°, and 270°, output duty cycle = 50% ± 1.5% or better, low output jitter, maximum acquisition time of 150 μs, low power consumption of 5 mW, exceptional tolerance to input period jitter, and four precise phases.

The CCC is able to generate clock signals (multiply/divide), adjust the delay, shift phase, and make them available to the FPGA core or I/O. In addition, the CCC can be connected to global networks (VersaNets), to be used as internal, external, or deskewed feedback in bypass mode and can be configured dynamically. Common PLL applications that can be used with ProASIC3/E FPGAs are waveform generation by clock division/multiplication, frequency synthesis, clock skew minimization, and clock delay or advance. This highly flexible clocking scheme contributes to design efficiency and higher levels of system integration.

Global Clocking

Logic functions within the device are interconnected through a four-level routing hierarchy. ProASIC3/E devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support, the architecture features a comprehensive global clock distribution network. Each VersaTile input and output port has access to 9 VersaNets (6 main, chip-wide, and 3 quadrant global networks). There are 18 VersaNets in total. The VersaNets can access all the logic, memory, and I/O tiles on the device, and can be driven by the CCC or directly accessed from the core via MUXes. The VersaNets may also be used to distribute low-skew clock signals or for rapid distribution of high-fanout nets. Furthermore, the global network branches can be separated from the chip (main) global network and used as local, low-skew global resources for internal/external clocks or high-fanout signals.

Applications that require extensive clock resources can easily route external or gated-internal clocks using VersaNet global routing networks. Designers can drastically reduce delay penalties and minimize resource usage by mapping critical, high-fanout nets to the VersaNet network.

I/O Structure

Another key difference between the ProASIC3/E FPGA family and the competition is its I/O structure. Actel devices offer higher I/O counts per number of system gates than any competitors, allowing designers to implement I/O-intensive designs quickly and easily without the penalty of moving to a higher-density device.

The ProASIC3/E I/O tile provides a flexible, programmable structure for implementing a large number of I/O standards. In addition, the registers available in the I/O tile can be used to support high-performance register inputs and outputs. The registers can also be used to support the JESD-79C Double Data Rate (DDR) standard within the I/O structure.

All of the ProASIC3/E FPGAs feature a flexible I/O structure that supports a range of voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V). The devices support up to 19 different I/O standards (single-ended, differential, and voltage-referenced). The I/Os are organized into banks, and the configuration of these banks determines the I/O standards supported. The I/Os provide programmable slew rates, drive strengths, weak pull-up and weak pull-down circuits, and many devices are capable of hot insertion and multi-voltage input and output tolerance.

With separate power and ground supplies for input and output pins, ProASIC3/E devices support efficient noise-reduced I/Os. This capability may contribute to I/O noise immunity and helps limit EMI emissions. Combined with the advanced I/O standards supported, the product line provides all the I/O capabilities required to meet the most demanding applications in the market.

The ProASIC3/E I/Os support 5 V, 3.3 V, 2.5 V, 1.8 V, and 1.5 V input tolerance for certain I/O standards. This feature simplifies communication with the FPGA device, and in the process, reduces the number of system components, saves board space, and minimizes power consumption.

UJTAG

The ProASIC3/E FPGA devices offer bidirectional access from the JTAG port to the core VersaTiles during normal operation. The UJTAG tiles are connected directly to the ProASIC3/E JTAG Test Access Port (TAP) Controller. Therefore, all functional blocks of the ProASIC3/E architecture, such as CCC and PLL, SRAM/ FIFO blocks, embedded FROM blocks, and I/O tiles, can be reached via the JTAG ports. Access to the FPGA core VersaTiles from the JTAG ports enables designers to implement many applications using the ProASIC3/E TAP Controller (JTAG port). Moreover, because the UJTAG can replace a dedicated I/O interface, this capability enhances the designer's I/O options.

Hot-Swap Support

Select ProASIC3/E devices also support hot swap operation, allowing designers to use a ProASIC3/E device in a variety of applications, such as line cards where the board specification requires hot insertion or hot removal from a powered-up system.

ProASIC3/E devices preserve data integrity on the host bus when the device power supply is not applied, and the output drive resistance of the board or card drivers is 50 Ω or less. Table 2 illustrates the various hot swap levels. ProASIC3E and A3P030 are designed to meet level 4, the highest level possible in which the system must support hot swap while maintaining the integrity of active I/O processes.

*Table 2:* **ProASIC3/E Supports Level 4 of the Hot Swap Classification**

Level	Description	Power Applied to Device?	Bus State	GND Connected to Device	Device Circuitry Connected to Bus Pins
1	Cold swap	No	–	–	–
2	Hot swap while reset	Yes	Held in reset	Must be made and maintained for 1 msec before, during, and after insertion/removal	–
3	Hot swap while bus idle	Yes	Held idle (no ongoing I/O processes during insertion/removal)	Same as Level 2	Must remain glitch-free during power-up or power-down
4	Hot swap on an active bus	Yes	Bus may have active I/O processes ongoing, but device being inserted or removed must be idle	Same as Level 2	Same as Level 3

Security

Based on Flash technology, the ProASIC3/E devices provide a high level of security from data and IP theft by cloning, reverse engineering, and overbuilding. A built-in 128-bit AES decryption core in the ProASIC3/E design facilitates secure in-system programming (ISP) of the FPGA core array fabric and the FROM. The FROM and the FPGA core fabric may be programmed independently of each other, allowing the FROM to be updated without the need for change to the FPGA core fabric. The AES master key is stored in on-chip nonvolatile memory and can be preloaded into the device in a secure programming environment. Users can then ship "blank" parts to an insecure programming or manufacturing center for final personalization with an AES encrypted bit stream.

Using this feature, designers are able to easily and securely implement late-stage product changes or customize the device by simply sending a programming file with AES encrypted data. In a similar manner, designers have the ability to perform secure remote field updates over public networks, such as the Internet or via satellite, by simply sending a configuration file with AES-encrypted data.

In contrast, designers using SRAM-based FPGAs must load the configuration file into the device each time the system powers up. Each time the system is powered up, the configuration bit stream can be intercepted and the IP exposed, thereby posing a significant security risk. In contrast to SRAM-based FPGAs, ProASIC3/E configuration files cannot be read back via JTAG or any other method. Designers have the ability to use a FlashLock Pass Key to prohibit any write or verification operations on the device and may have the ability to permanently lock a device using a mechanism that effectively creates a one-time programmable device. This procedure prohibits any future modifications to the device (Figure 5).
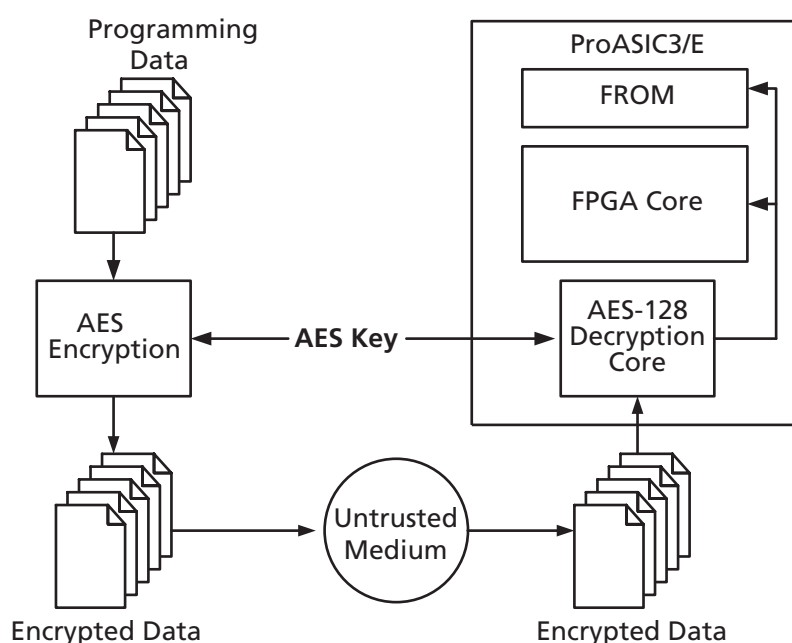
Figure 5: **Programming the ProASIC3 FPGA and/or FROM Contents with AES Encrypted Data**

As the ProASIC3/E architecture is based on Flash technology, the devices do not require a configuration bit stream once they are programmed in a secure environment. Further, Flash technology is inherently resistant to invasive attacks. Pirating strategies such as de-capping and stripping only expose the device structure and not the content of the Flash cell. Any attempt to reveal the Flash cell content will modify its value and present a major obstacle to reverse engineering attempts. In addition, there are millions of Flash cells in each ProASIC3/E device, making it extremely difficult and impractical to determine the state of each cell.

Firm-Error Immunity

ProASIC3/E Flash-based technology also offers immunity to soft and firm errors. Charged particles originating from a variety of sources, including cosmic rays and alpha particles from packaging contamination, can cause soft or firm errors in a device. Neutron or alpha-induced firm errors cause SRAM FPGA configuration corruption and require device reload or system-level reset. Errors are "firm" because they are not transient, and therefore, the error stays until detected and cleared.

SRAM-based FPGAs are vulnerable to radiation that may result in firm errors. If the I/O in an SRAM-based FPGA suffers a firm error, its output could be turned on, causing significant board damage, and its input could be turned off, resulting in critical signal loss (Figure 6 and Figure 7). By eliminating this danger, Flash-based ProASIC3/E FPGAs help designers avoid product liability issues, improve customer satisfaction, and minimize product return rates and other complications caused by firm errors.
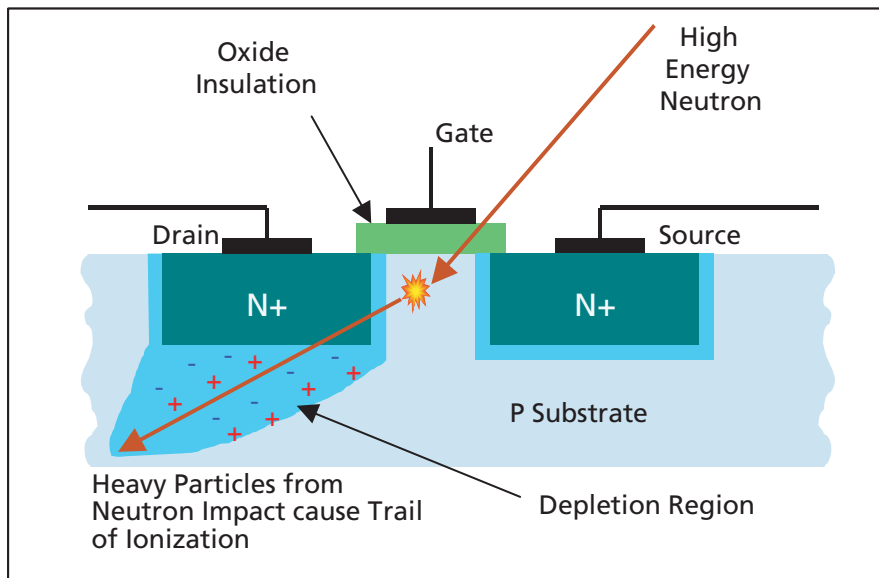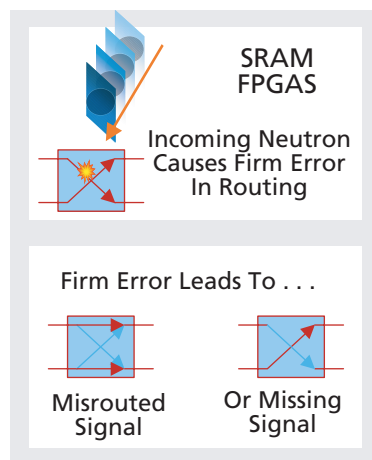

Figure 6: **Firm Errors in SRAM-Based FPGAs**

Figure 7: **Firm Errors Change the State of SRAM-Based FPGAs**

ProASIC3/E Production FPGAs

Power Management

Sophisticated power-up management circuitry is designed into every ProASIC3/E device. These circuits ensure easy transition between the powered-down state and the powered-up state of the device. The many different supplies can power-up in any sequence. In addition, the I/O will be in a known state through the power-up sequence.

There are five regions to consider during power-up, as illustrated in Figure 8 on page 14. The ProASIC3/E I/Os are activated when the following three conditions are met:

1. V_{CC} and V_{CCI} are above the minimum specified trip points
2. $V_{CCI} > V_{CC} - 0.75$ V
3. Chip is in the operating mode

The ProASIC3/E can be activated using a single 1.5 V power supply to both V_{CC} and V_{CCI} voltage pins. The I/Os are multi-voltage tolerant when used with certain I/O standards allowing the system to run on a single voltage source. This reduces cost and board space, and simplifies system design.

Unlike SRAM-based FPGAs, Flash-based ProASIC3/E devices do not require the loading of a configuration file to the FPGA. Instead, they are live at power-up and do not require additional components, thereby simplifying board and system design and reducing overall component cost.

The ProASIC3/E devices are instantly on; therefore, they may be used to implement or help in-system critical tasks upon power-up. For example, ProASIC3/E FPGAs are able to generate essential system clocking and monitor or supervise system signals.

By using the ProASIC3/E, a designer can eliminate the need for a CPLD (Complex Programmable Logic Device) on the board for MCU (microcontroller) decoding or other power-up issues. In SRAM-based FPGAs, it takes hundreds of milliseconds for the device to load the configuration file and for the logic to begin working.
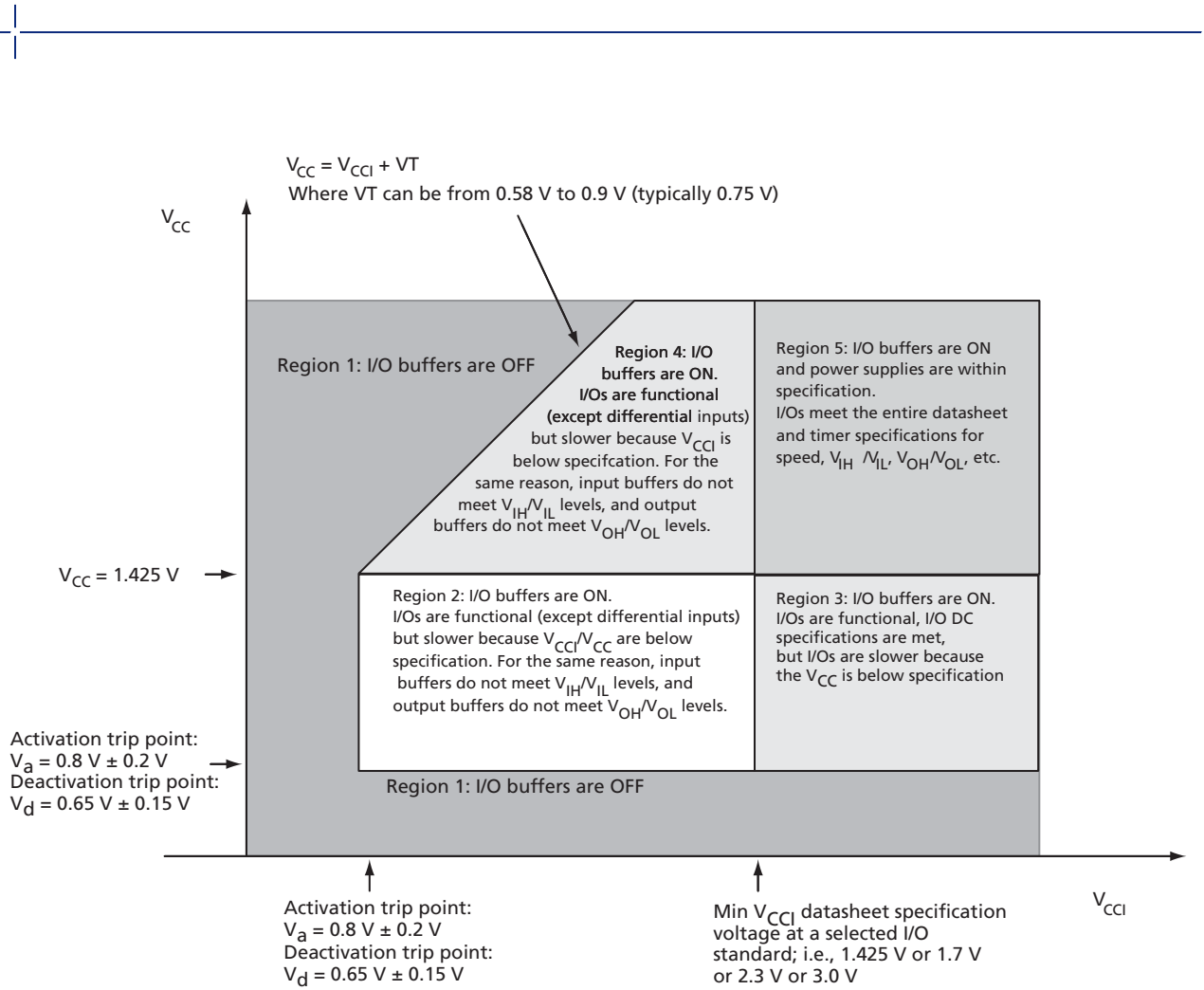
$V_{CC} = V_{CCI} + VT$
Where VT can be from 0.58 V to 0.9 V (typically 0.75 V)

V_{CC}

Region 1: I/O buffers are OFF

Region 4: I/O buffers are ON. I/Os are functional (except differential inputs) but slower because V_{CCI} is below specifcation. For the same reason, input buffers do not meet V_{IH}/V_{IL} levels, and output buffers do not meet V_{OH}/V_{OL} levels.

Region 5: I/O buffers are ON and power supplies are within specification. I/Os meet the entire datasheet and timer specifications for speed, V_{IH} /V_{IL}, V_{OH}/V_{OL}, etc.

$V_{CC} = 1.425$ V

Region 2: I/O buffers are ON. I/Os are functional (except differential inputs) but slower because V_{CCI}/V_{CC} are below specification. For the same reason, input buffers do not meet V_{IH}/V_{IL} levels, and output buffers do not meet V_{OH}/V_{OL} levels.

Region 3: I/O buffers are ON. I/Os are functional, I/O DC specifications are met, but I/Os are slower because the V_{CC} is below specification

Activation trip point:
$V_a = 0.8$ V ± 0.2 V
Deactivation trip point:
$V_d = 0.65$ V ± 0.15 V

Region 1: I/O buffers are OFF

V_{CCI}

Activation trip point:
$V_a = 0.8$ V ± 0.2 V
Deactivation trip point:
$V_d = 0.65$ V ± 0.15 V

Min V_{CCI} datasheet specification voltage at a selected I/O standard; i.e., 1.425 V or 1.7 V or 2.3 V or 3.0 V

Figure 8: **ProASIC3/E Power-Up Sequence**

ProASIC3/E Production FPGAs

Design Tools

Software

Actel offers extensive support for ProcASIC3/E in the Libero IDE and Designer FPGA development software tools to help the user implement an effective design quickly. The Actel Libero IDE is an integrated design manager that seamlessly integrates design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Additionally, the Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a comprehensive environment. The Libero IDE includes support from the following third-party EDA vendors: Magma® Design Automation, Synplicity®, Mentor Graphics®, and SynaptiCAD®.

With the Designer software, the designer can lock the design pins before layout while minimally impacting the results of place-and-route. Additionally, the Actel back-annotation flow is compatible with all major simulators so the simulation results can be cross-probed with Silicon Explorer II, the Actel integrated verification and logic analysis tool. The ACTgen macro builder, another tool included in the Designer software, easily creates popular and commonly used logic functions for implementation into a schematic or HDL design. Actel Designer software is compatible with the most popular FPGA design entry and verification tools from EDA vendors and is available for both the Windows® and UNIX operating systems.

Programming

Programming can be achieved via a microcontroller or JTAG port supporting industry standard IEEE1532 ISP. Programming requires a single V_{PUMP} voltage of 3.3 V. No additional programming circuitry is required. It is also possible to program the FROM user nonvolatile memory via the JTAG interface in system.

ISP supports 128-bit AES encrypted bitstreams for FPGA core or FROM programming. The AES key is securely stored on-chip in ProASIC3/E Flash FPGAs during programming and cannot be read back. The AES core in the ProASIC3/E device decrypts and authenticates the configuration bitstream prior to programming. This mechanism allows secure remote field updates (Figure 9).

The on-chip FROM in ProASIC3/E devices can be updated independently of the FPGA core using an AES-encrypted programming file or plain text.
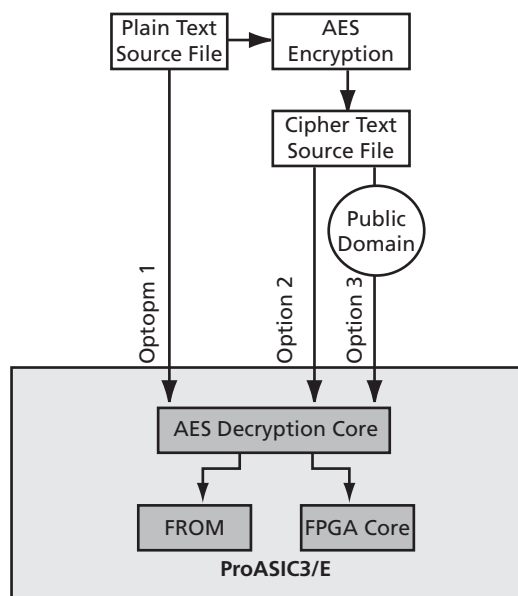

Figure 9: **ProASIC3 Programming Scenarios**

There are several ways to program a ProASIC3/E device. For example:

OPTION 0: ProASIC3/E devices can be programmed in-house with plain text.

OPTION 1: ProASIC3/E devices can be programmed in-house with an AES key only – final programming can happen at an untrusted site (contract manufacturer) using an AES-encrypted programming file.

OPTION 2: ProASIC3/E devices can be reprogrammed remotely using an AES-encrypted programming file for easy and secure field upgrades.

FlashPoint

FlashPoint is a software tool provided by Actel that enables a designer to generate a STAPL file with different contents for each ProASIC3/E device. For each case, optional AES encryption is available. To generate a STAPL file that contains different contents, the FlashPoint software needs an Array Map file, which represents the combination of the logic of the FPGA core generated by the Designer software, and a FROM configuration file generated by ACTgen tool (Figure 10).

The FlashPoint tool can generate a STAPL file with four different cases:

1. Single programming file – contents of both the FPGA core and FROM

2. Single programming file for the FPGA core and multiple FROM files for an application that uses device serialization

3. FPGA core programming file only

4. FROM programming file where the user can program the whole FROM or selectively program individual pages

The FlashPoint tool simplifies programming file generation and makes production faster and easier with ProASIC3/E devices. It also allows designers to use different FROM contents for different ProASIC3/E devices in production, and thereby accelerates implementation of the target application.
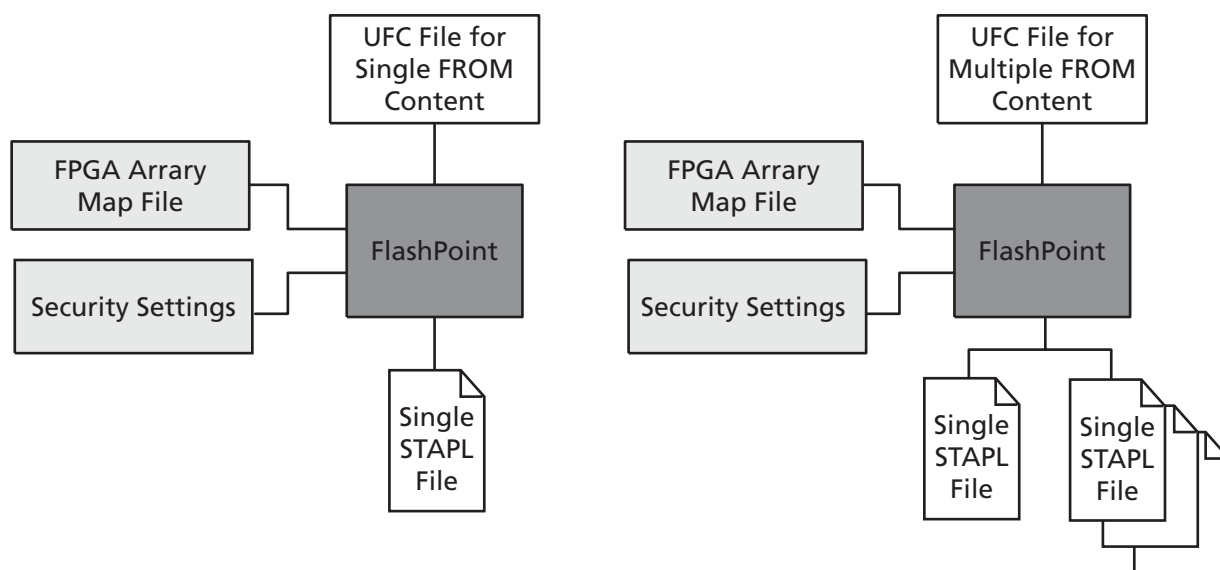

Figure 10: **Generation of Programming Files Using FlashPoint**

Device Serialization

By using the ProASIC3/E embedded FROM together with AES, designers can meet the requirements of many subscription-based or device serialization applications. ACTgen supports easy management of FROM contents over a large number of devices. The ACTgen tool can support FROM contents that contain the following:

- Static values
- Random numbers
- Values read from a file
- Independent updates of each page
- Auto-incrementing or auto-decrementing of fields

Summary

Today's rapidly shortening product life cycles, shrinking time-to-market windows, and relentless cost pressures have placed design teams in a bind. To address this highly dynamic and quickly changing marketplace, designers need a silicon solution that provides the flexibility and fast turnaround capabilities traditionally associated with FPGAs with the low unit cost, security, live-at-power-up, and power advantages historically found only in ASICs.

Based on an advanced and production-proven 130 nm Flash technology, Actel ProASIC3/E devices are addressing these challenges by delivering the first programmable devices that combine the best from both the ASIC and FPGA worlds. By bringing together in a single chip a programmable platform that offers low unit costs, low power, live-at-power-up capability, high levels of security, and firm-error immunity, ProASIC3/E devices offer designers the first production FPGAs capable of lowering total system costs and accelerating development in high-volume applications.

For more information, visit our website at **www.actel.com**

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