Flash FPGAs in the Value-Based Market

White Paper

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Introduction

Field programmable gate arrays (FPGAs) have a well-established position in every systems engineer's toolbox. FPGAs have been used by engineers for many years to rapidly prototype systems or meet low-volume preproduction requirements. When the communications- and network-driven Internet bubble took off at the turn of the millennium, demand skyrocketed for FPGAs in higher gate densities at any cost. Since then, FPGA requirements have changed dramatically. Today, as companies increasingly focus on the bill-of-materials bottom line, engineers look for silicon solutions that offer both low unit and low total system costs.

ASICs and structured arrays have traditionally offered the lowest unit cost of any silicon solution at high volumes. However, escalating time-to-market pressures, exponentially increasing nonrecurring engineering (NRE) charges, and the rising need to mitigate risk are preventing ASICs from addressing system designers' needs. Instead, a new ASIC alternative, the value FPGA, has emerged to address engineers' requirements for a technology capable of meeting today's shrinking development cycles with a low-cost structure. This paper examines the needs of the value-based FPGA market and describes the various FPGA-based ASIC alternative solutions available.

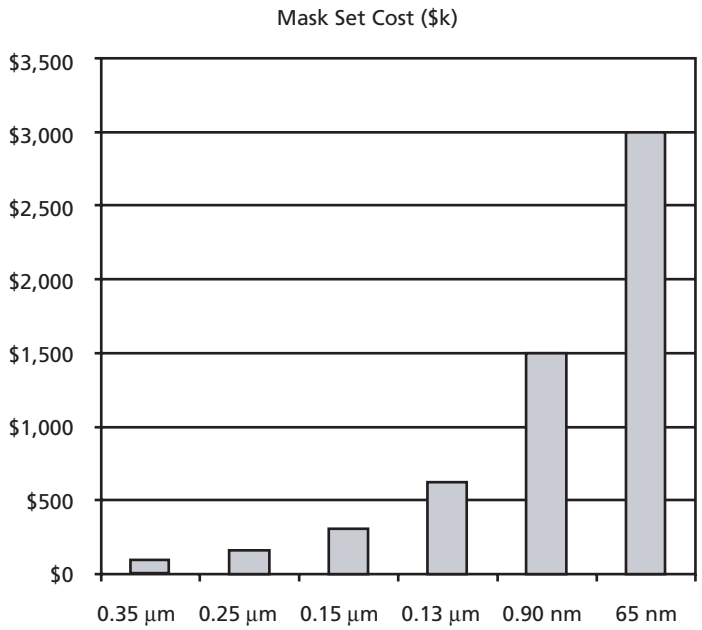

Figure 1: **Mask Set Costs by Technology**[1]

1. *Piper Jaffery/FSA*

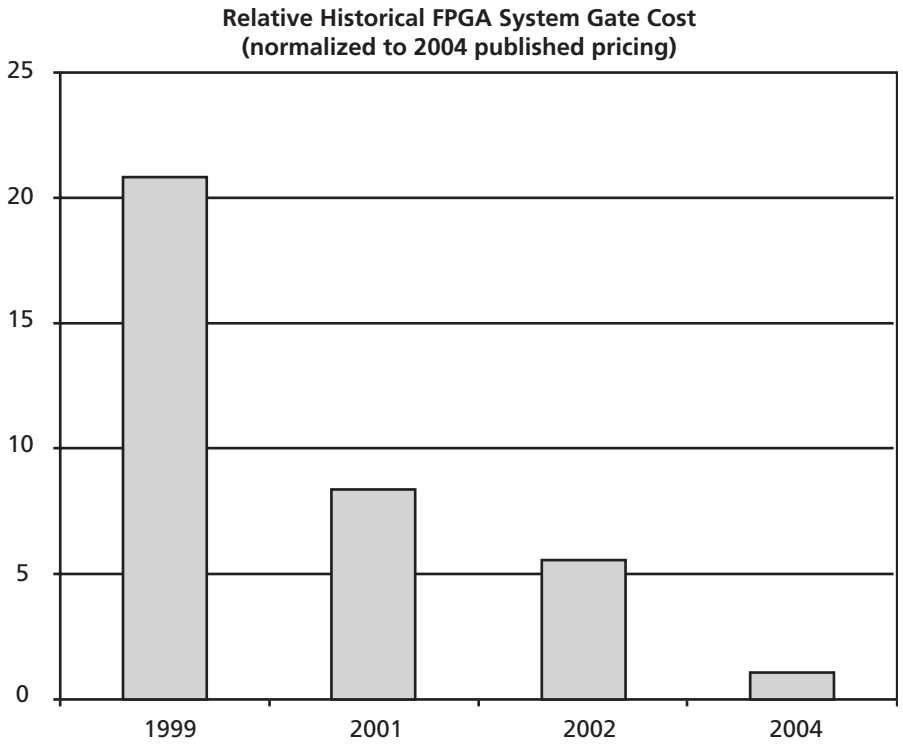

Figure 2: **Relative Cost of Value-Based FPGAs Normalized to 2004 = 1**

New Opportunities for FPGAs

Two factors are driving the rapid evolution of the value-based FPGA market. The first is the accelerating decline in FPGA unit costs. Leveraging advances in semiconductor process technology and ongoing manufacturing efficiencies, FPGA vendors are now able to offer programmable devices at unit costs comparable to traditional ASICs. Previously, FPGAs were not widely used in highly cost-sensitive markets due to higher unit costs.

At the same time, skyrocketing ASIC NREs are driving up ASIC unit costs. Today, it is common to see mask costs for a standard cell ASIC design amount to millions of dollars. As mask costs have risen, so have the effective unit costs of ASIC solutions, particularly in projects running under 500 k units. As a result, value-based FPGA alternatives are becoming increasingly attractive.

Market analysts' projections of growth in the programmable logic market reflect these trends (Figure 3 on page 5). First, analysts predict the use of FPGAs will continue to grow dramatically. With a Compound Annual Growth Rate (CAGR) of over 15 percent, analysts expect that the overall programmable logic market will nearly triple in size between 2002 and 2008. Second, analysts predict this growth will be driven by the rapid adoption of programmable logic within the automotive and consumer market segments. The use of FPGAs in consumer applications is forecast to grow to more than $1B by 2008, almost 10 times its 2002 revenue levels. Much of this growth will be fueled by the worldwide adoption of new digital and high-definition broadcast TV transmission standards, gaming and multimedia entertainment systems, LCD and plasma display technology, and the widespread use of home DVR and DVD-W technologies. In the automotive market, FPGAs will be increasingly used for in-cab entertainment systems and in-cab GPS navigation, information, communication, and safety systems. In both market segments, designers are turning to FPGAs for the unique advantages they offer in terms of rapid deployment and programmability

and their growing availability at lower price points. Value FPGAs are also finding their way into many data and telecom cost-reduction programs.

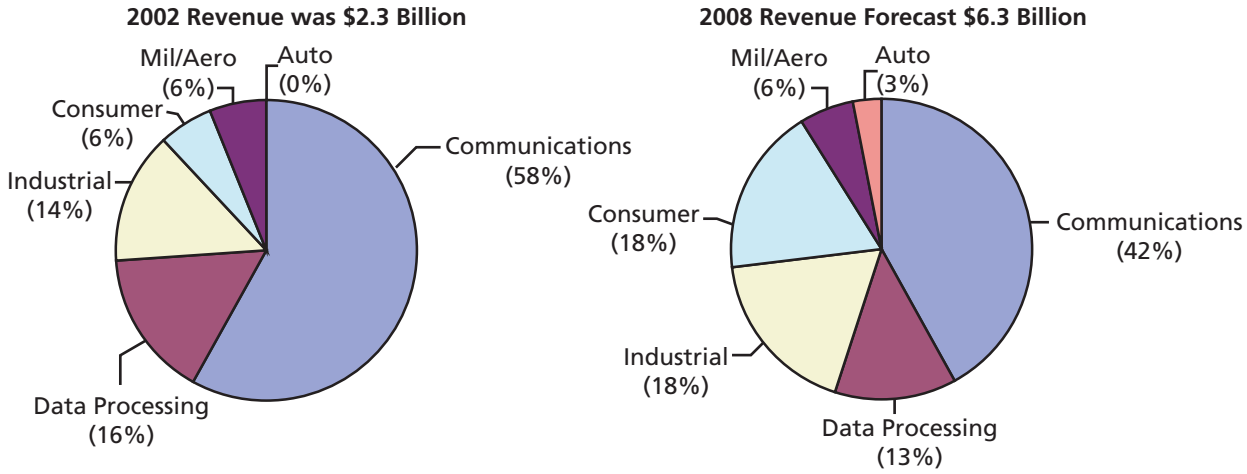

Figure 3: **Programmable Logic Revenue by End Market[2]**

Defining User Needs

Given the high growth rate forecast for the value-based FPGA market, FPGA vendors are aggressively positioning their technology as the best solution for these emerging applications. Many have begun promoting their products as the "world's lowest cost FPGA" and "the ASIC alternative" technology. Clearly, this battle will be fought at ASIC price points. But to successfully serve as an "ASIC alternative," value FPGAs must demonstrate a unit cost price structure that is highly competitive with ASIC unit costs plus their NRE. This new class of FPGAs must offer ASIC-like price points of sub-$2, sub-$5, sub-$10, and sub-$20.

Moreover, FPGAs in this new market must also match many of the additional characteristics that have made ASICs attractive in high-volume applications. The ASIC-like features that will factor heavily in the "ASIC alternative" (value FPGA) decision-making process include: high performance, low power, security, reliability, live at power-up, single chip, small form factor, and ease of use. It is important to note that these capabilities are either not available or come at a cost with some FPGA technologies. The additional cost must be factored into the overall unit cost of the solution.

Security and reliability are particularly important issues within the rapidly growing consumer and automotive electronics markets. For FPGA technology to be widely adopted in the consumer market, designers must be able to use the technology to protect the profits of consumer equipment manufacturers (CEMs). The highly competitive nature of the consumer market and the high-product run rates make consumer products highly attractive targets for theft. In a growing number of products, designers are implementing the easily replaceable portions of the product in standard, off-the-shelf parts while the value-added aspects of the system are embedded in FPGAs. The adoption rate of FPGAs in this market will depend in large part on the ability of FPGA technology to protect those unique value-added features. If a potential thief can steal a design by simply copying the FPGA code being loaded into an SRAM-based device, CEMs are unlikely to adopt programmable logic technology on a wide scale. So in many ways, the security capabilities of FPGA technology are more critical to the success of the product in low-cost, value FPGA applications than they are in applications that use higher priced, full-featured FPGAs.

2. *Source: Gartner*

Customers in the high-volume automotive market demand very high levels of quality and reliability. Some FPGAs, specifically those based on SRAM technology, suffer from reliability problems associated with neutron-induced configuration errors. These so-called "firm errors", while more prevalent at higher altitudes, are still a significant problem at "commercial" altitudes (less than 5,000 feet above sea level). Firm errors can cause an SRAM FPGA's design to change unexpectedly, possibly leading to a system malfunction. Independent data has shown that firm errors are the predominant failure mechanism in SRAM-based FPGAs at all altitudes, and that they have a failure rate up to two orders of magnitude higher than industry norms at commercial altitudes. In high-volume applications, such as those found in the automotive and consumer electronics market, ensuring product quality and reliability are key criteria for achieving market success and issues that must be addressed by the value FPGA product offerings.

Technology Options

FPGA vendors offer three fundamental technologies in this value, FPGA market segment: antifuse FPGAs, such as the Actel eX FPGA family; Flash FPGAs, such as the Actel ProASIC3 families; and SRAM-based FPGAs, which are offered by other vendors. At a glance, it is easy to assume that two of these FPGA technologies offer similar characteristics and capabilities: Flash and SRAM-based FPGAs are both in-system programmable, offer high-performance programmable logic, and are available in densities of 1 M system gates or more. However, there are very significant differences between the two technology offerings.

As with ASICs, the nonvolatile nature of reprogrammable Flash-based ProASIC3 devices provides key advantages over volatile SRAM-based offerings. ProASIC3 FPGAs use a Flash programming cell to control the gate of the switch within the FPGA fabric. Each switch has a single sense gate (the switch) and a single Flash floating gate that controls the state of the switch. In contrast, SRAM-based FPGAs rely on a six-transistor SRAM element for switch control and a pass gate for the switch itself. Unlike Flash-based ProASIC3 devices, the volatile SRAM FPGA programming element must be loaded from an external device at every system power-up. This difference means that Flash-based FPGAs are single-chip and live at power-up, which can translate into significant board-level cost savings.

From a system security standpoint, Flash-based FPGAs are the only value FPGA technology that is secure, immune from firm errors, and supports secure remote updates over public networks. This higher level of security offers better protection against theft of critical IP. The devices' firm error immunity reduces the CEM's risk of product liability and increases system reliability. The capability to conduct secure remote updates enables the product developer to update the product after deployment and, in the process, support a subscription-based business model through remote updates for feature enhancement. This capability can also eliminate the need for expensive service-based "truck rolls" to fix problems in the field.

Moreover, the inclusion of a small, nonvolatile memory (NVM) in Flash devices can serve as an enabling technology in many consumer and automotive applications. The NVM can be used to store encryption keys for secure communications or to support device serialization in set-top boxes for broadcast-based systems.

Cost Comparisons

ProASIC3 Flash-based FPGAs start at the industry's lowest cost point – $1.50 (250 k units). ProASIC3 includes four device densities with over 10 part package combinations for under $5 (250 k). Seven densities of the device with over 20 package combinations are available for under $10 (250 k). ProASIC3 has the lowest unit cost and the broadest product offering at ASIC-like price points in the value-FPGA market. In comparison, SRAM-based solutions provide at best two to three device densities under $10 and only a single device at the sub-$5 ASIC-like price point.

To compete with the unit cost advantages that Flash-based FPGAs enjoy, SRAM FPGA solutions must be implemented on the most aggressive process technologies. However, this aggressive use of process technology comes at the expense of total system cost. Designs using SRAM-based value-FPGA solutions must add expensive board-level infrastructure to support the technology. This undermines the cost benefit of the value SRAM FPGA.

FPGAs based on SRAM technology have always required additional support circuitry, and SRAM value FPGAs are no different. Each SRAM-based FPGA requires a boot PROM or microcontroller to load the FPGA configuration data. To ensure system reliability, designers often add an SRAM power supply brownout detection device. Moreover, many designs using SRAM-based FPGAs require a live at power-up complex programmable logic device (CPLD) to manage system start up, especially if a microcontroller is being used to load the SRAM FPGA.

SRAM-based FPGAs fabricated in the latest 90 nm processes must also meet stringent specifications on power-up as well as tight power supply tolerances, which often require costly supply sequencing devices to manage power to the part. In many applications, external clock distribution devices must handle system clock management because the SRAM FPGA's power-up configuration delay makes the device's internal PLL/DLL circuitry unsuitable for this important system-level task. In all, a "value" SRAM-based FPGA may require anywhere from $3 to $20 of support circuitry. Accordingly, that additional cost must be considered to determine the true cost of value SRAM-based FPGAs. The SRAM system overhead penalty can easily be over 100 percent of the SRAM FPGA’s unit cost price and that is without looking at the soft costs, reliability, inventory management, and design complexity issues.

In contrast, the cost savings of Flash-based FPGAs extend well beyond the unit cost (Table 1). The ASIC-like single-chip, live at power-up nature of Flash-based FPGAs allows designers to eliminate the additional devices associated with the SRAM FPGA. Unlike SRAM-based FPGAs, Flash-based ProASIC3 devices offer a true ASIC-like approach to the board-level design. ProASIC3 devices support single (1.5 V) power supply based designs, which eliminate the need for additional voltage regulators. These devices power up and down in a controlled and predictable way. Since they are inherently low-power, they reduce power supply requirements, enhance system reliability, and lower system thermal management costs. By supporting the use of separate power pins (same voltage) to inputs and outputs, Flash-based FPGAs reduce noise and may contribute to reduced EMI emissions. Additionally, by reducing component count, they help designers minimize PCB size.

Table 1: **Comparing ASIC and ASIC Alternative Features**

		Comparing ASIC Alternatives	
ASICs	**Key Metrics**	**ProASIC3/E FPGAs**	**Value (SRAM) FPGAs**
$$$	NRE	None	None
$	Unit Cost	Leadership	$
$	Total System Cost	Leadership	SRAM Penalty
✓	Performance	Meets Market Needs	Meets Market Needs
✓	Live at Power Up	Leadership	No
✓	Single Chip	Leadership	No
✓	Low Power	✓	No
✓	Security	Leadership	No
No	Secure ISP	Leadership	No
✓	Reliability	Leadership	High Failure in Time (FIT) rate from firm errors
Additional NRE	User NVM	Leadership	No

Summary

Technology constantly changes to meet the needs of the marketplace. Over the past 10 years, Flash technology has rapidly evolved from an innovative idea into a disruptive technology, dramatically impacting every application it has touched. It has transformed cell phones, cameras, video recorders, simple PLDs, microcontrollers, and memory solutions into revolutionary variants of their predecessors. Today, Flash technology is poised to do the same for the programmable logic market. By transforming the cost structure of basic feature set FPGAs, Flash technology promises to bring the flexibility and rapid deployment advantages of programmable logic to the value-based FPGA market.

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