CoreAHBLite Datasheet

DirectCore

Product Summary

Intended Use

- Intended for Use in a CoreMP7-Based Subsystem to Implement the AHB-Lite Bus Fabric. It Is Configured for Easy and Automatic System Design with CoreConsole

Key Features

- Supplied in SysBASIC Core Bundle
- Implements a Single Master AMBA AHB-Lite Bus Fabric
- Up to 16 AHB Slave Devices Supported
- Automatic Stitching of AHB Slaves in CoreConsole
- Supports Remapping of Slot0 and Slot1 to Facilitate Processor Boot

Benefits

- Allows Easy Connection of AHB Devices to a CoreMP7 Subsystem
- Auto Stitch in CoreConsole for rapid development
- Compatible with AMBA and CoreMP7

ARM Supported Families

- ProASIC®3 (M7A3P)
- ProASIC3E (M7A3PE)
- Fusion (M7AFS)

Synthesis and Simulation Support

- Supported in the Actel Libero® Integrated Design Environment (IDE)

Verification and Compliance

- Compliant with AMBA

Contents

General Description

CoreAHBLite implements the AHB-Lite bus fabric for a subsystem. CoreAHBLite is distinguished from CoreAHB in that it accommodates a single master only. Up to 16 AHB slaves can be present on the bus. From a memory map point of view, all AHB slaves are allocated an equal amount (256 MB) of memory.

AHB-Lite Overview

The CoreAHBLite bus component available in CoreConsole essentially implements an AHB-Lite bus fabric. AHB-Lite is a subset of the full AHB specification and is intended for use in designs where there is only a single bus master.

AHB-Lite simplifies the AHB specification by removing the protocol required for multiple bus masters. This includes arbitration based on a request/grant type mechanism and split/retry responses from AHB slaves.

The basic structure of this fabric is shown in Figure 1 on page 2. The elements labeled "Decoder" and "Read Data/Response MUX" in Figure 1 on page 2 are contained within the CoreAHBLite component.

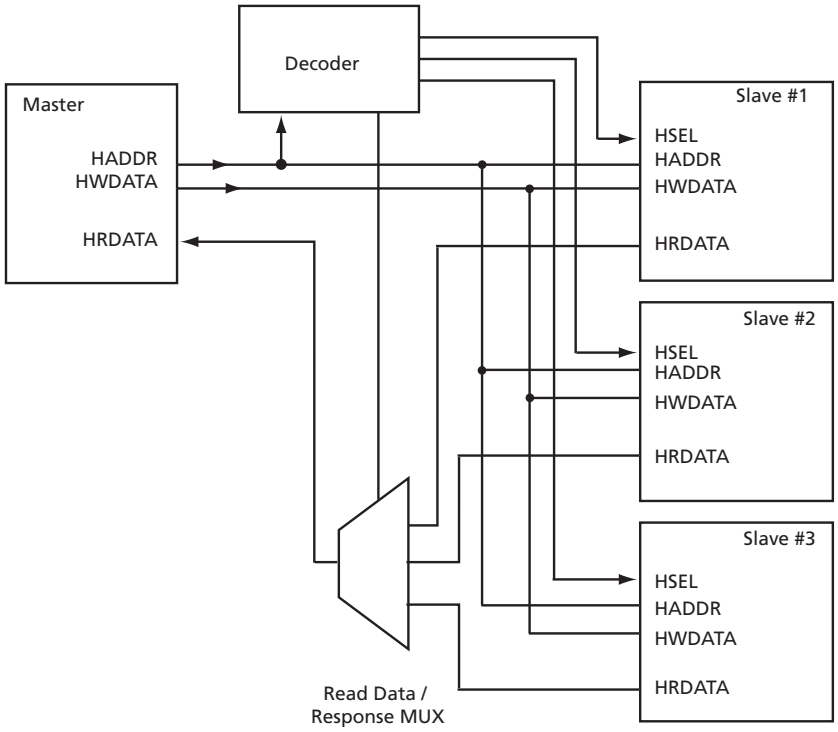

Figure 1 • **CoreAHBLite Block Diagram**

Connecting the CoreAHBLite in CoreConsole

Table 1 lists the ports present on the CoreAHBLite and describes how to connect these in CoreConsole.

Table 1 • **AHB Bus Connections**

Connection	CoreConsole Label	Description
Required Connections		
AHB mirrored master interface	AHBmmaster	This interface connects to the AHB master. Normally this will be connected to the AHBmaster interface of the CoreMP7Bridge.
HCLK	HCLK	AHB system clock input. Connect this to the HCLK output of the CoreMP7Bridge.
HRESETn	HRESETn	Active low AHB system reset. Connect this to the HRESETn output of the CoreMP7Bridge.
Optional Connections		
	AHBmslave0	AHB mirrored slave 0 interface. Normally connected to AHBslave_base interface of Memory Controller.
	AHBmslave1	AHB mirrored slave 1 interface
	AHBmslave2	AHB mirrored slave 2 interface
	AHBmslave3	AHB mirrored slave 3 interface
	AHBmslave4	AHB mirrored slave 4 interface
	AHBmslave5	AHB mirrored slave 5 interface
	AHBmslave6	AHB mirrored slave 6 interface
	AHBmslave7	AHB mirrored slave 7 interface

Table 1 • **AHB Bus Connections (Continued)**

Connection	CoreConsole Label	Description
	AHBmslave8	AHB mirrored slave 8 interface
	AHBmslave9	AHB mirrored slave 9 interface
	AHBmslave10	AHB mirrored slave 10 interface
	AHBmslave11	AHB mirrored slave 11 interface
	AHBmslave12	AHB mirrored slave 12 interface
	AHBmslave13	AHB mirrored slave 13 interface
	AHBmslave14	AHB mirrored slave 14 interface
	AHBmslave15	AHB mirrored slave 15 interface

CoreAHBLite Port List

Table 2 lists the ports present on the CoreAHBLite. Four groups of signals can be identified:

1. Common AHB system signals (clock and reset)
2. AHB mirrored master interface. This connects to the master on the AHB Bus. A mirrored master interface is made up of the same signals as a master interface but the direction of the signals is reversed.
3. Signals common to all 16 AHB mirrored slave interfaces. These are AHB master signals which connect to all slaves.
4. AHB mirrored slave (master) signals specific to each slave.

Table 2 • **Ports on the AHB Bus Component**

Signal	Direction	Description
Common AHB System Signals		
HCLK	Input	Bus clock. This clock times all bus transfers. All signal timings are related to the rising edge of HCLK.
HRESETn	Input	Reset. The bus reset signal is active low and is used to reset the system and the bus. This is the only active low AHB signal.
Mirrored AHB Master Interface		
HADDR[31:0]	Input	This is the 32-bit system address bus.
HTRANS[1:0]	Input	Transfer type. Indicates the type of the current transfer: 00 – Idle 01 – Busy 10 – Non-Sequential 11 – Sequential
HWRITE	Input	Transfer direction. When high, this signal indicates a write transfer; when low, indicates a read transfer.
HSIZE[2:0]	Input	Transfer size. Indicates the size of the transfer, which can be byte (8-bit), halfword (16-bit), or word (32-bit).
HBURST[2:0}	Input	Burst type. Indicates if the transfer forms part of a burst. The CoreMP7 performs incrementing bursts of type INCR.
HPROT[3:0]	Input	Protection control. These signals indicate if the transfer is an opcode fetch or data access, and if the transfer is a Supervisor mode access or User mode access.
HWDATA[31:0]	Input	32-bit data from the master.
HRDATA[31:0]	Output	32-bit date written back to the master.
HREADY	Output	Transfer done. When high the HREADY signal indicates that a transfer has finished on the bus. This signal can be driven low to extend a transfer.
HRESP[1:0]	Input	Transfer response. Indicates an Okay Error Retry, or Split response.

Table 2 • **Ports on the AHB Bus Component (Continued)**

Signal	Direction	Description
Common AHB Mirrored Slave Signals		
HADDRS[31:0]	Output	This is the 32-bit system address bus.
HTRANSS[1:0]	Output	Transfer type. Indicates the type of the current transfer: 00 – Idle 01 – Busy 10 – Non-Sequential 11 – Sequential
HWRITES	Output	Transfer direction. A write transfer is indicated when this signal is high and a read transfer is indicated this signal is low during the address phase of an AHB transfer.
HSIZES[2:0]	Output	Transfer Size. Indicates the size of the transfer, which can be: 00 – byte (8-bit) 01 – halfword (16-bit) 10 – word (32-bit)
HBURSTS[2:0]	Output	Burst type. Indicates if the transfer forms part of a burst.
HPROTS[3:0]	Output	Protection control. These signals indicate if the transfer is an opcode fetch or data access, and if the transfer is a Supervisor mode access or User mode access.
HWDATA[31:0]	Output	32-bit data to the slave
HREADYS	Output	Transfer done. Out to the slaves (alias of HREADY)
Slave-Specific Mirrored Slave Signals		
HSELx	Output	Select of slave x (where x is an integer between 0 and 15)
HRDATASx[31:0}	Input	32-bit read data from slave x.
HREADYSx	Input	Ready signal from slave x. When high indicates that slave has completed transfer and is ready for another transfer.
HRESPSx[1:0]	Input	Transfer response from slave x which can be: 00 – Okay 01 – Error 10 – Retry 11– Split
Remap	Input	Swap (remap) slot1 to slot0 if Remap = 1. Leave as configured if Remap = 0.

Remapping

There is a remap input on CoreAHBLite. This can be connected to the remap output of CoreRemap, which will allow software control of the mapping of slot0 and slot1. It can be left unconnected (defaulting to 0 and having no effect) or it can be controlled from an external signal, either directly or via the input on CoreRemap. The intended use of the Remap input is to address a typical system design requirement of locating nonvolatile memory at 0 (for booting the processor) with volatile RAM at slot1. For performance and other reasons, it is often desirable to boot from nonvolatile memory, then copy the contents of that memory into RAM and execute the program from there. This can be achieved with the Remap input.

Resource Requirements

The utilization for CoreAHBLite in a ProASIC3E device is 700 tiles.

Ordering Information

CoreAHBLite is included in the SysBASIC core bundle that is supplied with the Actel CoreConsole IP Deployment Platform tool. The obfuscated RTL version of SysBASIC (SysBASIC-OC) is available for free with CoreConsole. The source RTL version of SysBASIC (SysBASIC-RM) can be ordered through your local Actel sales representative. CoreAHBLite cannot be ordered separately from the SysBASIC core bundle.

Datasheet Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," and "Production." The definitions of these categories are as follows:

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The product brief is a summarized version of an advanced or production datasheet containing general product information. This brief summarizes specific device and family information for unreleased products.

Advanced

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

Unmarked (production)

This datasheet version contains information that is considered to be final.

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