CoreAI

FlashLock

Product Summary

Intended Use

- Analog Interface Control Using a Microprocessor/ Microcontroller and an Actel Fusion™ Device
- Voltage, Current, and Temperature Monitoring Using a Microprocessor/Microcontroller and an Actel Fusion Device

Key Features

- ADC Conversions Controlled by MCU/MPU Writes
- AMBA APB Slave Interface (8- or 16-Bit Data Widths Supported)
- 14 Maskable Interrupt Sources
- Internal Clock Divider for Generating Analog Configuration MUX Clock
- Optional Read FIFO Stores up to 256 ADC Conversion Results
- Analog Configuration MUX Can Be Configured by SmartGen

Supported Families

- Fusion (including M7 devices)

Core Deliverables

- Evaluation Version
  - Compiled RTL Simulation Model Fully Supported in Actel Libero® Integrated Design Environment (IDE)
- Netlist Version
  - Structural Verilog and VHDL Netlists (with and without I/O Pads) Compatible with Actel Designer Software Place-and-Route Tool
  - Compiled RTL Simulation Model Fully Supported in Actel Libero IDE
- RTL Version
  - Verilog and VHDL Core Source Code
  - Core Synthesis Scripts
- Testbench (Verilog and VHDL)

Synthesis and Simulation Support

- Directly Supported within Actel Libero IDE and CoreConsole
- Synthesis: Synplicity®, Synopsys® (Design Compiler / FPGA Compiler / FPGA Express), Exemplar
- Simulation: OVI-Compliant Verilog Simulators and Vital-Compliant VHDL Simulators

Core Verification

- Comprehensive VHDL and Verilog Testbenches
- User Can Easily Modify User Testbench Using Existing Format to Add Custom Tests

General Description

CoreAI (Analog Interface) allows for simple control of the analog peripherals within the Fusion family of Actel devices. Control may be implemented with an internal or external microprocessor or microcontroller (such as Core8051 or CoreMP7), or with user-created custom logic within the FPGA fabric. The industry-standard AMBA (Advanced Microcontroller Bus Architecture) APB (Advanced Peripheral Bus) slave interface is used as the primary control mechanism within CoreAI.

CoreAI instantiates the AB (Analog Block) macro, as shown in Figure 1 on page 2. The AB macro includes the ACM (Analog Configuration MUX) interface, Analog Quads, and RTC (Real-Time Counter). The ACM interface, within the AB macro, is used to control configuration of the Analog Quads and RTC in the Fusion device. CoreAI generates the control signals used by the ACM, including its clock signal, which is generated by an internal clock divider. The ACM clock divider is used to ensure that the ACM interface is clocked at a frequency less than or equal to 10 MHz. For more details on the silicon features of the AB macro, such as the Analog Quads, RTC, or ACM, refer to the *Fusion datasheet*.

Several aspects of CoreAI can be configured using top-level parameters (Verilog) or generics (VHDL). For a detailed description of the parameters/generics, refer to the *CoreAI datasheet*.

The CoreAI block diagram is shown in Figure 1. A typical application using CoreAI is shown in Figure 2.

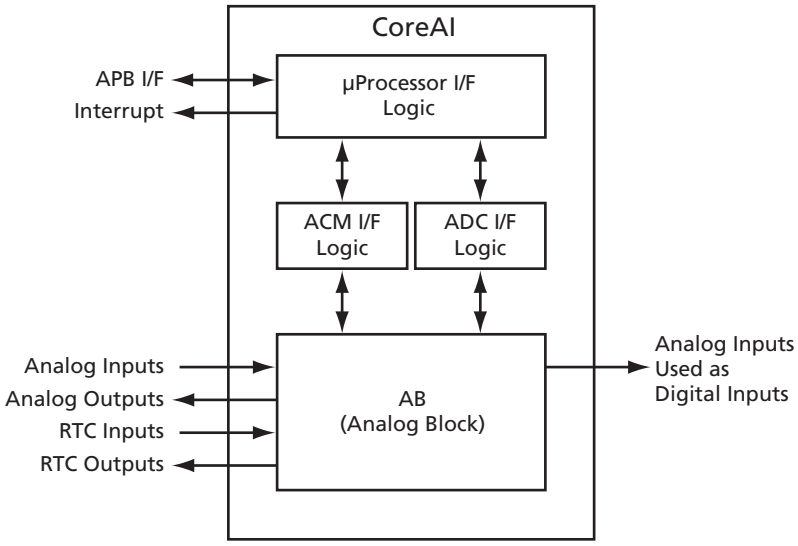

Figure 1 • **CoreAI Block Diagram**

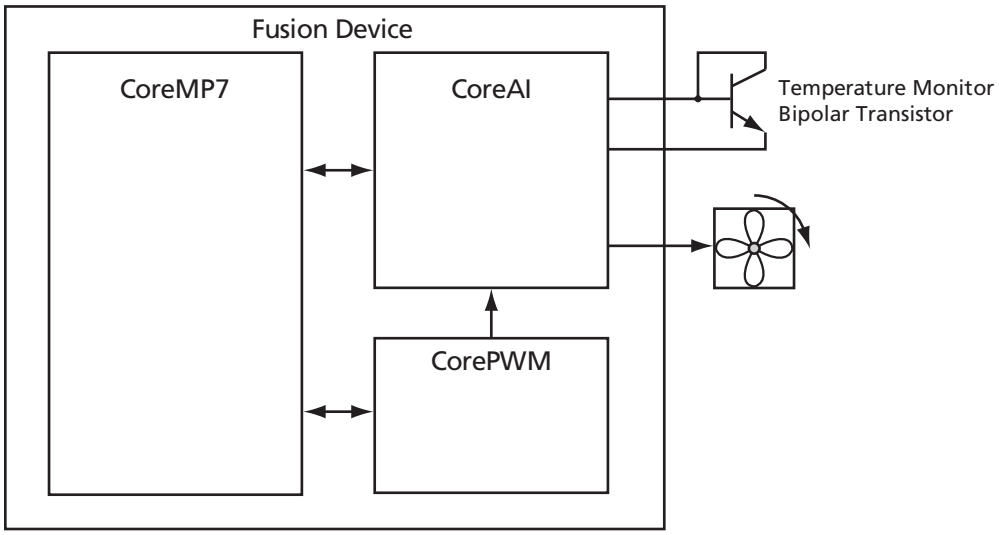

Figure 2 • **CoreAI Typical Application**

Functional Block Descriptions

CoreAI, shown in Figure 1, consists of the microprocessor interface logic, ACM interface logic, and ADC interface logic blocks. The microprocessor interface logic implements APB slave logic and generates a maskable interrupt. The ACM interface block writes configuration data into the AB macro to control Analog Quad and RTC settings. The ADC interface block sends control data to and receives status information from the ADC.

CoreAI Device Requirements

CoreAI has been implemented for use in the Actel Fusion device family. A summary of the data for CoreAI is listed in Table 1 and Table 2.

Table 1 • **CoreAI Device Utilization and Performance (minimum configuration)**

Family	Cells or Tiles			Utilization		Performance
	Sequential	Combinatorial	Total	Device	Total	
Fusion	45	105	150	AFS090	7%	150 MHz

Note: *Data in this table were achieved using typical synthesis and layout settings. Top-level parameters/generics that differ from the default values were set as follows: FIXED_VAREFSEL = 1, FIXED_VAREFSEL_VAL = 0, FIXED_MODE = 1, FIXED_MODE_VAL = 0, FIXED_TVC = 1, FIXED_TVC_VAL = 0, FIXED_STC = 1, FIXED_STC_VAL = 0, CFG_ACx = 512, CFG_ATx = 512, DISABLE_TMSTBINT = 1, CFG_GDx = 768, ACTLOW_INTERRUPT = 0, DISABLE_INTERRUPT = 1, APB_16BIT_DATA = 1.*

Table 2 • **CoreAI Device Utilization and Performance (maximum configuration)**

Family	Cells or Tiles				Utilization		Performance
	Sequential	Combinatorial	Total	FIFO	Device	Total	
Fusion	130	330	460	1	AFS090	20%	133 MHz

Note: *Data in this table were achieved using typical synthesis and layout settings. Top-level parameters/generics that differ from the default values were set as follows: ACM_CLK_DIV = 4, USE_RTC = 1, USE_RDFIFO = 1, USE_RDFIFO_AEVAL = 16, USE_RDFIFO_AFVAL = 240.*

CoreAI Verification

The comprehensive simulation testbench verifies correct operation of the CoreAI macro.

The testbench applies several tests to the CoreAI macro, including the following:

- Voltage monitor, current monitor, and temperature monitor tests
- RTC tests
- Gate-driver control tests

Using the supplied testbench as a guide, the user can alter the verification of the core by adding custom tests or removing existing tests.

I/O Signal Descriptions

The port signals for the CoreAI macro are defined in Table 3 and illustrated in Figure 3. CoreAI has 120 I/O signals. Note that vector notation is used in Figure 3 for the AV, AC, AT, ATRETURN, DDGDON, DAVOUT, DACOUT, DATOUT, AG, and RTCXTLMODE ports; however, these ports are actually split into individual single-bit ports, as described in Table 3. For example, there are two individual output ports, RTCXTLMODE1 and RTCXTLMODE0, rather than one vectored output port RTCXTLMODE[1:0].

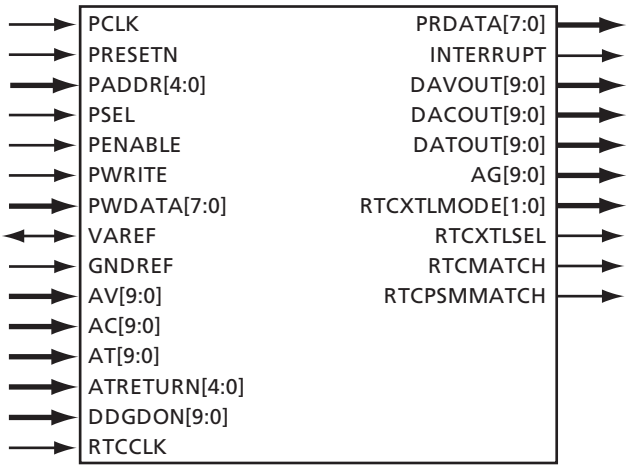

Figure 3 • **CoreAI I/O Signal Diagram**

Table 3 • **CoreAI I/O Signal Descriptions**

Name	Type	Description
APB Interface		
PCLK	Input	APB System Clock: reference clock for all internal logic
PRESETN	Input	APB active-low asynchronous reset
PADDR[4:0]	Input	APB address bus – This port is used to address internal CoreAI registers.
PSEL	Input	APB Slave Select – This signal selects CoreAI for reads or writes.
PENABLE	Input	APB Strobe – This signal indicates the second cycle of an APB transfer.
PWRITE	Input	APB Write/Read – If high, a write will occur when an APB transfer to CoreAI takes place; if low, a read from CoreAI will take place.
PWDATA[15:0]	Input	APB write data – If the APB_16BIT_DATA parameter/generic is set to 1, all 16 bits are used; if the APB_16BIT_DATA parameter/generic is set to 0, only the lower 8 bits, PWDATA[7:0], are used (in this case, PWDATA[15:8] should be tied to static high or low values).
PRDATA[15:0]	Output	APB read data – If the APB_16BIT_DATA parameter/generic is set to 1, all 16 bits are used; if the APB_16BIT_DATA parameter/generic is set to 0, only the lower 8 bits, PRDATA[7:0], are used (in this case, PRDATA[15:8] can be left unconnected).
INTERRUPT	Output	Microprocessor interrupt output – This interrupt signal is generated from 14 possible interrupt sources, each of which can be masked or enabled via the INTENABLE register. The polarity of this output is controlled via the ACTLOW_INTERRUPT parameter/generic.

Note: All signals active high (logic 1) unless otherwise noted.

Table 3 • **CoreAI I/O Signal Descriptions (Continued)**

Name	Type	Description
Analog Interface		
VAREF	Input or Output	Voltage reference – If using the internal voltage reference, this signal will be an output; if using an external voltage reference, this signal will be an input for this reference (see the FIXED_VAREFSEL and FIXED_VAREFSEL_VAL parameters/generics).
GNDREF	Input	Ground reference – If external voltage reference is used, this signal must be connected to the ground for the reference; otherwise this should be connected to digital ground (logic 0).
AV9, AV8, AV7, AV6, AV5, AV4, AV3, AV2, AV1, AV0	Input	Analog Voltage Monitor inputs – These signals correspond to the AVx voltage monitor inputs (AV9 through AV0) of the AB macro. **Note:** Unused AVx inputs need to be disabled with the CFG_AVx parameters/generics and connected to logic 0.
AC9, AC8, AC7, AC6, AC5, AC4, AC3, AC2, AC1, AC0	Input	Analog Current Monitor inputs – These signals correspond to the ACx current monitor inputs (AC9 through AC0) of the AB macro. **Note:** Unused ACx inputs need to be disabled with the CFG_ACx parameters/generics and connected to logic 0.
AT9, AT8, AT7, AT6, AT5, AT4, AT3, AT2, AT1, AT0	Input	Analog Temperature Monitor inputs – These signals correspond to the ATx temperature monitor inputs (AT9 through AT0) of the AB macro. **Note:** Unused ATx inputs need to be disabled with the CFG_ATx parameters/generics and connected to logic 0.
ATRETURN4, ATRETURN3, ATRETURN2, ATRETURN1, ATRETURN0]	Input	Shared Analog Temperature Monitor Returns – These signals correspond to the shared returns for the temperature monitor inputs (ATRETURN89 through ATRETURN01) of the AB macro.
DAVOUT9, DAVOUT8, DAVOUT7, DAVOUT6, DAVOUT5, DAVOUT4, DAVOUT3, DAVOUT2, DAVOUT1, DAVOUT0	Output	Digital AV outputs – These signals correspond to the digital AV outputs (DAVOUT9 through DAVOUT0) of the AB macro. If any of the AVx inputs are configured as digital inputs rather than analog inputs, their corresponding buffered digital signals are put out on these ports.
DACOUT9, DACOUT8, DACOUT7, DACOUT6, DACOUT5, DACOUT4, DACOUT3, DACOUT2, DACOUT1, DACOUT0	Output	Digital AC outputs – These signals correspond to the digital AC outputs (DACOUT9 through DACOUT0) of the AB macro. If any of the ACx inputs are configured as digital inputs rather than analog inputs, their corresponding buffered digital signals are put out on these ports.
DATOUT9, DATOUT8, DATOUT7, DATOUT6, DATOUT5, DATOUT4, DATOUT3, DATOUT2, DATOUT1, DATOUT0	Output	Digital AT outputs – These signals correspond to the digital AT outputs (DATOUT9 through DATOUT0) of the AB macro. If any of the ATx inputs are configured as digital inputs rather than analog inputs, their corresponding buffered digital signals are put out on these ports.
DDGDON9, DDGDON8, DDGDON7, DDGDON6, DDGDON5, DDGDON4, DDGDON3, DDGDON2, DDGDON1, DDGDON0	Input	Direct Digital Gate Driver enables – These signals can control the corresponding GDONx gate-driver enable inputs (GDON9 through GDON0) of the AB macro if the CFG_GDx parameters/generics are set appropriately (refer to the *CoreAI datasheet*).
AG9, AG8, AG7 AG6, AG5, AG4, AG3, AG2, AG1, AG0	Output	Analog Gate Driver outputs – These signals correspond to the AGx gate driver outputs (AG9 through AG0) of the AB macro. **Note:** If unused, each of these gate driver outputs can be disabled via the CFG_GDx parameters/generics.

Note: All signals active high (logic 1) unless otherwise noted.

Table 3 • **CoreAI I/O Signal Descriptions (Continued)**

Name	Type	Description
RTCCLK	Input	RTC Clock input – If the RTC is used (via the USE_RTC parameter/generic), this input must come from the internal crystal oscillator (XTLOSC) CLKOUT pin; if the RTC is not used, this pin should be tied low.
RTCXTLMODE1, RTCXTLMODE0	Output	RTC XTLOSC Mode outputs – If the RTC is used (via the USE_RTC parameter/generic), these output ports must be connected to the internal crystal oscillator (XTLOSC) RTCMODE[1:0] pins; if the RTC is not used, these pins should be left unconnected.
RTCXTLSEL	Output	RTC XTLOSC Mode Selection output – If the RTC is used (via the USE_RTC parameter/generic), this output port must be connected to the internal crystal oscillator (XTLOSC) MODESEL pin; if the RTC is not used, this pin should be left unconnected.
RTCMATCH	Output	RTC Match output – If the RTC is used (via the USE_RTC parameter/generic), this output port indicates that a match event has occurred and can be connected to other FPGA logic; if the RTC is not used, this pin should be left unconnected.
RTCPSMMATCH	Output	RTC Match VRPSM output – If the RTC is used (via the USE_RTC parameter/generic), this output port can be connected to the VRPSM pin of the internal voltage regulator to control regulator power-up; if the RTC is not used, this pin should be left unconnected.

Note: All signals active high (logic 1) unless otherwise noted.

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