CoreAhbSram Datasheet

DirectCore

Product Summary

Intended Use

- Provides an AHB Hardware Bus Interface to the Embedded SRAM Blocks within ProASIC®3, ProASIC3E, and Fusion devices

Key Features

- Supplied in SysBASIC Core Bundle
- Implements Standard Slave AHB Bus Hardware Interface
- 32-Bit Interface, Allowing Byte, Halfword, or Word Accesses to SRAM
- Ability to Logically Merge Multiple SRAM Blocks into One Large Area of SRAM

Supported Families

- ProASIC3 (M7A3P)
- ProASIC3E (M7A3PE)
- Fusion (M7AFS)

Core Deliverables

- VHDL and Verilog Delivered as Plaintext or Obfuscated RTL via Actel CoreConsole IP Deployment Platform
- Unit Test Delivered as CoreMP7 Bus Functional Model (BFM) Scripts, and Example AHB-Based System

Core Verification

- User Can Easily Modify User Testbench Using Existing Format to Add Custom Tests.

Contents

General Description

CoreAhbSram provides an AHB bus interface to the embedded SRAM memory blocks within ProASIC3, ProASIC3E, and Fusion devices. In these devices, software running on an AHB-based microprocessor will be able to read and write the embedded SRAM. Note that this datasheet focuses on the operation of the CoreAhbSram and does not provide detailed information on the structure or the behavior of the ProASIC3/E or Fusion SRAM memory. Refer to the *Actel ProASIC3 FPGA* or *Fusion Family of Mixed-Signal FPGAs* datasheets for details on the internal SRAM memory.

Device Utilization and Performance

Table 1 • **CoreAhbSram Device Utilization and Performance**

SRAM Size	Tiles	Performance (MHz)
2 kB	236	100
10 kB	552	118
28 kB	607	73

I/O Signal Descriptions

The port signals for the CoreAhbSram core are illustrated in Table 2.

Table 2 • **CoreAhbSram Port Signals**

Signal	Direction	Description
HCLK	Input	Bus clock. This clock times all bus transfers. All signal timings are related to the rising edge of HCLK.
HRESETn	Input	Reset. The bus reset signal is active low and is used to reset the system and the bus. This is the only active low AHB signal.
HADDR[14:0]	Input	This is a 15-bit bus which connects to the lower 15 bits of the 32-bit AHB system address bus.
HTRANS[1:0]	Input	Transfer type. Indicates the type of the current transfer: 00 – Idle 01 – Busy 10 – Non-Sequential 11 – Sequential
HWRITE	Input	Transfer direction. When high this signal indicates a write transfer and when low a read transfer.
HSIZE[2:0]	Input	Transfer size. Indicates the size of the transfer, which can be byte (8-bit), halfword (16-bit), or word (32-bit).
HWDATA[31:0]	Input	32-bit data from the master
HREADYIN	Input	Ready signal from all other AHB slaves
HSEL	Input	Combinatorial decode of HADDR, which indicates that this slave is currently selected
HRDATA[31:0]	Output	32-bit date written back to the master
HREADY	Output	Transfer done. When high the HREADY signal indicates that a transfer has finished on the bus. This signal can be driven low to extend a transfer.
HRESP[1:0]	Output	Transfer response, which has the following meanings: 00 – Okay 01 – Error 10 – Retry 11 – Split

Generic/Parameter Descriptions

CoreAhbSram has one generic (VHDL) or one parameter (Verilog), called RAM_BLOCK_INSTANCES. This can take on the values shown in Table 3. If instantiated within CoreConsole, this generic/parameter is set by means of selecting a value from a pull-down box within the configuration window.

Table 3 • **Generic/Parameter Descriptions**

RAM_BLOCK_INSTANCES	SRAM Size (kBytes)
4	2
20	10
28	14
56	28

These SRAM sizes correspond to the maximum SRAM available in the M7 (ARM®-enabled) cores shown in Table 4.

Table 4 • **Available SRAM on Actel M7 devices**

M7 Core	Available SRAM (kBytes)
M7A3P250	2
M7A3P1000	14
M7A3PE600	10
M7AFS600	10
M7AFS1500	28
M7A3PE1500	28

Timing Diagrams

The timing diagrams for CoreAhbSram are the normal AHB read and write timing diagrams available in the AHB specification from ARM.

Ordering Information

CoreAhbSram is included in the SysBASIC core bundle that is supplied with the Actel CoreConsole IP Deployment Platform tool. The obfuscated RTL version of SysBASIC (SysBASIC-OC) is available for free with CoreConsole. The source RTL version of SysBASIC (SysBASIC-RM) can be ordered through your local Actel sales representative. CoreAhbSram cannot be ordered separately from the SysBASIC core bundle.

Datasheet Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," and "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of an advanced or production datasheet containing general product information. This brief summarizes specific device and family information for unreleased products.

Advanced

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

Unmarked (production)

This datasheet version contains information that is considered to be final.

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