Generating Power on Reset for CoreMP7

Introduction

The state of a system at startup is an important consideration in designing most types of circuits. It is usually desirable to provide an input signal at startup to reset synchronous circuitry. Otherwise, the system may initially operate in an unpredictable fashion because flip-flops are not designed to power-on in any particular state.

This is especially true if a microprocessor like CoreMP7 (the Actel optimized soft IP ARM7) is resident in the system, as the potential exists for the processor to execute runaway code prior to the completion of the initialization sequence. Further, ARM® requires that the nRESET pin of the ARM7TDMI-S™ processor (the Actel CoreMP7 processor) is held asserted for a minimum of two MCLK cycles to fully reset the processor core logic. Refer to the *CoreMP7* datasheet for any requirements in relation to the reset circuitry.

Most systems will have a dedicated power management device, similar to those devices offered by Maxim Integrated Products or Linear Technology. However, this application brief will focus on those systems that do not have a dedicated power controller and will implement a simple Power-on Reset (PoR) circuit using an FPGA I/O and core logic.

M7 ProASIC3 and ProASIC3E Architecture

The M7 ProASIC3/E devices do not make the internal PoR signal directly available to the FPGA core or I/O structures. The internal PoR signal can be used as a predecessor to generate a usable PoR signal for the microprocessor IP cores.

Power Supplies

Actel M7 ProASIC3/E devices are Flash-based FPGAs manufactured on a 0.13 µm process node. M7 ProASIC3/E devices offer a single-chip, reprogrammable solution and support Level 0 live at power-up (LAPU) due to their nonvolatile architecture.

Three main voltage pins are used by ProASIC3/E devices during normal operation:

- V_{CC}: Voltage supply to the FPGA core
- V_{CCI}Bx[1]: Supply voltage to the bank's I/O output buffers and logic
- VMVx[1]: Quiet supply voltage to the input buffers of each I/O bank

The bank VMV pin must be tied to the V_{CCI} pin of the same bank. Therefore, the supplies that need to be powered up/down during normal operation are V_{CC} and V_{CCI}. These power supplies can be powered up/down in any sequence during normal operation of M7 ProASIC3/E FPGAs. During power-up, I/Os in each bank will remain tristated until the last supply (being either V_{CCI}Bx or V_{CC}) reaches its functional activation voltage. Similarly, during power-down, I/Os in each bank are tristated once the first supply reaches its brownout deactivation voltage.

I/O Behavior at Power-Up and Power-Down

As mentioned earlier, VMVx and V_{CCI}Bx are tied together and therefore inputs and outputs are powered up/down at the same time. The behavior of the I/Os during power-up/down is not solely dependent upon the I/O bank supplies, but also the FPGA core supply. This section examines the various conditions of power sequencing in regards to the I/O bank and FPGA core voltages and their effects on the I/O pins.

1. *The 'x' represents the I/O bank number; refer to the ProASIC3 and ProASIC3E datasheets located at http://www.actel.com/techdocs/ds for further information.*

I/O State During Power-Up/Down

Before the start of power-up, all I/Os are in tristate mode. The I/Os will remain tristated during power-up until the last voltage supply (V_{CC} or V_{CCI}) is powered to its functional level (power supply functional levels are discussed in the "Power-Up to Functional Time" section on page 3). After the last supply reaches the functional level, the outputs will exit the tristate mode and drive the logic at the input of the output buffer. Similarly, the input buffers will pass the state of the external logic into the FPGA fabric once the last supply reaches the functional level. The behavior of user I/Os is independent of the V_{CC} and V_{CCI} sequence or the state of other voltage supplies of the FPGA (VPUMP and VJTAG). Figure 1 shows the output buffer behavior during power-up with 10 kΩ external pull-down. In Figure 1, V_{CC} is powered first, and V_{CCI} is powered 5 ms after V_{CC}. Figure 2 shows the state of the I/O when V_{CCI} is powered about 5 ms before V_{CC}. In the circuitry shown in Figure 2, the output is externally pulled down. During power-down, device I/Os become tristated once the first power supply (V_{CC} or V_{CCI}) drops below its brownout voltage level. The I/O behavior during power-down is also independent of voltage supply sequencing.

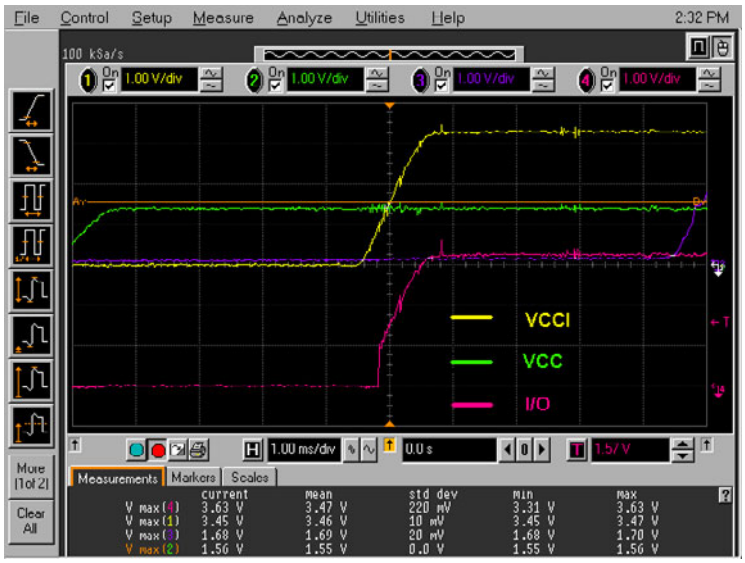

Figure 1 • **I/O State When V_{CC} is Powered Before V_{CCI}**

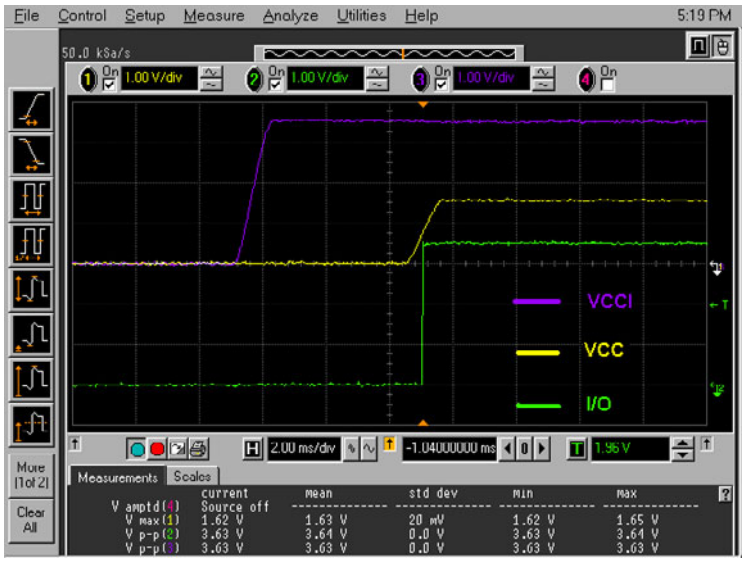

Figure 2 • **I/O State When V_{CCI} is Powered Before V_{CC}**

Power-Up to Functional Time

At power-up, device I/Os exit the tristate mode and become functional once the last voltage supply in the power-up sequence (V_{CCI} or V_{CC}) reaches its functional activation level. Typical I/O behavior during power-up to functional time is illustrated in Figure 1 on page 2 and Figure 2 on page 2.

The functional level of the voltage supplies at power-up is designed to be 0.85 V+/–0.25 V for V_{CC} and 0.9 V+/–0.3 V for V_{CCI} supply. Once the last voltage supply in the power-up sequence exceeds its functional level, the device I/Os will transition into a functional state. Therefore, the power-up to functional time is the time that it takes for the last supply to power-up from zero to its functional level. However, the functional level of the power supply during power-up may vary slightly within the specification in different ramp rates.

M7 ProASIC3/E devices meet Level 0 LAPU (i.e., they can be functional prior to V_{CC} reaching the regulated voltage required). This important advantage distinguishes M7 ProASIC3/E Flash devices from their SRAM-based counter parts. SRAM-based FPGAs, due to their volatile technology, require hundreds of milliseconds after power-up to configure the design bitstream before they become functional. Refer to Figure 3 for more information.

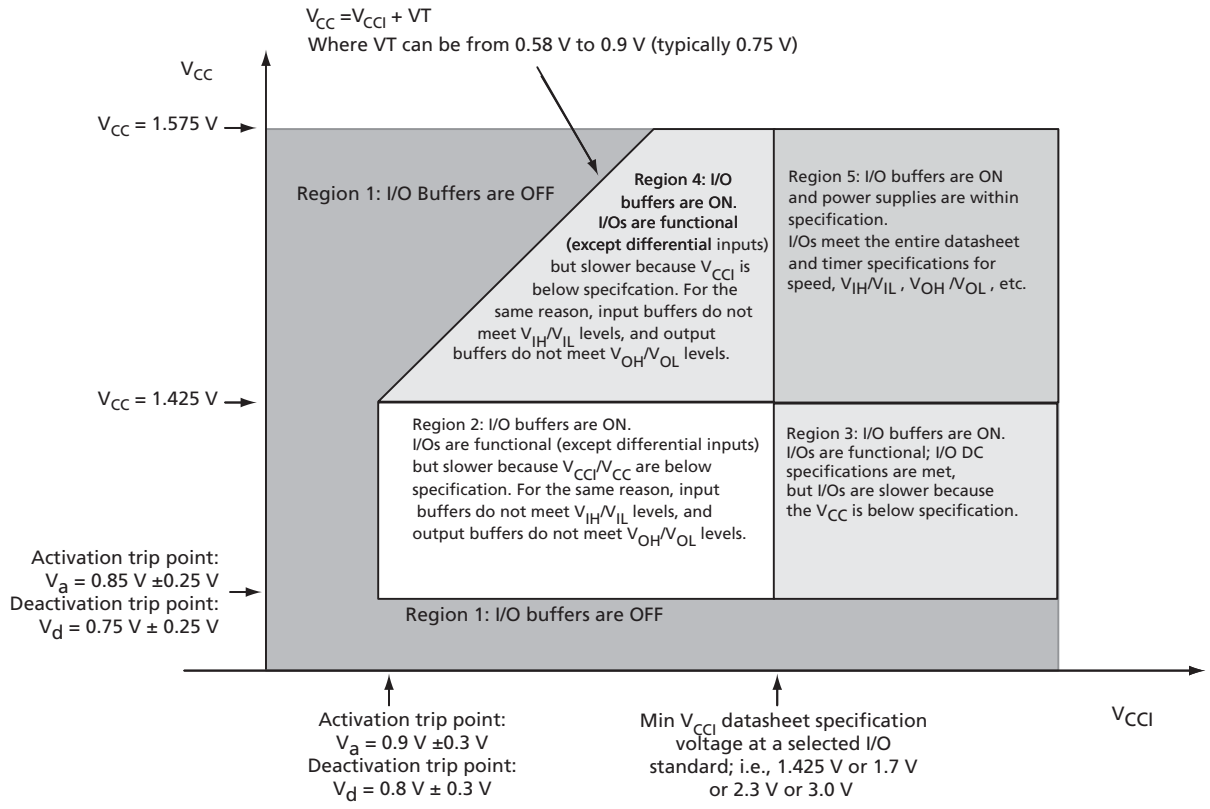

Figure 3 • **I/O State as a Function of V_{CCI} and V_{CC} Voltage Levels**

Brownout Voltage

Brownout is a condition in which the voltage supplies are lower than normal, causing the device to malfunction as a result of insufficient power. In general, Actel does not guarantee the functionality of the design inside M7 ProASIC3/E devices, if voltage supplies are below their minimum recommended operating condition. Actel has performed measurements to characterize the brownout levels of FPGA power supplies. The brownout levels of the power supplies for M7 ProASIC3/E devices are designed to be 0.75 V+/–0.25 V for V_{CC} and 0.8 V+/-0.3 V for V_{CCI}. For the purpose of characterization, a direct path from the device input to output is monitored while voltage supplies are lowered gradually. The brownout point is defined as the voltage level at which the output stops following the input. Characterization tests performed on two M7A3PE600-PQ208 EAS devices in typical operating conditions showed the brownout voltage levels to be within the specification.

During device power-down, the device I/Os become tristated once the first supply in the power-down sequence drops below its brownout deactivation voltage.

Internal Pull-Up and Pull-Down

M7 ProASIC3/E device I/Os are equipped with internal weak pull-up/down resistors that can be used by designers. If used, these internal pull-up/down resistors will be activated during power-up, once both V_{CC} and V_{CCI} are passed their functional activation level. Similarly, during power-down these internal pull-up/down resistors will turn off once the first supply voltage falls below its brownout deactivation level.

Design Theory and Implementation

Implementing the microprocessor PoR requires a few resources, a general purpose I/O pin, and a few core logic tiles. The I/O pin is configured as an input with a weak pull-down resistor and is monitored by the user-implemented logic. When the I/Os become active, the logic will see this value and begin the internal reset count as required by microprocessor core.

The dedicated I/O used for monitoring should be configured as either TTL or CMOS input without Schmitt Trigger capabilities, with an external 10 kΩ pull-down resistor. Upon a PoR, the dedicated I/O gets "reset" and does not become activated until the corresponding V_{CCI}Bx and V_{CC} reach the threshold discussed in the "Power-Up to Functional Time" section on page 3.

Once V_{CC} reaches the power-on threshold, the user logic begins sampling the state of the dedicated I/O pin, regardless of the I/O buffers being active. Prior to the dedicated I/O being powered, the internal net resides in a tristate or Hi-Z state. Once the logic is able to successfully read the pull-down state of dedicated I/O pin, the processor core reset time count begins to allow for a proper processor reset. Therefore, Actel recommends that the V_{CCI} of the dedicated I/O become powered beyond the working threshold, prior to the core V_{CC} reaching its power-on threshold level, to assure generating a proper PoR signal.

The output of the user-implemented PoR circuit should then be connected to the microprocessor's top-level reset signal, or to the input of the PoR IP block, if one is included in the design.

Conclusion

For systems that include a microprocessor without a dedicated power management chipset, the PoR signal generation described in this application brief is sufficient to prevent the execution of runaway code and other system initialization issues. However, in order for the PoR generation to work effectively, care must be given to the sequence of the powering of V_{CCI}Bx and V_{CC}. The power sequencing described in the "Design Theory and Implementation" section describes how to generate an internal PoR signal for M7 ProASIC3/E devices.

Related Documents

Datasheets

CoreMP7
http://www.actel.com/ipdocs/CoreMP7_DS.pdf
ProASIC3 Flash Family FPGAs
http://www.actel.com/documents/PA3_DS.pdf
ProASIC3E Flash Family FPGAs
http://www.actel.com/documents/PA3_DS.pdf

www.actel.com

Actel Corporation

2061 Stierlin Court
Mountain View, CA
94043-4655 USA
Phone 650.318.4200
Fax 650.318.4600

Actel Europe Ltd.

Dunlop House, Riverside Way
Camberley, Surrey GU15 3YL
United Kingdom
Phone +44 (0) 1276 401 450
Fax +44 (0) 1276 401 490

Actel Japan
www.jp.actel.com

EXOS Ebisu Bldg. 4F
1-24-14 Ebisu Shibuya-ku
Tokyo 150 Japan
Phone +81.03.3445.7671
Fax +81.03.3445.7668

Actel Hong Kong
www.actel.com.cn

Suite 2114, Two Pacific Place
88 Queensway, Admiralty
Hong Kong
Phone +852 2185 6460
Fax +852 2185 6488

51900107-0/10.05