DC and Power Characteristics

General Specifications

DC and switching characteristics for –F speed grade targets are based only on simulation.

The characteristics provided for –F speed grade are subject to change after establishing FPGA specifications. Some restrictions might be added and will be reflected in future revisions of this document. The –F speed grade is only supported in the commercial temperature range.

Operating Conditions

Stresses beyond those listed in the Table 3-1 may cause permanent damage to the device.

Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating ranges specified in Table 3-2 on page 3-2.

Table 3-1 • **Absolute Maximum Ratings**

Symbol	Parameter	Limits	Units
V_{CC}	DC core supply voltage	–0.3 to 1.65	V
V_{JTAG}	JTAG DC voltage	–0.3 to 3.75	V
V_{PUMP}	Programming voltage	–0.3 to 3.75	V
V_{CCPLL}	Analog power supply (PLL)	–0.3 to 1.65	V
V_{CCI}	DC I/O output buffer supply voltage	–0.3 to 3.75	V
VMV	DC I/O input buffer supply voltage	–0.3 to 3.75	V
VI	I/O input voltage	–0.3 V to 3.6 V (when I/O hot insertion mode is enabled) –0.3 V to (V_{CCI} + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot-insertion mode is disabled)	V
V_{CC33A}	(+3.3 V) power supply	–0.3 to 3.75	V
VAREF	Voltage reference for ADC	1.0 to 3.75	V
V_{CC15A}	Digital Power supply for the analog system	–0.3 to 1.65	V
V_{CCNVM}	Embedded Flash power supply	–0.3 to 1.65	V
V_{CCOSC}	Oscillator power supply	–0.3 to 3.75	V

Notes:

1. *Device performance is not guaranteed if storage temperature exceeds 110°C.*
2. *The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 3-3 on page 3-2.*

Table 3-2 • **Recommended Operating Conditions**

Symbol	Parameter		Commercial	Industrial	Units
T_a	Ambient temperature		0 to +70	–40 to +85	°C
V_{CC}	1.5 V DC core supply voltage		1.425 to 1.575	1.425 to 1.575	V
V_{JTAG}	JTAG DC voltage		1.4 to 3.6	1.4 to 3.6	V
V_{PUMP}	Programming voltage	Programming mode	3.0 to 3.6	3.0 to 3.6	V
		Operation[3]	0 to 3.6	0 to 3.6	V
V_{CCPLL}	Analog power supply (PLL)		1.4 to 1.6	1.4 to 1.6	V
V_{CCI} and VMV	1.5 V DC supply voltage		1.425 to 1.575	1.425 to 1.575	V
	1.8 V DC supply voltage		1.7 to 1.9	1.7 to 1.9	V
	2.5 V DC supply voltage		2.3 to 2.7	2.3 to 2.7	V
	3.3 V DC supply voltage		3.0 to 3.6	3.0 to 3.6	V
	LVDS differential I/O		2.375 to 2.625	2.375 to 2.625	V
	LVPECL differential I/O		3.0 to 3.6	3.0 to 3.6	V
V_{CC33A}	(+3.3 V) power supply		2.97 to 3.63	2.97 to 3.63	V
VAREF	Voltage reference for ADC		2.527 to 2.593	2.527 to 2.593	V
V_{CC15A}	Digital Power supply for the analog system		1.425 to 1.575	1.425 to 1.575	V
V_{CCNVM}	Embedded Flash power supply		1.425 to 1.575	1.425 to 1.575	V
V_{CCOSC}	Oscillator power supply		2.97 to 3.63	2.97 to 3.63	V

Notes:

1. *The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-72 on page 2-124. VMV and V_{CCI} should be at the same voltage within a given I/O bank.*
2. *All parameters representing voltages are measured with respect to GND unless otherwise specified.*
3. *V_{PUMP} can be left floating during normal operation (not programming mode).*

Table 3-3 • **Overshoot and Undershoot Limits (as measured on quiet I/Os)[1]**

V_{CCI} and VMV	Average V_{CCI}-GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle[2]	Maximum Overshoot/ Undershoot)[2]
2.7 V or less	10%	1.4 V
	5%	1.49 V
3.0 V	10%	1.1 V
	5%	1.19 V
3.3 V	10%	0.79 V
	5%	0.88 V
3.6 V	10%	0.45 V
	5%	0.54 V

Notes:

1. *Based on reliability requirements at 85°C.*
2. *The duration is allowed at one cycle out of six clock cycles (estimated SSO density over cycles). If the overshoot/undershoot occurs at 1 out of 2 cycles, then the maximum overshoot/undershoot has to be reduced by 0.15 V.*

Table 3-4 • **FPGA Programming, Storage, and Operating Limits**

Product Grade	Programming Cycles	Program Retention	Storage Temperature		Maximum Operating Junction Temperature T_J (°C)
			Min.	Max.	
Commercial	500	20 years	0	110	110
Industrial	500	20 years	–40	110	110

Note: *This is a stress rating only. Functional operation at any other condition other than those indicated is not implied.*

I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every Fusion device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power-up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in Figure 3-1.

There are five regions to consider during power-up.

Fusion I/Os are activated only if ALL of the following three conditions are met:

1. V_{CC} and V_{CCI} are above the minimum specified trip points (Figure 3-1).
2. $V_{CCI} > V_{CC} – 0.75$ V (Typical).
3. Chip is in the operating mode.

V_{CCI} Trip Point:
Ramping up: 0.6 V < trip_point_up < 1.2 V

Ramping down: 0.5 V < trip_point_down < 1.1 V

V_{CC} Trip Point:
Ramping up: 0.6 V < trip_point_up < 1.1 V

Ramping down: 0.5 V < trip_point_down < 1 V

V_{CC} and V_{CCI} ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to V_{CCI}.
- JTAG supply, PLL power supplies, and charge pump V_{PUMP} supply have no influence on I/O behavior.

Internal Power-Up Activation Sequence

1. Core
2. Input buffers
3. Output buffers, after 200 ns delay from input buffer activation.

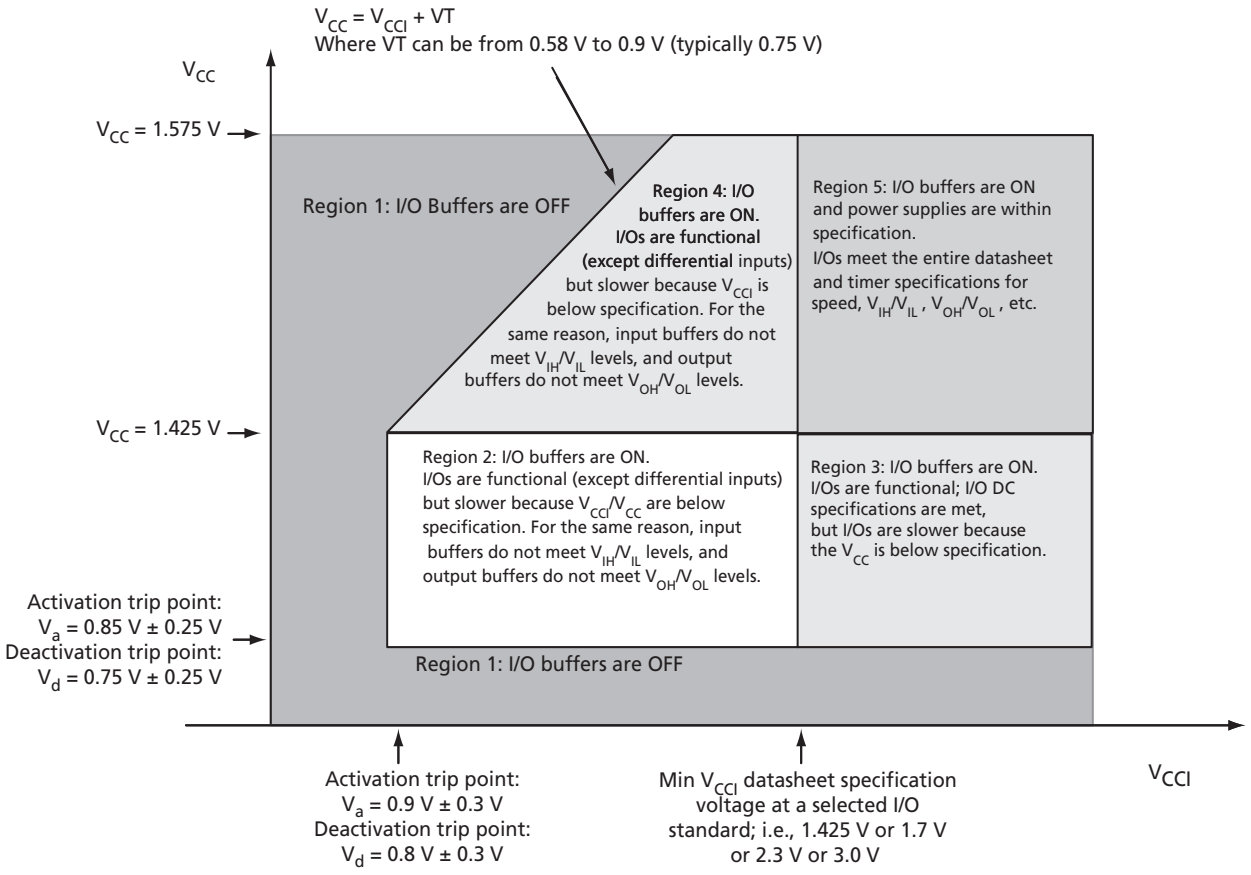

Figure 3-1 • **I/O State as a Function of V_{CCI} and V_{CC} Voltage Levels**

Thermal Characteristics

Introduction

The temperature variable in the Actel Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption will cause the chip's junction temperature to be higher than the ambient, case, or board temperatures. EQ 3-1 and EQ 3-3 give the relationship between thermal resistance, temperature gradient, and power.

$$\theta_{JA} = \frac{T_J - \theta_A}{P} \qquad \textit{EQ 3-1}$$

$$\theta_{JB} = \frac{T_J - T_B}{P} \qquad \textit{EQ 3-2}$$

$$\theta_{JC} = \frac{T_J - T_C}{P} \qquad \textit{EQ 3-3}$$

where:

θ_{JA} = Junction-to-air thermal resistance

θ_{JB} = Junction-to-board thermal resistance

θ_{JC} = Junction-to-case thermal resistance

T_J = Junction temperature

T_A = Ambient temperature

T_B = Board temperature (measured 1.0 mm away from the package edge)

T_C = Case temperature

P = Total power dissipated by the device

Table 3-5 • **Package Thermal Resistance**

Product	θ_{JA}			θ_{JC}	θ_{JB}	Units
	Still Air	1.0 m/s	2.5 m/s			
AFS090-QN108	TBD	TBD	TBD	TBD	TBD	°C/W
AFS090-QN180	TBD	TBD	TBD	TBD	TBD	°C/W
AFS250-QN180	TBD	TBD	TBD	TBD	TBD	°C/W
AFS250-PQ208	TBD	TBD	TBD	TBD	TBD	°C/W
AFS600-PQ208	TBD	TBD	TBD	TBD	TBD	°C/W
AFS090-FG256	TBD	TBD	TBD	TBD	TBD	°C/W
AFS250-FG256	TBD	TBD	TBD	TBD	TBD	°C/W
AFS600-FG256	36.86	25.11	22.62	5.80	16.40	°C/W
AFS1500-FG256	TBD	TBD	TBD	TBD	TBD	°C/W
AFS600-FG484	30.67	19.00	17.00	8.28	10.87	°C/W
AFS1500-FG484	TBD	TBD	TBD	TBD	TBD	°C/W
AFS1500-FG676	TBD	TBD	TBD	TBD	TBD	°C/W

Theta-JA

Junction-to-ambient thermal resistance (θ_{JA}) is determined under standard conditions specified by JEDEC (JESD-51), but it has little relevance in actual performance of the product. It should be used with caution but is useful for comparing the thermal performance of one package to another.

A sample calculation showing the maximum power dissipation allowed for the AFS600-FG484 package under forced convection of 1.0 m/s and 75°C ambient temperature is as follows:

$$\text{Maximum Power Allowed} = \frac{T_{J(MAX)} - T_{A(MAX)}}{\theta_{JA}}$$

EQ 3-4

where:

θ_{JA} = 19.00°C/W (taken from Table 3-5 on page 3-4).
T_A = 75.00°C

$$\text{Maximum Power Allowed} = \frac{110.00°C - 75.00°C}{19.00°C/W} = 1.84\ W$$

The power consumption of a device can be calculated using the Actel power calculator. The device's power consumption must be lower than the calculated maximum power dissipation by the package. If the power consumption is higher than the device's maximum allowable power dissipation, then a heat sink can be attached on top of the case or the airflow inside the system must be increased.

Theta-JB

Junction-to-board thermal resistance (θ_{JB}) measures the ability of the package to dissipate heat from the surface of the chip to the printed circuit board. As defined by the JEDEC (JESD-51) standard, the thermal resistance from junction to board uses an isothermal ring cold plate zone concept. The ring cold plate is simply a means to generate an isothermal boundary condition at the perimeter. The cold plate is mounted on a JEDEC standard board with a minimum distance of 5.0 mm away from the package edge.

Theta-JC

Junction-to-case thermal resistance (θ_{JC}) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable for packages used with external heat sinks. Constant temperature is applied to the surface in consideration and acts as a boundary condition. This only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration.

Calculation for Heat Sink

For example, in a design implemented in an AFS600-FG484 package with 2.5 m/s airflow, the power consumption value using the power calculator is 3.00 W. The user-dependent T_a and T_j are given as follows:

T_J = 110.00°C
T_A = 70.00°C

From the datasheet:

θ_{JA} = 17.00°C/W
θ_{JC} = 8.28°C/W

$$P = \frac{T_J - T_A}{\theta_{JA}} = \frac{110°C - 70°C}{17.00\ W} = 2.35\ W$$

EQ 3-5

The 2.35 W power is less than the required 3.00 W. The design therefore requires a heat sink, or the airflow where the device is mounted should be increased. The design's total junction-to-air thermal resistance requirement can be estimated by EQ 3-6:

$$\theta_{ja(total)} = \frac{T_J - T_A}{P} = \frac{110°C - 70°C}{3.00\ W} = 13.33°C/W$$

EQ 3-6

Determining the heat sink's thermal performance:

$$\theta_{JA(TOTAL)} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

EQ 3-7

where:

θ_{JA} = 0.37 °C/W
= Thermal resistance of the interface material between the case and the heat sink, usually provided by the thermal interface manufacturer
θ_{SA} = Thermal resistance of the heat sink in °C/W

$$\theta_{SA} = \theta_{JA(TOTAL)} - \theta_{JC} - \theta_{CS}$$

EQ 3-8

$$\theta_{SA} = 13.33°C/W - 8.28°C/W - 0.37°C/W = 5.01°C/W$$

A heat sink with a thermal resistance of 5.01°C/W or better should be used. Thermal resistance of heat sinks is a function of airflow. The heat sink performance can be significantly improved with increased airflow.

Carefully estimating thermal resistance is important in the long-term reliability of an Actel FPGA. Design engineers should always correlate the power consumption of the device with the maximum allowable power dissipation of the package selected for that device.

Note: The junction-to-air and junction-to-board thermal resistances are based on JEDEC standard (JESD-51) and assumptions made in building the model. It may not be realized in actual application and therefore should be used with a degree of caution. Junction-to-case thermal resistance assumes that all power is dissipated through the case.

Temperature and Voltage Derating Factors

Table 3-6 • **Temperature and Voltage Derating Factors for Timing Delays (Normalized to T_J = 70°C, V_{CC} = 1.425 V)**

Array Voltage V_{CC} (V)	Junction Temperature (°C)					
	–40°C	0°C	25°C	70°C	85°C	100°C
1.425	0.88	0.93	0.95	1.00	1.02	1.05
1.500	0.83	0.88	0.90	0.95	0.96	0.99
1.575	0.80	0.85	0.86	0.91	0.93	0.96

Calculating Power Dissipation

Quiescent Supply Current

Table 3-7 • **Quiescent Supply Current Characteristics (I_{DDQ})[1]**

Parameter	Conditions and Modes	AFS600	AFS250	AFS090
	Maximum in operating mode (85°C) [2]	45 mA	30 mA	15 mA
	Maximum in operating mode (70°C) [2]	30 mA	20 mA	10 mA
I_{DC1}	Typical in operating mode (25°C) [2]	5 mA	3 mA	2 mA
I_{DC2}	Typical in sleep mode (25°C) [3]	200 µA	200 µA	200 µA
I_{DC3}	Typical in standby mode (25°C) [4]	10 µA	10 µA	10 µA

Notes:

1. *–F speed grade devices may experience higher Quiescent Supply current of up to five times the standard I_{DD} and higher I/O leakage.*
2. *I_{DC1} includes V_{CC}, V_{PUMP}, V_{CCI}, and VMV currents. Values do not include I/O static contribution, which is shown in Table 3-8 on page 3-7 and Table 3-9 on page 3-8.*
3. *I_{DC2} represents the current from the V_{CC33A} supply when the RTC (and the crystal oscillator) is ON, the FPGA is OFF, and voltage regulator is OFF.*
4. *I_{DC3} represents the current from the V_{CC33A} supply when the RTC (and the crystal oscillator), the FPGA, and the voltage regulator are OFF.*

Power Per I/O Pin

Table 3-8 • **Summary of I/O Input Buffer Power (Per Pin) – Default I/O Software Settings[1, 2]**

	VMV (V)	Static Power P_{DC7} (mW)[3]	Dynamic Power P_{AC9} (µW/MHz)[4]
Single-Ended			
3.3 V LVTTL/LVCMOS	3.3	–	17.39
3.3 V LVTTL/LVCMOS – Schmitt trigger	3.3	–	25.51
2.5 V LVCMOS	2.5	–	5.76
2.5 V LVCMOS – Schmitt trigger	2.5	–	7.16
1.8 V LVCMOS	1.8	–	2.72
1.8 V LVCMOS – Schmitt trigger	1.8	–	2.80
1.5 V LVCMOS (JESD8-11)	1.5	–	2.08
1.5 V LVCMOS (JESD8-11) – Schmitt trigger	1.5	–	2.00
3.3 V PCI	3.3	–	18.82
3.3 V PCI – Schmitt trigger	3.3	–	20.12
3.3 V PCI-X	3.3	–	18.82
3.3 V PCI-X – Schmitt trigger	3.3	–	20.12
Voltage-Referenced			
3.3 V GTL	3.3	2.90	8.23
2.5 V GTL	2.5	2.13	4.78
3.3 V GTL +	3.3	2.81	4.14
2.5 V GTL +	2.5	2.57	3.71
HSTL (I)	1.5	0.17	2.03
HSTL (II)	1.5	0.17	2.03
SSTL2 (I)	2.5	1.38	4.48
SSTL2 (II)	2.5	1.38	4.48
SSTL3 (I)	3.3	3.21	9.26
SSTL3 (II)	3.3	3.21	9.26
Differential			
LVDS, BLVDS, M-LVDS	2.5	2.26	1.50
LVPECL	3.3	5.71	2.17

Notes:

1. *Input buffer power values provided in this table correspond to Pro I/Os. Pins assigned to east and west peripheries may have slightly lower power characteristics.*
2. *For a different pin location, Actel recommends using the Actel power calculator or SmartPower in Actel Libero IDE software.*
3. *P_{DC7} is the static power (where applicable) measured on VMV.*
4. *P_{AC9} is the total dynamic power measured on V_{CC} and VMV.*

Table 3-9 • **Summary of I/O Output Buffer Power (Per Pin)—Default I/O Software Settings[1, 2, 3]**

	C_{LOAD} (pF)	V_{CCI} (V)	Static Power P_{DC8} (mW)[4]	Dynamic Power P_{AC10} (µW/MHz)[5]
Single-Ended				
3.3 V LVTTL/LVCMOS	35	3.3	–	474.70
2.5 V LVCMOS	35	2.5	–	270.73
1.8 V LVCMOS	35	1.8	–	151.78
1.5 V LVCMOS (JESD8-11)	35	1.5	–	104.55
3.3 V PCI	10	3.3	–	204.61
3.3 V PCI-X	10	3.3	–	204.61
Voltage-Referenced				
3.3 V GTL	10	3.3	–	24.08
2.5 V GTL	10	2.5	–	13.52
3.3 V GTL+	10	3.3	–	24.10
2.5 V GTL+	10	2.5	–	13.54
HSTL (I)	20	1.5	7.08	26.22
HSTL (II)	20	1.5	13.88	27.22
SSTL2 (I)	30	2.5	16.69	105.56
SSTL2 (II)	30	2.5	25.91	116.60
SSTL3 (I)	30	3.3	26.02	114.87
SSTL3 (II)	30	3.3	42.21	131.76
Differential				
LVDS, BLVDS, M-LVDS	–	2.5	7.70	89.62
LVPECL	–	3.3	19.42	168.02

Notes:

1. *Dynamic power consumption is given for standard load and software default drive strength and output slew.*
2. *Output buffer power values provided in this table correspond to Pro I/Os. Output buffers assigned to east and west peripheries may have slightly lower power characteristics.*
3. *For a different pin location, output load, drive strength, or slew rate, Actel recommends using the Actel power calculator or SmartPower in Actel Libero IDE software.*
4. *P_{DC8} is the static power (where applicable) measured on V_{CCI}.*
5. *P_{AC10} is the total dynamic power measured on V_{CC} and V_{CCI}.*

Dynamic Power Consumption of Various Internal Resources

Table 3-10 • **Different Components Contributing to the Dynamic Power Consumption in Fusion Devices**

Parameter	Definition	Power Supply		Device-Specific Dynamic Contributions			Units
		Name	Setting	AFS600	AFS250	AFS090	
P_{AC1}	Clock contribution of a Global Rib	V_{CC}	1.5 V	12.8	12.8	12.8	µW/MHz
P_{AC2}	Clock contribution of a Global Spine	V_{CC}	1.5 V	1.9	1.9	1.9	µW/MHz
P_{AC3}	Clock contribution of a VersaTile row	V_{CC}	1.5 V	0.81	0.81	0.81	µW/MHz
P_{AC4}	Clock contribution of a VersaTile used as a sequential module	V_{CC}	1.5 V	0.11	0.11	0.11	µW/MHz
P_{AC5}	First contribution of a VersaTile used as a sequential module	V_{CC}	1.5 V	0.07	0.07	0.07	µW/MHz
P_{AC6}	Second contribution of a VersaTile used as a sequential module	V_{CC}	1.5 V	0.29	0.29	0.29	µW/MHz
P_{AC7}	Contribution of a VersaTile used as a combinatorial module	V_{CC}	1.5 V	0.29	0.29	0.29	µW/MHz
P_{AC8}	Average contribution of a routing net	V_{CC}	1.5 V	0.70	0.70	0.70	µW/MHz
P_{AC9}	Contribution of an I/O input pin (standard dependent)	VMV/ V_{CC}	See Table 3-8 on page 3-7				
P_{AC10}	Contribution of an I/O output pin (standard dependent)	V_{CCI}/V_{CC}	See Table 3-9 on page 3-8				
P_{AC11}	Average contribution of a RAM block during a read operation	V_{CC}	1.5 V	25.00	25.00	25.00	µW/MHz
P_{AC12}	Average contribution of a RAM block during a write operation	V_{CC}	1.5 V	30.00	30.00	30.00	µW/MHz
P_{AC13}	First contribution of a PLL	V_{CC}	1.5 V	4.00	4.00	4.00	µW/MHz
P_{AC14}	Second contribution of a PLL	V_{CC}	1.5 V	2.00	2.00	2.00	µW/MHz
P_{AC15}	Contribution of NVM block during a read operation (F < 33MHz)	V_{CC}	1.5 V	358.00	358.00	358.00	µW/MHz
P_{AC16}	1st contribution of NVM block during a read operation (F > 33MHz)	V_{CC}	1.5 V	12.88	12.88	12.88	mW
P_{AC17}	2nd contribution of NVM block during a read operation (F > 33MHz)	V_{CC}	1.5 V	4.80	4.80	4.80	µW/MHz
P_{AC18}	Crystal Oscillator contribution	V_{CC33A}	3.3 V	0.63	0.63	0.63	mW
P_{AC19}	RC Oscillator contribution	V_{CC33A}	3.3 V	3.30	3.30	3.30	mW
P_{AC20}	Analog Block dynamic power contribution of ADC	V_{CC}	1.5 V	3.00	3.00	3.00	mW

Static Power Consumption of Various Internal Resources

Table 3-11 • **Different Components Contributing to the Static Power Consumption in Fusion Devices**

Parameter	Definition	Power Supply		Device-Specific Static Contributions			Units
		Name	Setting	AFS600	AFS250	AFS090	
P_{DC1}	Core static power contribution in operating mode	V_{CC}	1.5 V	7.50	4.50	3.00	mW
P_{DC2}	Device static power contribution in sleep mode	V_{CC33A}	3.3 V	0.03	0.03	0.03	mW
P_{DC3}	Device static power contribution in standby mode	V_{CC33A}	3.3 V	0.03	0.03	0.03	mW
P_{DC4}	NVM static power contribution	V_{CC}	1.5 V	1.19	1.19	1.19	mW
P_{DC5}	Analog Block static power contribution of ADC	V_{CC33A}	3.3 V	8.25	8.25	8.25	mW
P_{DC6}	Analog Block static power contribution per Quad	V_{CC33A}	3.3 V	3.30	3.30	3.30	mW
P_{DC7}	Static contribution per input pin – standard dependent contribution	VMV/ V_{CC}	See Table 3-8 on page 3-7				
P_{DC8}	Static contribution per input pin – standard dependent contribution	VMV/ V_{CC}	See Table 3-9 on page 3-8				

Power Calculation Methodology

The section below describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in the Libero IDE software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- The number of NVM blocks used in the design
- The number of Analog quads used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 3-12 on page 3-15
- Enable rates of output buffers—guidelines are provided for typical applications in Table 3-13 on page 3-15
- Read rate and write rate to the RAM—guidelines are provided for typical applications in Table 3-13 on page 3-15.
- Read rate to the NVM blocks

The calculation should be repeated for each clock domain defined in the design.

Methodology

Total Power Consumption—P_{TOTAL}

Operating Mode, Sleep Mode, and Standby Mode

$P_{TOTAL} = P_{STAT} + P_{DYN}$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

Total Static Power Consumption—P_{STAT}

Operating Mode

$P_{STAT} = P_{DC1} + (N_{NVM\text{-}BLOCKS} * P_{DC4}) + P_{DC5} + (N_{QUADS} * P_{DC6}) + (N_{INPUTS} * P_{DC7}) + (N_{OUTPUTS} * P_{DC8})$

$N_{NVM\text{-}BLOCKS}$ is the number of NVM blocks available in the device.

N_{QUADS} is the number of Analog Quads used in the design.

N_{INPUTS} is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

Sleep Mode

$P_{STAT} = P_{DC2}$

Standby Mode

$P_{STAT} = P_{DC3}$

Total Dynamic Power Consumption—P_{DYN}

Operating Mode

$P_{DYN} = P_{CLOCK} + P_{S\text{-}CELL} + P_{C\text{-}CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL} + P_{NVM} + P_{XTL\text{-}OSC} + P_{RC\text{-}OSC} + P_{AB}$

Sleep Mode

$P_{DYN} = P_{XTL\text{-}OSC}$

Standby Mode

$P_{DYN} = 0$ W

Global Clock Dynamic Contribution—P_{CLOCK}

Operating Mode

$P_{CLOCK} = (P_{AC1} + N_{SPINE} * P_{AC2} + N_{ROW} * PAC3 + N_{S\text{-}CELL} * P_{AC4}) * F_{CLK}$

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in Table 3-12 on page 3-15.

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in Table 3-12 on page 3-15.

F_{CLK} is the global clock signal frequency.

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

Sleep Mode and Standby Mode

$P_{CLOCK} = 0$ W

Sequential Cells Dynamic Contribution—$P_{S\text{-}CELL}$

Operating Mode

$P_{S\text{-}CELL} = N_{S\text{-}CELL} * (P_{AC5} + (\alpha_1 / 2) * P_{AC6}) * F_{CLK}$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 3-12 on page 3-15.

F_{CLK} is the global clock signal frequency.

Sleep Mode and Standby Mode

$P_{S\text{-}CELL} = 0$ W

Combinational Cells Dynamic Contribution—$P_{C\text{-}CELL}$

Operating Mode

$P_{C\text{-}CELL} = N_{C\text{-}CELL} * (\alpha_1 / 2) * P_{AC7} * F_{CLK}$

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 3-12 on page 3-15.

F_{CLK} is the global clock signal frequency.

Sleep Mode and Standby Mode

$P_{C\text{-}CELL} = 0$ W

Routing Net Dynamic Contribution—P_{NET}

Operating Mode

$P_{NET} = (N_{S\text{-}CELL} + N_{C\text{-}CELL}) * (\alpha_1 / 2) * P_{AC8} * F_{CLK}$

$N_{S\text{-}CELL}$ is the number VersaTiles used as sequential modules in the design.

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 3-12 on page 3-15.

F_{CLK} is the global clock signal frequency.

Sleep Mode and Standby Mode

$P_{NET} = 0$ W

I/O Input Buffer Dynamic Contribution-P_{INPUTS}

Operating Mode

$P_{INPUTS} = N_{INPUTS} * (\alpha_2 / 2) * P_{AC9} * F_{CLK}$

N_{INPUTS} is the number of I/O input buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 3-12 on page 3-15.

F_{CLK} is the global clock signal frequency.

Sleep Mode and Standby Mode

$P_{INPUTS} = 0$ W

I/O Output Buffer Dynamic Contribution—$P_{OUTPUTS}$

Operating Mode

$P_{OUTPUTS} = N_{OUTPUTS} * (\alpha_2 / 2) * \beta_1 * P_{AC10} * F_{CLK}$

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 3-12 on page 3-15.

β_1 is the I/O buffer enable rate—guidelines are provided in Table 3-13 on page 3-15.

F_{CLK} is the global clock signal frequency.

Sleep Mode and Standby Mode

$P_{OUTPUTS} = 0$ W

RAM Dynamic Contribution—P_{MEMORY}

Operating Mode

$P_{MEMORY} = (NBLOCKS * P_{AC11} * \beta_2 * F_{READ\text{-}CLOCK}) + (NBLOCK * P_{AC12} * \beta_3 * F_{WRITE\text{-}CLOCK})$

NBLOCKS is the number of RAM blocks used in the design.

$F_{READ\text{-}CLOCK}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations—guidelines are provided in Table 3-13 on page 3-15.

β_3 the RAM enable rate for write operations—guidelines are provided in Table 3-13 on page 3-15.

$F_{WRITE\text{-}CLOCK}$ is the memory write clock frequency.

Sleep Mode and Standby Mode

$P_{MEMORY} = 0$ W

PLL/CCC Dynamic Contribution—P_{PLL}

Operating Mode

$P_{PLL} = P_{AC13} * F_{CLKIN} + \Sigma (P_{AC14} * F_{CLKOUT})$

F_{CLKIN} is the input clock frequency.

F_{CLKOUT} is the output clock frequency.[1]

Sleep Mode and Standby Mode

$P_{PLL} = 0$ W

1. *The PLL dynamic contribution depends on the input clock frequency, the number of output clock signals generated by the PLL, and the frequency of each output clock. If a PLL is used to generate more than one output clock, include each output clock in the formula output clock by adding its corresponding contribution (P_{AC14} * F_{CLKOUT} product) to the total PLL contribution.*

Nonvolatile Memory Dynamic Contribution—P_{NVM}

Operating Mode

The NVM dynamic power consumption is a piece-wise linear function of frequency.

$P_{NVM} = N_{NVM\text{-}BLOCKS} * \beta_4 * P_{AC15} * F_{READ\text{-}NVM}$ when $F_{READ\text{-}NVM} \le 33$ MHz,

$P_{NVM} = N_{NVM\text{-}BLOCKS} * \beta_4 * (P_{AC16} + P_{AC17} * F_{READ\text{-}NVM})$ when $F_{READ\text{-}NVM} > 33$ MHz

$N_{NVM\text{-}BLOCKS}$ is the number of NVM blocks used in the design (2 in AFS600)

β_4 is the NVM enable rate for read operations. Default is 0 (NVM mainly in idle state)

$F_{READ\text{-}NVM}$ is the NVM read-clock frequency

Sleep Mode and Standby Mode

$P_{NVM} = 0$ W

Crystal Oscillator Dynamic Contribution—$P_{XTL\text{-}OSC}$

Operating Mode

$P_{XTL\text{-}OSC} = P_{AC18}$

Sleep Mode

$P_{XTL\text{-}OSC} = P_{AC18}$

Standby Mode

$P_{XTL\text{-}OSC} = 0$ W

RC Oscillator Dynamic Contribution—$P_{RC\text{-}OSC}$

Operating Mode

$P_{RC\text{-}OSC} = P_{AC19}$

Sleep Mode and Standby Mode

$P_{RC\text{-}OSC} = 0$ W

Analog System Dynamic Contribution—P_{AB}

Operating Mode

$P_{AB} = P_{AC20}$

Sleep Mode and Standby Mode

$P_{AB} = 0$ W

Guidelines

Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that this net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100% as all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
  - Bit 0 (LSB) = 100%
  - Bit 1 = 50%
  - Bit 2 = 25%
  - …
  - Bit 7 (MSB) = 0.78125%
  - The average toggle rate is = (100% + 50% + 25% + 12.5% + . . . 0.78125%) / 8.

Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When nontristate output buffers are used, the enable rate should be 100%.

Table 3-12 • **Toggle Rate Guidelines Recommended for Power Calculation**

Component	Definition	Guideline
α_1	Toggle rate of VersaTile outputs	10%
α_2	I/O buffer toggle rate	10%

Table 3-13 • **Enable Rate Guidelines Recommended for Power Calculation**

Component	Definition	Guideline
β_1	I/O output buffer enable rate	100%
β_2	RAM enable rate for read operations	12.5%
β_3	RAM enable rate for write operations	12.5%
β_4	NVM enable rate for read operations	0%

Example of Power Calculation

This example considers a shift register with 5,000 storage tiles including a counter and memory that stores analog information. The shift register is clocked at 50 MHz and stores and reads information from a RAM.

The device used is a commercial AFS600 device operating in typical conditions.

The calculation below uses the power calculation methodology previously presented and shows how to determine the dynamic and static power consumption of resources used in the application.

Also included in the example is the calculation of power consumption in operating, sleep, and standby modes to illustrate the benefit of power-saving modes.

Global Clock Contribution—P_{CLOCK}

F_{CLK} = 50 MHz

Number of Sequential VersaTiles: $N_{S\text{-}CELL}$ = 5,000

Estimated number of Spines: N_{SPINES} = 5

Estimated number of Rows: N_{ROW} = 313

Operating Mode

$P_{CLOCK} = (P_{AC1} + N_{SPINE} * P_{AC2} + N_{ROW} * PAC3 + N_{S\text{-}CELL} * P_{AC4}) * F_{CLK}$

$P_{CLOCK} = (0.0128 + 5*0.0019 + 313*0.00081 + 5{,}000*0.00011)*50$

P_{CLOCK} = 41.28 mW

Sleep Mode and Standby Mode

P_{CLOCK} = 0 W

Logic – Sequential Cells, Combinational Cells, and Routing Net Contributions—$P_{S\text{-}CELL}$, $P_{C\text{-}CELL}$, and P_{NET}

F_{CLK} = 50 MHz

Number of Sequential VersaTiles: $N_{S\text{-}CELL}$ = 5,000

Number of Combinational VersaTiles: $N_{C\text{-}CELL}$ = 6,000

Estimated Toggle rate of VersaTile outputs: α_1 = 0.1 (10%)

Operating Mode

$P_{S\text{-}CELL} = N_{S\text{-}CELL} * (P_{AC5} + (\alpha_1 / 2) * P_{AC6}) * F_{CLK}$

$P_{S\text{-}CELL} = 5{,}000*(0.00007 + (0.1/2)*0.00029) * 50$

$P_{S\text{-}CELL}$ = 21.13 mW

$P_{C\text{-}CELL} = N_{C\text{-}CELL} * (\alpha_1 / 2) * P_{AC7} * F_{CLK}$

$P_{C\text{-}CELL} = 6{,}000 * (0.1/2) * 0.00029 * 50$

$P_{C\text{-}CELL}$ = 4.35 mW

$P_{NET} = (N_{S\text{-}CELL} + N_{C\text{-}CELL}) * (\alpha_1 / 2) * P_{AC8} * F_{CLK}$

$P_{NET} = (5{,}000+6{,}000) * (0.1/2) * 0.0007 * 50$

P_{NET} = 19.25 mW

PLOGIC = $P_{S\text{-}CELL} + P_{C\text{-}CELL} + P_{NET}$

PLOGIC = 21.13 mW + 4.35m W + 19.25 mW

PLOGIC = 44.73 mW

Sleep Mode and Standby Mode

$P_{S\text{-}CELL}$ = 0 W

$P_{C\text{-}CELL}$ = 0 W

P_{NET} = 0 W

PLOGIC = 0 W

I/O Input and Output Buffer Contribution—$P_{I/O}$

This example uses LVTTL 3.3 V I/O cells. The output buffers are 12 mA capable configured with high output slew and are driving a 35 pF output load.

F_{CLK} = 50 MHz

Number of input pin used: N_{INPUTS} = 30

Number of output pins used: $N_{OUTPUTS}$ = 40

Estimated I/O buffer toggle rate: α_2 = 0.1 (10%)

Estimated IO buffer enable rate: β_1 = 1 (100%)

Operating Mode

$P_{INPUTS} = N_{INPUTS} * (\alpha_2 /2) * P_{AC9} * F_{CLK}$

$P_{INPUTS} = 30 * (0.1/2) * 0.01739 * 50$

P_{INPUTS} = 1.30 mW

$P_{OUTPUTS} = N_{OUTPUTS} * (\alpha_2 /2) * \beta_1 * P_{AC10} * F_{CLK}$

$P_{OUTPUTS} = 40 * (0.1/2) * 1 * 0.4747 * 50$

$P_{OUTPUTS}$ = 47.47 mW

$PIO = P_{INPUTS} + P_{OUTPUTS}$

PIO = 1.30 mW + 47.47 mW

PIO = 48.77 mW

Sleep Mode and Standby Mode

P_{INPUTS} = 0 W

$P_{OUTPUTS}$ = 0 W

$P_{I/O}$ = 0 W

RAM Contribution—P_{MEMORY}

Frequency of Read-Clock: $F_{READ\text{-}CLOCK}$ = 10 MHz

Frequency of Write-Clock: $F_{WRITE\text{-}CLOCK}$ = 10 MHz

Number of Ram Blocks: NBLOCKS = 20

Estimated RAM Read Enable Rate: β_2 = 0.125 (12.5%)

Estimated RAM Write Enable Rate: β_3 = 0.125 (12.5%)

Operating Mode

$P_{MEMORY} = (NBLOCKS * P_{AC11} * \beta_2 * F_{READ\text{-}CLOCK}) + (NBLOCK * P_{AC12} * \beta_3 * F_{WRITE\text{-}CLOCK})$

$P_{MEMORY} =(20 * 0.025 * 0.125 * 10) + (20 * 0.030 * 0.125 * 10)$

P_{MEMORY} = 1.38 mW

Sleep Mode and Standby Mode

P_{MEMORY} = 0 W

PLL/CCC Contribution—P_{PLL}

PLL is not used in this application.

P_{PLL} = 0 W

Nonvolatile Memory—P_{NVM}

Nonvolatile memory is not used in this application.

P_{NVM} = 0 W

Crystal Oscillator—$P_{XTL-OSC}$

The application utilizes sleep mode. The crystal oscillator is assumed to be active.

Operating Mode

$P_{XTL-OSC} = P_{AC18}$

$P_{XTL-OSC}$ = 0.63 mW

Sleep Mode

$P_{XTL-OSC} = P_{AC18}$

$P_{XTL-OSC}$ = 0.63 mW

Standby Mode

$P_{XTL-OSC}$ = 0 W

RC Oscillator—P_{RC-OSC}

Operating Mode

$P_{RC-OSC} = P_{AC19}$

P_{RC-OSC} = 3.30 mW

Sleep Mode and Standby Mode

P_{RC-OSC} = 0 W

Analog System—P_{AB}

Number of Quads used: N_{QUADS} = 4

Operating Mode

$P_{AB} = P_{AC20}$

P_{AB} = 3.00 mW

Sleep Mode and Standby Mode

P_{AB} = 0 W

Total Dynamic Power Consumption—P_{DYN}

Operating Mode

P_{DYN} = PCLOCK + P_{S-CELL} + P_{C-CELL} + P_{NET} + P_{INPUTS} + $P_{OUTPUTS}$ + P_{MEMORY} + P_{PLL} + P_{NVM}+ $P_{XTL-OSC}$ + P_{RC-OSC} + P_{AB}

P_{DYN} = 41.28 mW + 21.1 mW + 4.35 mW + 19.25 mW + 1.30 mW + 47.47 mW + 1.38 mW + 0 + 0 + 0.63 mW + 3.30 mW + 3.00 mW

P_{DYN} = 143.06 mW

Sleep Mode

$P_{DYN} = P_{XTL-OSC}$

P_{DYN} = 0.63 mW

Standby Mode

P_{DYN} =0 W

Total Static Power Consumption—P_{STAT}

Number of Quads used: N_{QUADS} = 4

Number of NVM blocks available AFS600: $N_{NVM-BLOCKS}$ = 2

Number of Input pins used: N_{INPUTS} = 30

Number of Output pins used: $N_{OUTPUTS}$ = 40

Operating Mode

$P_{STAT} = P_{DC1} + (N_{NVM-BLOCKS} * P_{DC4}) + P_{DC5} + (N_{QUADS} * P_{DC6}) + (N_{INPUTS} * P_{DC7}) + (N_{OUTPUTS} * P_{DC8})$

P_{STAT} = 7.50 mW + (2 * 1.19 mW) + 8.25 mW + (4 * 3.30 mW) + (30 * 0.00) + (40 * 0.00)

P_{STAT} = 31.33 mW

Sleep Mode

$P_{STAT} = P_{DC2}$

P_{STAT} = 0.03 mW

Standby Mode

$P_{STAT} = P_{DC3}$

P_{STAT} = 0.03 mW

Total Power Consumption—P_{TOTAL}

In operating mode, the total power consumption of the device is 174.39 mW:

$P_{TOTAL} = P_{STAT} + P_{DYN}$

P_{TOTAL} = 143.06 mW + 31.33 mW

P_{TOTAL} = 174.39 mW

In sleep mode, the total power consumption of the device is limited to 0.66 mW:

$P_{TOTAL} = P_{STAT} + P_{DYN}$

P_{TOTAL} = 0.03 mW + 0.63 mW

P_{TOTAL} = 0.66 mW

In Standby mode, the total power consumption of the device drops as low as 0.03 mW:

$P_{TOTAL} = P_{STAT} + P_{DYN}$

P_{TOTAL} = 0.03 mW

Power Consumption

Table 3-14 • **Power Consumption**

Parameter	Description	Condition	Min	Typ	Max	Units
Crystal Oscillator						
$I_{STBXTAL}$	Standby Current of Crystal Oscillator			10		µA
$I_{DYNXTAL}$	Operating Current	RC		0.6		mA
		0.032–0.2		0.6		mA
		0.2–2.0		0.6		mA
		2.0–20.0		0.6		mA
RC Oscillator						
I_{DYNRC}	Operating Current			1		mA
ACM						
	Operating Current (Fixed Clock)			200		µA/MHz
	Operating Current (User Clock)			30		µA
NVM System						
	NVM Array Operating Power					
		Idle		795		µA
		Read operation		See Table 3-11 on page 3-10.		See Table 3-11 on page 3-10.
		Erase		900		µA
		Write		900		µA
$P_{NVMCTRL}$	NVM Controller Operating Power			20		uW/MHz