Actel®

Product Brief

Fusion Family of Mixed-Signal Flash FPGAs with Optional Soft ARM® Support

FlashLock®

Features and Benefits

High Performance Reprogrammable Flash Technology

- Advanced 130-nm, 7-Layer Metal, Flash-Based CMOS Process
- Nonvolatile, Retains Program When Powered-Off
- Live at Power-Up (LAPU) Single-Chip Solution
- 350 MHz System Performance

Embedded Flash Memory

- User Flash Memory – 2 Mbits to 8 Mbits
  - Configurable 8-, 16-, or 32-Bit Datapath
  - 10 ns Access in Read-Ahead Mode
- 1 kbit of Additional FlashROM

Integrated A/D Converter (ADC) and Analog I/O

- Up to 12 bit resolution and Up to 600 ksps
- Internal 2.56 V or External Reference Voltage
- ADC: Up to 30 Scalable Analog Input Channels
- High Voltage Input Tolerance ±12 V
- Current Monitor and Temperature Monitor Blocks
- Up to 10 MOSFET Gate Driver Outputs
  - P- and N-Channel Power MOSFET support
  - Programmable 1, 3, 10, 30 µA and 25 mA Drive Strengths

On-Chip Clocking Support

- Internal 100 MHz RC Oscillator (accurate to 1%)
- Crystal Oscillator Support (32 kHz to 20 MHz)
- Programmable Real-Time Counter (RTC)
- 6 Clock Conditioning Circuits (CCCs) with 1 or 2 Integrated PLLs
  - Phase Shift, Multiply/Divide, and Delay Capabilities
  - Frequency: Input (1.5–350 MHz), Output (0.75–350 MHz)

Low Power Consumption

- Single 3.3 V Power Supply with On-Chip 1.5 V Regulator
- Sleep and Standby Low Power Modes

In-System Programming (ISP) and Security

- Secure ISP with 128-Bit AES Via JTAG
- FlashLock® to Secure FPGA Contents

Advanced Digital I/O

- 1.5 V, 1.8 V, 2.5 V, and 3.3 V Mixed-Voltage Operation
- Bank-Selectable I/O Voltages – Up to 5 Banks per Chip
- Single-Ended I/O Standards: LVTTL, LVCMOS 3.3 V / 2.5 V / 1.8 V / 1.5 V, 3.3 V PCI / 3.3 V PCI-X and LVCMOS 2.5 V / 5.0 V Input
- Differential I/O Standards: LVPECL, LVDS, BLVDS, and M-LVDS
  - Built-In I/O Registers
  - 700 Mbps DDR Operation
- Hot-Swappable I/Os
- Programmable Output Slew Rate, Drive Strength, and Weak Pull-Up/Down Resistor
- Pin-Compatible Packages Across the Fusion Family

SRAMs and FIFOs

- Variable-Aspect-Ratio 4,608-Bit SRAM Blocks (x1, x2, x4, x9, and x18 organizations available)
- True Dual-Port SRAM (except x18)
- Programmable Embedded FIFO Control Logic

Soft ARM7™ Core Support in M7 Fusion Devices

- CoreMP7Sd (with debug) and CoreMP7S (without debug)

Table 1 • **Fusion Family**

Fusion Devices		**AFS090**	**AFS250**	**AFS600**	**AFS1500**
ARM-Enabled Fusion Devices				**M7AFS600**	**M7AFS1500**
General Information	System Gates	90,000	250,000	600,000	1,500,000
	Tiles (D-Flip-Flops)	2,304	6,144	13,824	38,400
	Usable Tiles with CoreMP7S[1]			7,500	32,000
	Usable Tiles with CoreMP7Sd[1]			5,237	29,878
	Secure (AES) ISP	Yes	Yes	Yes	Yes
	PLLs	1	1	2	2
	Globals	18	18	18	18
Memory	Flash Memory Blocks (2 Mbits)	1	1	2	4
	Total Flash Memory Bits	2 M	2 M	4 M	8 M
	FlashROM Bits	1 k	1 k	1 k	1 k
	RAM Blocks (4,608 bits)	6	8	24	60
	RAM kbits	27	36	108	270
Analog and I/Os	Analog Quads	5	6	10	10
	Analog Input Channels	15	18	30	30
	Gate Driver Outputs	5	6	10	10
	I/O Banks (+ JTAG)	4	4	5	5
	Maximum Digital I/Os[2]	75	114	172	278
	Analog I/Os	20	24	40	40

Notes:

1. *Refer to the CoreMP7 datasheet for more information.*
2. *Some debug tools require 10 digital I/Os for external connection.*

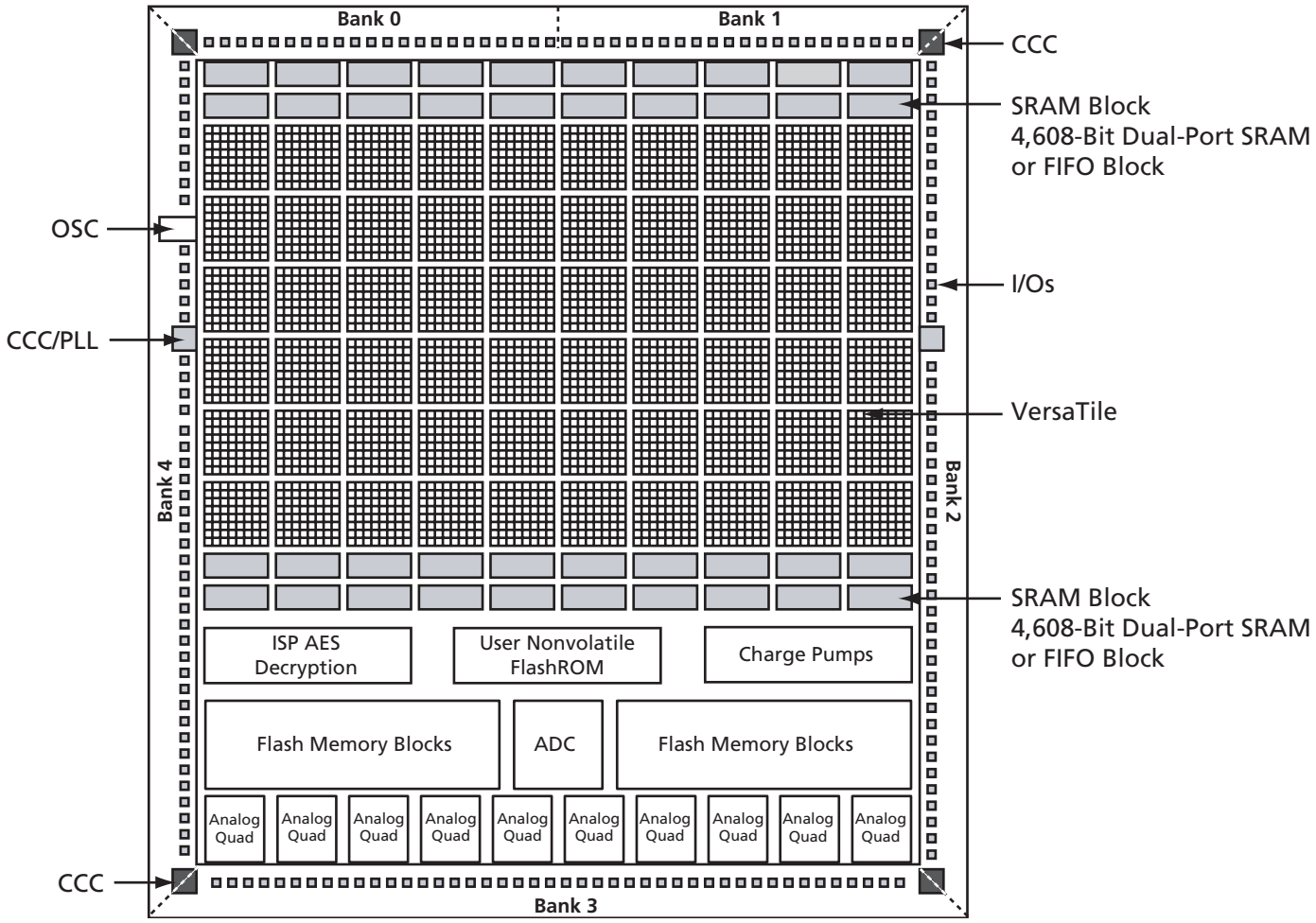


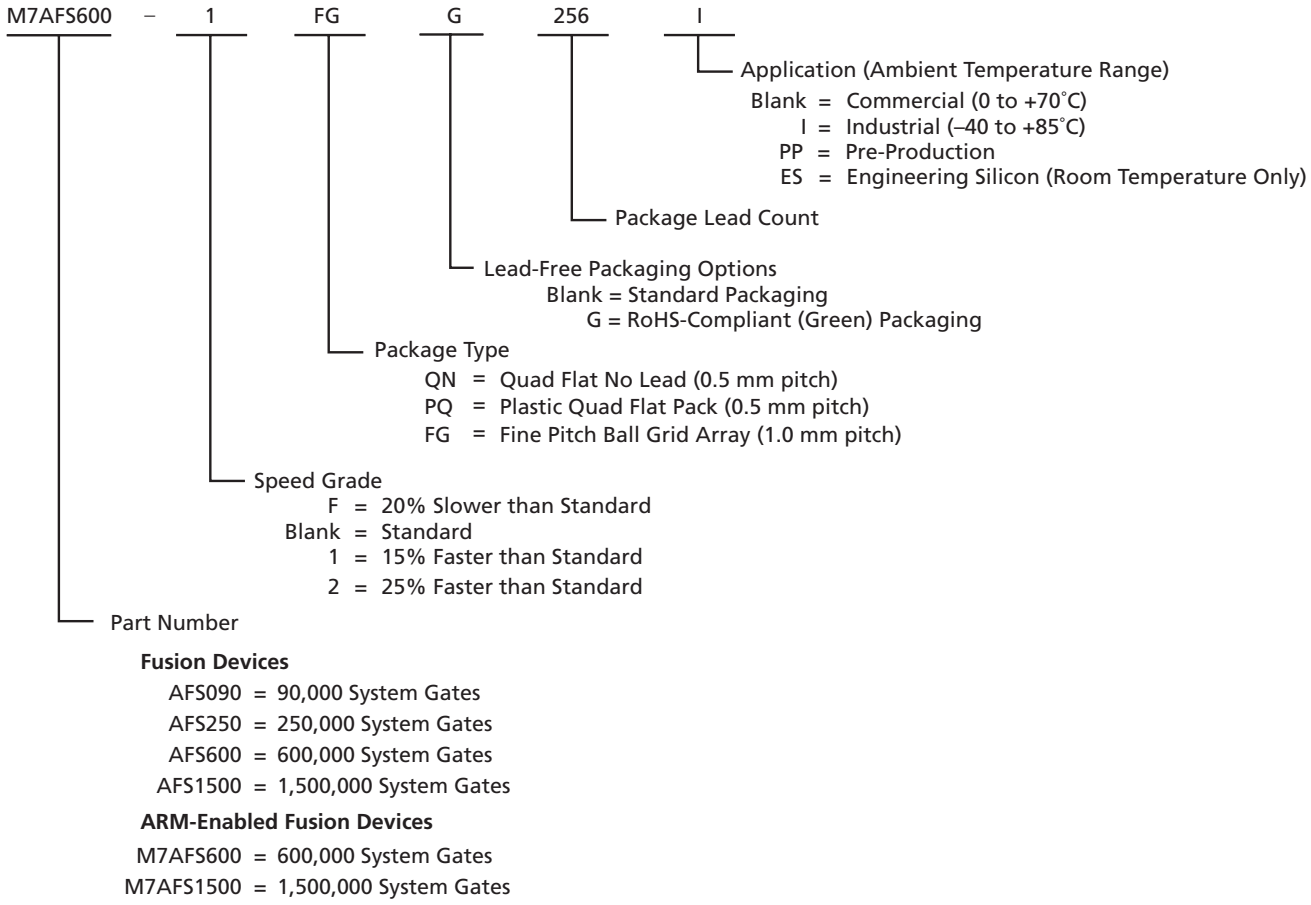
Figure 1 • **Fusion Device Architecture Overview (AFS600)**

Package I/Os: Single/Double-Ended (Analog)

Fusion Devices	AFS090	AFS250	AFS600	AFS1500
ARM-Enabled Devices			**M7AFS600**	**M7AFS1500**
QN108	37/9 (16)			
QN180	60/16 (20)	65/15 (24)		
PQ208		93/26 (24)	95/46 (40)	
FG256	75/22 (20)	114/37 (24)	119/58 (40)	119/58 (40)
FG484			172/86 (40)	228/86 (40)
FG676				278/139 (40)

Note: *All devices in the same package are pin compatible with the exception of the PQ208 package (AFS250 and AFS600).*

Product Ordering Codes



Fusion Devices

AFS090 = 90,000 System Gates
AFS250 = 250,000 System Gates
AFS600 = 600,000 System Gates
AFS1500 = 1,500,000 System Gates

ARM-Enabled Fusion Devices

M7AFS600 = 600,000 System Gates
M7AFS1500 = 1,500,000 System Gates

Note: *DC and switching characteristics for –F speed grade targets based only on simulation. The characteristics provided for –F speed grade are subject to change after establishing FPGA specifications. Some restrictions might be added and will be reflected in future revisions of this document. The –F speed grade is only supported in commercial temperature range.*

Temperature Grade Offerings

Fusion Devices	AFS090	AFS250	AFS600	AFS1500
ARM-Enabled Devices			**M7AFS600**	**M7AFS1500**
QN108	C, I	–	–	–
QN180	C, I	C, I	–	–
PQ208	–	C, I	C, I	–
FG256	C, I	C, I	C, I	C, I
FG484	–	–	C, I	C, I
FG676	–	–	–	C, I

Notes:

1. *C = Commercial Temperature Range: 0°C to 70°C Ambient*
2. *I = Industrial Temperature Range: –40°C to 85°C Ambient*

Speed Grade and Temperature Grade Matrix

	–F[1]	Std.	–1	–2
C[2]	✓	✓	✓	✓
I[3]	–	✓	✓	✓

Notes:

1. *DC and switching characteristics for –F speed grade targets based only on simulation. The characteristics provided for –F speed grade are subject to change after establishing FPGA specifications. Some restrictions might be added and will be reflected in future revisions of this document. The –F speed grade is only supported in commercial temperature range.*
2. *C = Commercial Temperature Range: 0°C to 70°C Ambient*
3. *I = Industrial Temperature Range: –40°C to 85°C Ambient*

Contact your local Actel representative for device availability (http://www.actel.com/contact/offices/index.html).

Introduction and Overview

Introduction

The Actel Fusion™ Programmable System Chip (PSC) satisfies the demand from system architects for a device that simplifies design and unleashes their creativity. As the world's first mixed-signal FPGA family, Fusion integrates mixed-signal analog, Flash memory, and FPGA fabric in a monolithic PSC. Actel Fusion devices enable designers to quickly move from concept to completed design, and then deliver feature-rich systems to market. This new technology takes advantage of the unique properties of Actel Flash-based FPGAs, including a high-isolation, triple-well process, and the ability to support high-voltage transistors to meet the demanding requirements of mixed-signal system design.

Actel Fusion PSCs bring the benefits of programmable logic to many application areas, including power management, smart battery charging, clock generation and management, and motor control. Until now, these applications have only been implemented with costly and space-consuming discrete analog components or mixed-signal ASIC solutions. Actel Fusion PSCs present new capabilities for system development by allowing designers to integrate a wide range of functionality into a single device, while at the same time offering the flexibility of upgrades late in the manufacturing process or after the device is in the field. Actel Fusion devices provide an excellent alternative to costly and time-consuming mixed-signal ASIC designs. In addition, when used in conjunction with the Actel 8051-based or ARM-based soft MCU core, the Actel Fusion technology represents the definitive PSC platform.

Flash-based Fusion devices are live at power-up. As soon as system power is applied and within normal operating specifications, Fusion devices are working. Fusion devices have a 128-bit Flash-based lock and industry-leading AES decryption, used to secure programmed intellectual property (IP) and configuration data. Actel Fusion devices are the most comprehensive single-chip analog and digital programmable logic solution available today.

To support this new ground-breaking technology, Actel has developed a series of major tool innovations to help maximize designer productivity. Implemented as extensions to the popular Actel Libero® Integrated Design Environment (IDE), these new tools will allow designers to easily instantiate and configure peripherals within a design, establish links between peripherals, create or import building blocks or reference designs, and perform hardware verification. This tools suite will also add a comprehensive hardware/software debug capability as well as a suite of utilities to simplify development of embedded soft processor-based solutions.

General Description

The Actel Fusion family, based on the highly successful ProASIC®3 and ProASIC3E Flash FPGA architecture, has been designed as a high-performance, programmable, mixed-signal platform. By combining an advanced Flash FPGA core with Flash memory blocks and analog peripherals, Fusion devices dramatically simplify system design, and as a result, dramatically reduce overall system cost and board space.

The state-of-the-art Flash memory technology offers high-density integrated Flash memory blocks, enabling savings in cost, power, and board area relative to external Flash solutions, while providing increased flexibility and performance. The Flash memory blocks and integrated analog peripherals enable true mixed-mode programmable logic designs. Two examples include using an on-chip soft processor to implement a fully functional Flash MCU, or using high-speed FPGA logic to offer system and power supervisory capabilities. Live at power-up and capable of operating from a single 3.3 V supply, the Fusion family is ideally suited for system management and control applications.

The devices in the Fusion family are categorized by FPGA core density. Each family member contains many peripherals, including Flash memory blocks, analog to digital converter (ADC), high-drive outputs, both RC and crystal oscillators, and real-time counter (RTC). This provides the user with a high level of flexibility and integration to support a wide variety of mixed-signal applications. The Flash memory block capacity ranges from 2 Mbits to 8 Mbits. The integrated 12-bit ADC supports up to 30 independently configurable input channels. The on-chip crystal and RC oscillators work in conjunction with the integrated phase-locked loops (PLLs) to provide clocking support to the FPGA array and on-chip resources. In addition to supporting typical RTC uses such as watchdog timer, the Fusion RTC can control the on-chip voltage regulator to power down the device (FPGA fabric, Flash memory block, and ADC), enabling a low power sleep mode.

The Actel Fusion family offers revolutionary features, never before available in an FPGA. The nonvolatile Flash technology gives the Fusion family the advantage of being a secure, low power, single-chip solution that is live at power-up. Fusion is reprogrammable and offers time to market benefits at an ASIC-level unit cost. These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

The family has up to 1.5 M system gates, supported with up to 270 kbits of true dual-port SRAM, up to 8 Mbits of Flash memory, 1 kbit of user FlashROM, and up to 278 user I/Os. With integrated Flash memory, the Fusion family is the ultimate soft processor platform. The AFS600 and AFS1500 devices both support the Actel ARM7 core (CoreMP7). The ARM-enabled versions are identified with the M7 prefix as M7AFS600 and M7AFS1500.

Flash Advantages

Reduced Cost of Ownership

Advantages to the designer extend beyond low unit cost, high performance, and ease of use. The Flash-based Fusion devices are live at power-up and do not need to be loaded from an external boot PROM. On-board security mechanisms prevent access to the programming information and enable secure remote updates of the FPGA logic. Designers can perform secure remote in-system reprogramming to support future design iterations and field upgrades with confidence that valuable intellectual property (IP) cannot be compromised or copied. Secure ISP can be performed using the industry standard AES algorithm, with MAC data authentication on-board the device. The Fusion family device architecture mitigates the need for ASIC migration at higher user volumes. This makes the Fusion family a cost-effective ASIC replacement solution for applications in the consumer, networking and communications, computing, and avionics markets.

Security

As the nonvolatile, Flash-based Fusion family requires no boot PROM, there is no vulnerable external bitstream. Fusion devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile, Flash programming can offer.

Fusion devices utilize a 128-bit Flash-based key lock and a separate AES key used to secure programmed intellectual property (IP) and configuration data. The FlashROM data in the Fusion devices can also be encrypted prior to loading. Additionally, the Flash memory blocks can be programmed during runtime using the industry-leading AES-128 block cipher encryption standard (FIPS Publication 192). The AES standard was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the DES standard, which was adopted in 1977. Fusion devices have a built-in AES decryption engine and a Flash-based AES key that make Fusion devices the most comprehensive programmable logic device security solution available today. Fusion devices with AES-based security allow for secure remote field updates over public networks, such as the Internet, and ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves. As an additional security measure, the FPGA configuration data of a programmed Fusion device cannot be read back, although secure design verification is possible. During design, the user controls and defines both internal and external access to the Flash memory blocks.

Security, built into the FPGA fabric, is an inherent component of the Fusion family. The Flash cells are located beneath seven metal layers and many device design and layout techniques have been used to make invasive attacks extremely difficult. Fusion with FlashLock and AES security is unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected, making secure remote ISP possible. A Fusion device provides the most impenetrable security for programmable logic designs.

Single Chip

Flash-based FPGAs store the configuration information in on-chip Flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, Flash-based Fusion FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load the device configuration data. This reduces bill-of-materials costs and printed circuit board (PCB) area, and increases security and system reliability.

Live at Power-Up

Flash-based Fusion devices are Level 0 live at power-up (LAPU). LAPU Fusion devices greatly simplify total system design and reduce total system cost by eliminating the need for Complex Programmable Logic Devices (CPLDs). The Fusion LAPU clocking (PLLs) replaces off-chip clocking resources. The Fusion mix of LAPU clocking and analog resources makes these devices an excellent choice for both system supervisor and system management functions. LAPU from a single 3.3 V source enables Fusion devices to initiate, control, and monitor multiple voltage supplies, while also providing system clocks. In addition, glitches and brownouts in system power will not corrupt the Fusion device Flash configuration. Unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables reduction or complete removal of the expensive voltage monitor and

brownout detection devices from the PCB design. Flash-based Fusion devices simplify total system design and reduce cost and design risk, while increasing system reliability.

Firm Errors

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. Another source of radiation-induced firm errors comes from alpha particles. For an alpha to cause a soft or firm error, its source must be in very close proximity to the affected circuit. The alpha source must be in the package molding compound or in the die itself. While low alpha molding compounds are being increasingly used, this helps reduce but does not entirely eliminate alpha-induced firm errors.

Firm errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not occur in Fusion Flash-based FPGAs. Once it is programmed, the Flash cell configuration element of Fusion FPGAs cannot be altered by high-energy neutrons and is therefore immune to errors from them.

Recoverable (or soft) errors occur in the user data SRAMs of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Low Power

Flash-based Fusion devices exhibit power characteristics similar to those of an ASIC, making them an ideal choice for power-sensitive applications. With Fusion devices, there is no power-on current surge and no high current transition, both of which occur on many FPGAs.

Fusion devices also have low dynamic power consumption and support both low power sleep mode and very low power standby mode, offering further power savings.

Advanced Flash Technology

The Fusion family offers many benefits, including nonvolatility and reprogrammability through an advanced Flash-based, 130-nm LVCMOS process with 7 layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant Flash switches allows very high logic utilization (much higher than competing SRAM technologies) without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

Advanced Architecture

The proprietary Fusion architecture provides granularity comparable to standard-cell ASICs. The Fusion device consists of several distinct and programmable architectural features, including the following (Figure 2 on page 9):

- Embedded memories
  - Flash memory blocks
  - FlashROM
  - SRAM and FIFO
- Clocking resources
  - PLL and CCC
  - RC oscillator
  - Crystal oscillator
  - No Glitch MUX (NGMUX)
- Digital I/Os with advanced I/O standards
- FPGA VersaTiles
- Analog components
  - Analog-to-digital converter (ADC)
  - Analog I/Os supporting voltage, current, and temperature monitoring
  - 1.5 V on-board voltage regulator
  - Real-time counter

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic lookup table (LUT) equivalent or a D-flip-flop or latch (with or without enable) by programming the appropriate Flash switch interconnections. This versatility allows efficient use of the FPGA fabric. The VersaTile capability is unique to the Actel families of Flash-based FPGAs. VersaTiles and larger functions are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

In addition, extensive on-chip programming circuitry allows for rapid (3.3 V) single-voltage programming of the Fusion devices via an IEEE 1532 JTAG interface.

Unprecedented Integration

Integrated Analog Blocks and Analog I/Os

Fusion devices offer a robust and flexible analog mixed-signal capability in addition to the high-performance Flash FPGA fabric and Flash memory block. The many built-in analog peripherals include a configurable 32:1 input analog multiplexer (MUX), up to 10 independent metal-oxide semiconductor field-effect transistor

(MOSFET) gate driver outputs, and a configurable ADC. The ADC supports 8-, 10-, and 12-bit modes of operation with a cumulative sample rate up to 600 k samples per second (ksps), differential nonlinearity (DNL) < 1.0 LSB, and Total Unadjusted Error (TUE) of ±4 LSB in 10-bit mode. The TUE is used for characterization of the conversion error, and includes errors from all sources, such as offset and linearity. Internal bandgap circuitry offers 1% voltage reference accuracy with the flexibility of utilizing an external reference voltage. The ADC channel sampling sequence and sampling rate are programmable and implemented in the FPGA logic using Designer and Libero IDE software tool support.

Two channels of the 32-channel ADCMUX are dedicated. Channel 0 is connected internally to V_{CC} and can be used to monitor core power supply. Channel 31 is connected to an internal temperature diode which can be used to monitor device temperature. The 30 remaining channels can be connected to external analog signals. The exact number of I/Os available for external connection signals is device-dependent (refer to Table 1 on page 1 for details).

With Fusion, Actel also introduces the Analog Quad I/O structure (Figure 2 on page 9). Each quad consists of three analog inputs and one gate driver. Each quad can be configured in various built-in circuit combinations, such as three pre-scaler circuits, three digital input circuits, a current monitor circuit, or a temperature monitor circuit. Each pre-scaler has multiple scaling factors programmed by FPGA signals to support a large range of analog inputs with positive or negative polarity. The input range for voltage signals is from –12 V to +12 V with full-scale output values from 0.125 V to 16 V. When the current monitor circuit is selected, two adjacent analog inputs measure the voltage drop across a small external sense resistor. Built-in operational amplifiers (op amps) amplify small voltage signals (2 mV sensitivity) for accurate current measurement. One analog input in each quad may be connected to an external temperature monitor diode and achieves detection accuracy of ±2°C with calibration. In addition to the external temperature monitor diode(s), a Fusion device can monitor an internal temperature diode using dedicated channel 31 of the ADCMUX.

Figure 2 on page 9 illustrates a typical use of the Analog Quad I/O structure. The Analog Quad shown is configured to monitor and control an external power supply. The AV pad is measuring the source of the power supply. The AC pad is measuring the voltage drop across an external sense resistor in order to calculate current. The AG MOSFET gate driver pad turns the external MOSFET on and off. The AT pad is measuring the load side voltage level.

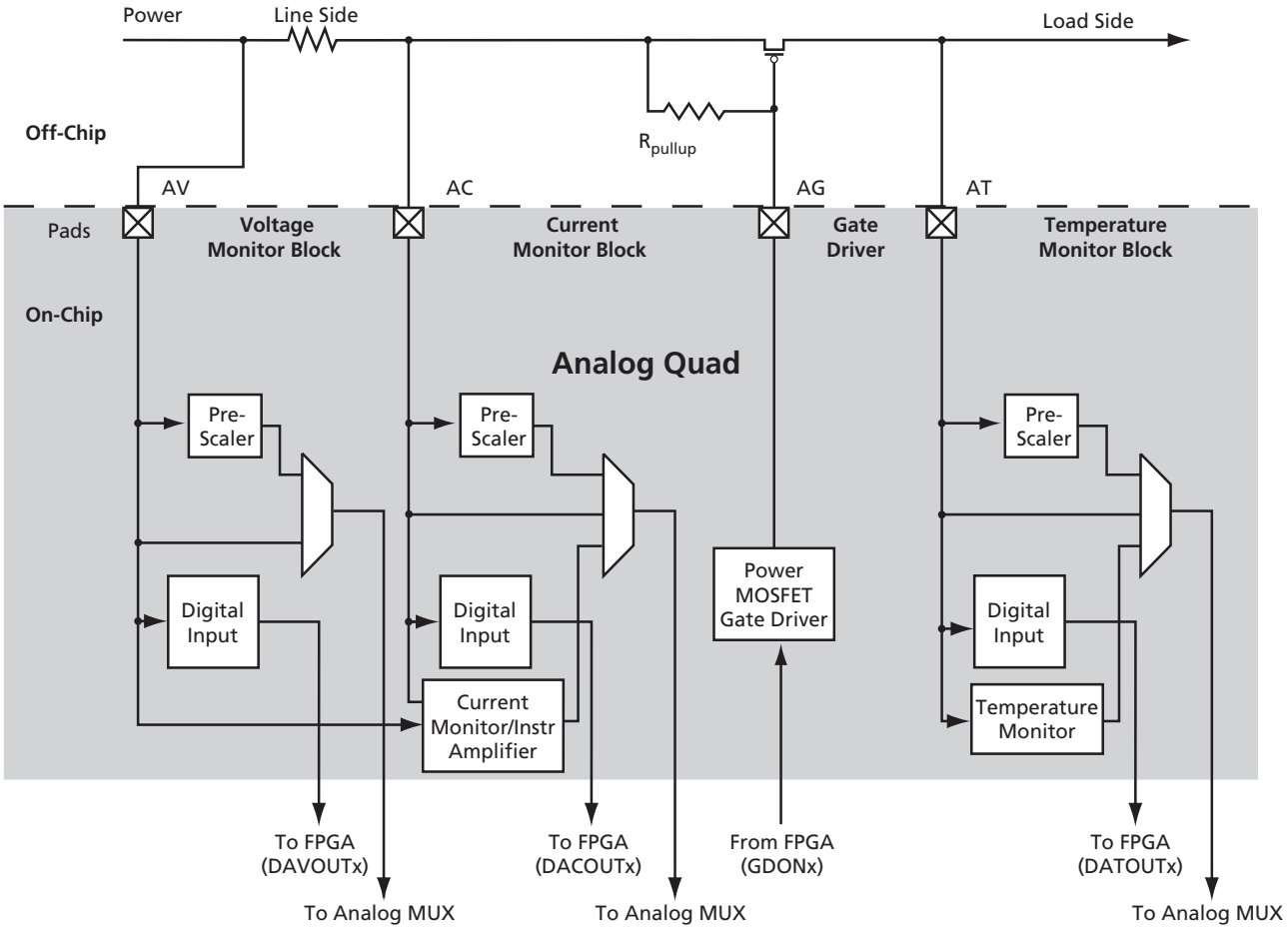


Figure 2 • **Analog Quad**

Embedded Memories

Flash Memory Blocks

The Flash memory available in each Fusion device is composed of 1 to 4 Flash blocks, each 2 Mbits in density. Each block operates independently with a dedicated Flash controller and interface. Fusion Flash memory blocks combine fast access times (60 ns random access and 10 ns access in Read-Ahead mode) with a configurable 8-, 16-, or 32-bit datapath, enabling high-speed Flash operation without wait states. The memory block is organized in pages and sectors. Each page has 128 bytes, with 33 pages comprising one sector and 64 sectors per block. The Flash block can support multiple partitions. The only constraint on size is that partition boundaries must coincide with page boundaries. The flexibility and granularity enable many use models and allow added granularity in programming updates.

Fusion devices support two methods of external access to the Flash memory blocks. The first method is a serial interface that features a built-in JTAG-compliant port, which allows in-system programmability during user or monitor/test modes. This serial interface supports programming of an AES-encrypted stream. Secure data can be passed through the JTAG interface, decrypted, and then programmed in the Flash block. The second method is a soft parallel interface.

FPGA logic or an on-chip soft microprocessor can access Flash memory through the parallel interface. Since the Flash parallel interface is implemented in the FPGA fabric, it can potentially be customized to meet special user requirements. The Flash memory parallel interface provides configurable byte-wide (x8), word-wide (x16), or dual word-wide (x32) data port options. Through the programmable Flash parallel interface, the on-chip and off-chip memories can be cascaded for wider or deeper configurations.

The Flash memory has built-in security. The user can configure either the entire Flash block or the small blocks to prevent unintentional or intrusive attempts to change or destroy the storage contents. Each on-chip Flash memory block has a dedicated controller, enabling each block to operate independently.

The Flash block logic consists of the following sub-blocks:

- Flash block – Contains all stored data. The Flash block contains 64 sectors and each sector contains 33 pages of data.
- Page Buffer – Contains the contents of the current page that is being modified. A page contains 8 blocks of data.
- Block Buffer – Contains the contents of the last block accessed. A block contains 128 data bits.
- ECC Logic – The Flash memory stores error correction information with each block to perform single-bit error correction and double-bit error detection on all data blocks.

User Nonvolatile FlashROM

In addition to the Flash blocks, Actel Fusion devices have 1 kbit of user-accessible, nonvolatile FlashROM on-chip. The FlashROM is organized as 8x128-bit pages. The FlashROM can be used in diverse system applications:

- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard IEEE 1532 JTAG programming interface. Pages can be individually programmed (erased and written). On-chip AES decryption can be used selectively over public networks to securely load data such as security keys stored in the FlashROM for a user design.

The FlashROM can be programmed (erased and written) via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing.

The FlashPoint tool in the Actel Fusion development software solutions, Libero IDE and Designer, has extensive support for Flash memory blocks and FlashROM memory. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Actel Libero IDE and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

SRAM and FIFO

Fusion devices have embedded SRAM blocks along the north and south sides of the device. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256x18, 512x9, 1kx4, 2kx2, and 4kx1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be written through a 4-bit port and read as a single bitstream. The SRAM blocks can be initialized from the Flash memory blocks or via the device JTAG port (ROM emulation mode), using the UJTAG macro.

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost-Empty (AEMPTY) and Almost-Full (AFULL) flags in addition to the normal EMPTY and FULL flags. The embedded FIFO control unit contains the counters necessary for the generation of the read and write address pointers. The SRAM/FIFO blocks can be cascaded to create larger configurations.

Clock Resources

PLL and Clock Conditioning Circuitry (CCC)

Fusion devices provide designers with very flexible clock conditioning capabilities. Each member of the Fusion family contains six CCCs. In the two larger family members, two of these CCCs also include a PLL; the smaller devices support one PLL.

The inputs of the CCC blocks are accessible from the FPGA core or from one of several I/O inputs with dedicated CCC block connections.

The CCC block has the following key features:

- Wide input frequency range (f_{IN_CCC}) = 1.5 MHz to 350 MHz
- Output frequency range (f_{OUT_CCC}) = 0.75 MHz to 350 MHz
- Clock phase adjustment via programmable and fixed delays from –6.275 ns to +8.75 ns
- Clock skew minimization (PLL)
- Clock frequency synthesis (PLL)
- On-chip analog clocking resources usable as inputs:
  - 100 MHz on-chip RC oscillator
  - Crystal oscillator

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°
- Output duty cycle = 50% ± 1.5%
- Low output jitter. Samples of peak-to-peak period jitter when a single global network is used:
  - 70 ps at 350 MHz
  - 90 ps at 100 MHz
  - 180 ps at 24 MHz
  - Worst case < 2.5% × clock period
- Maximum acquisition time = 150 µs
- Low Power Consumption of 5 mW

Global Clocking

Fusion devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there are on-chip oscillators as well as a comprehensive global clock distribution network.

The integrated RC oscillator generates a 100 MHz clock. It is used internally to provide a known clock source to the Flash memory read and write control. It can also be used as a source for the PLLs.

The crystal oscillator supports the following operating modes:

- Crystal (32.768 kHz to 20 MHz)
- Ceramic (500 kHz to 8 MHz)
- RC (32.768 kHz to 4 MHz)

Each VersaTile input and output port has access to nine VersaNets: six main and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via MUXes. The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high-fanout nets.

Digital I/Os with Advanced I/O Standards

The Fusion family of FPGAs features a flexible digital I/O structure, supporting a range of voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V). Fusion FPGAs support many different digital I/O standards, both single-ended and differential.

The I/Os are organized into banks, with four or five banks per device. The configuration of these banks determines the I/O standards supported. The banks along the east and west sides of the device support the full range of I/O standards (single-ended and differential). The south bank supports the Analog Quads (analog I/O). In the family's two smaller devices, the north bank supports multiple single-ended digital I/O standards. In the family's larger devices, the north bank is divided into two banks of digital Pro I/Os, supporting a wide variety of single-ended, differential, and voltage-referenced I/O standards.

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of the following applications:

- Single-Data-Rate (SDR) applications
- Double-Data-Rate (DDR) applications—DDR LVDS I/O for chip-to-chip communications
- Fusion banks support LVPECL, LVDS, BLVDS and M-LVDS with 20 multi-drop points.

VersaTiles

The Fusion core consists of VersaTiles, which are also used in the successful Actel ProASIC3 family. The Fusion VersaTile supports the following:

- All three-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set and optional enable

Refer to Figure 3 for the VersaTile configuration arrangement.

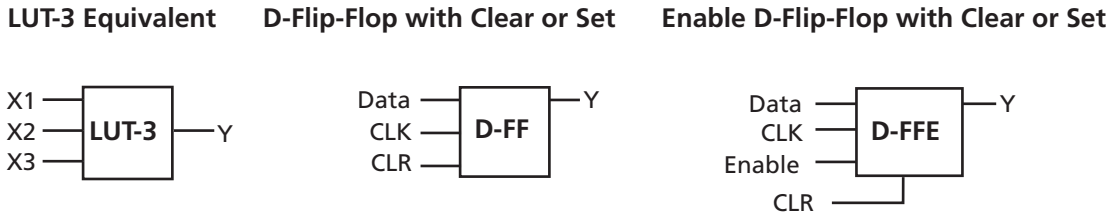


Figure 3 • **VersaTile Configurations**

Datasheet Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," "Production," and "Datasheet Supplement." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advanced or production) containing general product information. This brief gives an overview of specific device and family information.

Advanced

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

Unmarked (production)

This datasheet version contains information that is considered to be final.

Datasheet Supplement

The datasheet supplement gives specific device information for a derivative family that differs from the general family datasheet. The supplement is to be used in conjunction with the datasheet to obtain more detailed information and for specifications that do not differ between the two families.

Export Administration Regulations (EAR)

The products described in this datasheet are subject to the Export Administration Regulations (EAR). They could require an approved export license prior to export from the United States. An export includes the release of the product or disclosure of technology to a foreign national inside or outside the United States.

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