Actel Fusion™

THE WORLD'S FIRST MIXED-SIGNAL FPGA
WITH OPTIONAL SOFT ARM® SUPPORT

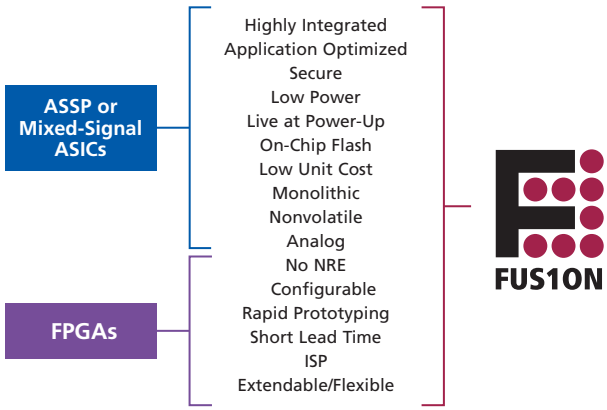
Misc. Photos: Bosch

Key Fusion Features

- In-System Configurable Analog Supports a Wide Variety of Applications
- Up to 8 Mbits of User Flash Memory
- Extensive Clocking Resources:
  - Analog PLLs
  - 1% RC Oscillator
  - Crystal Oscillator Circuit
  - Real-Time Counter (RTC)
- Flash FPGA Fabric
  - Single Chip
  - Low Power
  - Secure
  - Live at Power-Up (LAPU)
  - Firm Error Immune

FlashLock®

The Actel Fusion Programmable System Chip (PSC) is the world's first mixed-signal FPGA family, integrating configurable analog, large Flash memory blocks, comprehensive clock generation and management circuitry, and high performance programmable logic in a monolithic device. Innovative Actel Fusion architecture can be used with the Actel soft MCU core as well as the performance maximized 32-bit ARM7™ core, and is the definitive Programmable System Chip platform.



Actel Fusion: Unlock Creativity. Sim

ONECHIP is all you need

One Chip is All You Need

Until now, system designers were forced to choose costly and space-consuming discrete analog components with programmable logic or mixed-signal ASIC solutions and a processor to implement a typical system. Fixed architectures and other technology barriers prevented the integration of individual components into a single, low cost chip that met all design requirements.

Real World Interface

Fusion interfaces to the real world; up to 30 high-voltage-tolerant analog inputs enable direct connection to signals from –12 V to +12 V, eliminating the need for signal preconditioning. The Fusion analog to digital converter (ADC) is configurable and supports resolutions up to 12 bits, and sample rates up to 600 k samples per second (ksps). Fusion adds additional functionality with the inclusion of multiple differential input current monitor blocks, each with a built-in amplifier, increasing sensitivity and efficiency. The Fusion integrated temperature monitor circuitry allows for the monitoring of multiple remote temperatures with only an external diode. Up to ten high current drive outputs are ideal for metal-oxide semiconductor field-effect transistor (MOSFET) control and/or pulse width modulation (PWM) functions such as direct fan control.

Power and Thermal Management

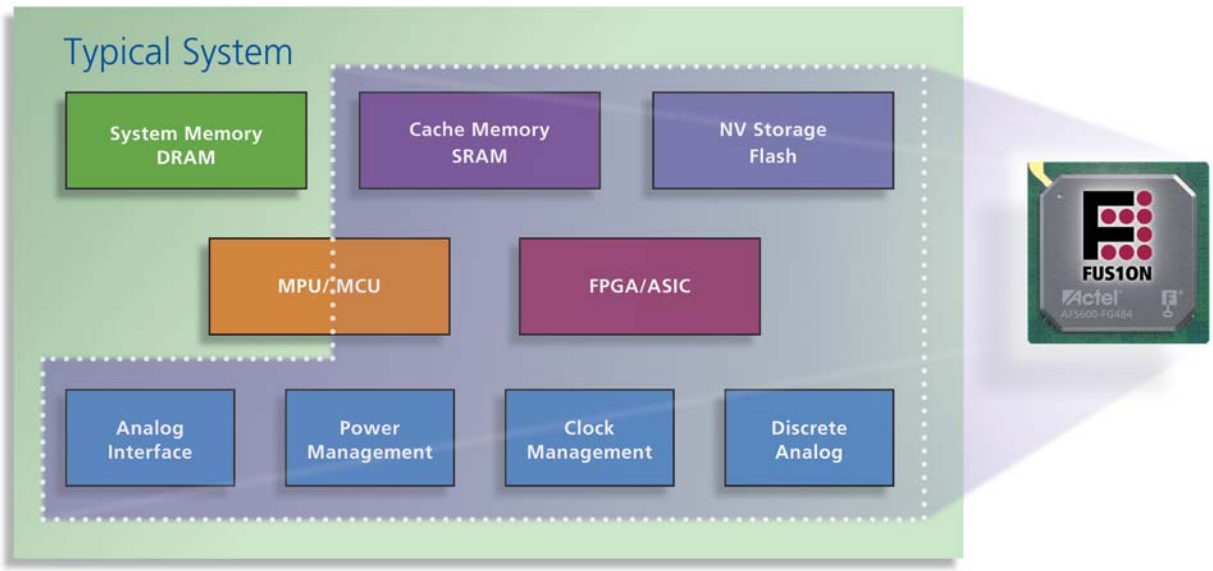
Fusion is Level 0 live at power-up (LAPU) and can be run from a single 3.3 V power supply. These simple startup requirements enable Fusion to act as the ultimate system manager, capable of monitoring and sequencing multiple power supplies to bring up your board in a controlled manner. The ramp-rate of each power supply is programmable from the Fusion device. Fusion easily integrates thermal management aspects of system control boards by combining its temperature monitor and MOSFET/PWM capabilities.

Dynamic System Configuration

The ability of Fusion devices to support many system-level functions in a single chip makes Fusion an ideal candidate for leading edge system management protocols.

Fusion high performance Flash memory blocks provide nonvolatile memory flexibility to every aspect of your design. At system startup, the Flash memory can be used to initialize the system. SRAMs and registers can be automatically loaded with data from the on-chip Flash memory. Prior to system shutdown, the volatile values in SRAM or registers on the Fusion device can be saved back into the on-chip Flash memory—saving the state of the device for the next system startup (SAVE and RESTORE). The

plify Implementation. No Compromises.



Actel Fusion integrates Flash memory, basic analog functionality, "scratch pad" SRAM, and programmable logic into the world's first monolithic mixed-signal FPGA. Embedding a soft microcontroller in the FPGA fabric turns Fusion into the ultimate programmable system chip.

Fusion Flash memory also enables the dynamic changing of system parameters (CONTEXT switch). System boot codes can be stored in the Flash memory for both on-chip and off-chip requirements. The Flash memory can be configured to emulate EEPROM operation with an available endurance extender IP. The optional soft IP Common Flash Interface (CFI) core from Actel can use part of the Flash memory for file storage.

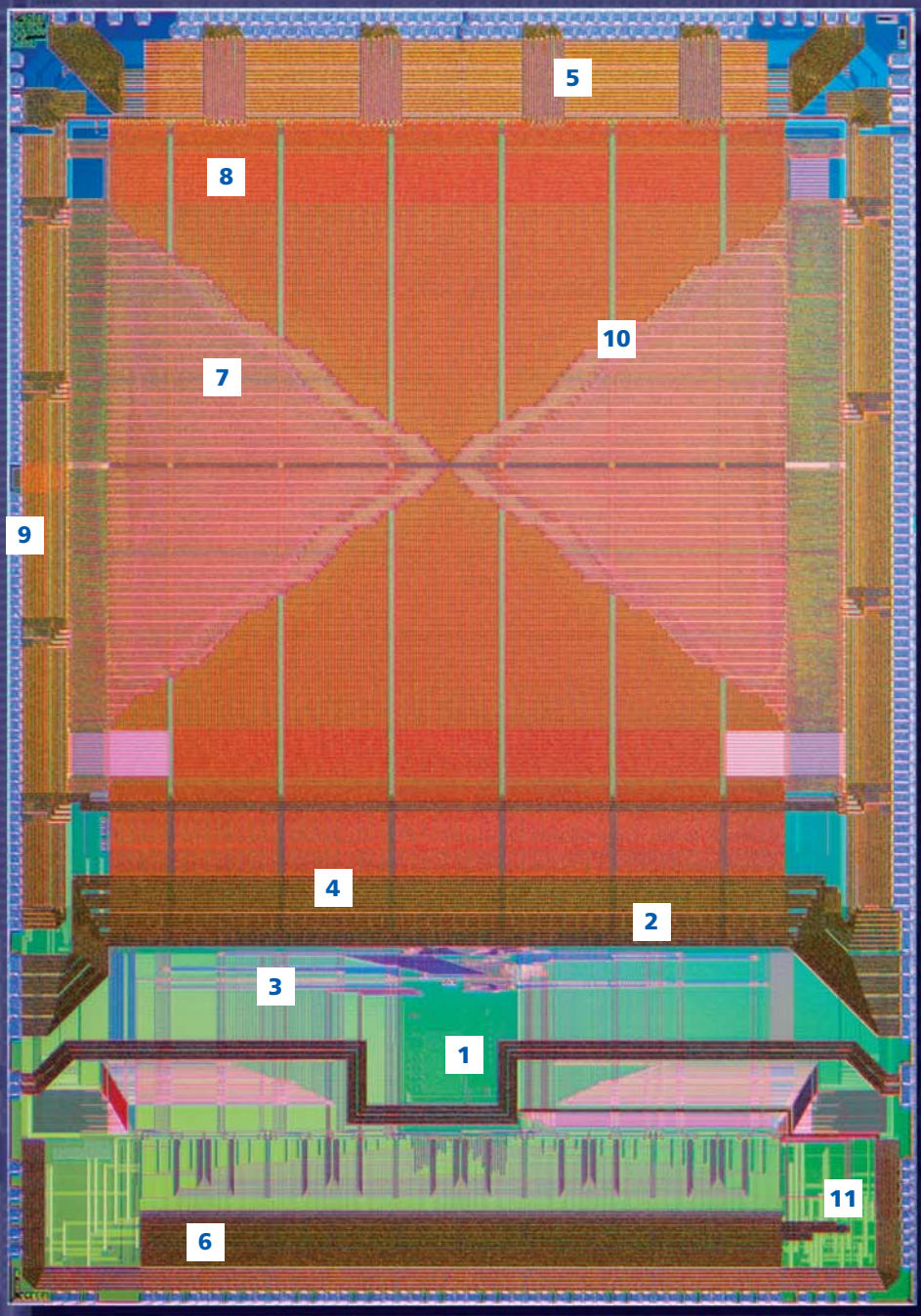
Low Power

Built on a low power, high performance Flash process, Fusion provides industry leading low static and dynamic power. Fusion also offers several sleep and standby modes of operation to further extend battery life in portable applications. The Fusion Real-Time Counter (RTC) offers a wide variety of functionality: sleep, standby, periodic wake-up, and low speed/power operation.

The addition of both a 1% RC oscillator and two-pin crystal oscillator circuit eliminates the need for expensive external clock sources.

Reconfiguring Systems

Inherent in the fabric of Fusion are the benefits of configurability and field reprogrammability from the successful Actel ProASIC®3 family of Flash FPGA devices. Fusion can be securely programmed late in the manufacturing process or after it is in the field. By enabling a single hardware platform to support multiple projects and products, Fusion allows designers to leverage economies of scale in purchasing, while maintaining the ability to customize products for different markets. Both the firmware (Flash memory) and hardware can be updated in a single step.


5
8
10
7
9
4
2
3
1
11
6

Fusion—Mixed-Signal FPGA Architecture

1 Integrated Analog to Digital Converter (ADC)

For the first time, an FPGA supports an integrated ADC, eliminating the need for external mixed-signal support ICs. With resolutions up to 12 bits and frequencies up to 600 ksps, this configurable ADC supports a broad application space.

2 Fusion Supports Low Power

The Fusion Real-Time Counter (RTC) includes a programmable 40-bit counter and match register (timer) that generates time-based match events. In addition to use models such as watchdog timer, device lifetime monitoring, and event timer, the RTC can be used to wake the Fusion device out of sleep mode, enabling very low power modes of operation. The no-glitch MUX (NGMUX) allows the device switch between asynchronous clock domains to occur in a controlled manner. The device switches to a slower clock frequency during periods of relative inactivity, thereby reducing active power consumption.

3 Embedded Flash Memory

The Actel Fusion family is the only programmable logic solution to include up to 8 Mbits of embedded Flash memory, arranged in 1,024-bit pages. This high performance, configurable Flash memory supports 100 MHz operation and data bus widths of of 8, 16, and 32-bits. Utilizing an endurance extender IP block, sections of the Flash memory can emulate an EEPROM device to on-chip or off-chip resources. When used in conjunction with either a soft MCU on-chip or an external MCU, the Flash memory offers an excellent code space solution with the ability to execute in place, eliminating the need to shadow code in RAM. Increasing overall data reliability, the Flash memory integrates error correction circuitry (ECC) with single-bit error fix and two-bit error-detect capabilities.

4 Charge Pumps

Fusion devices are designed to operate from a single 3.3 V supply. The Fusion devices supply all other voltages to write (program) the embedded Flash memory and the FPGA core.

5 Advanced I/O Standards

- 700 Mbps LVDS, BLVDS, and MLVDS capable DDR I/Os
- Multiple I/O banks per device
- Single-ended I/O standards: LVTTL, LVCMOS 3.3 V / 2.5 V / 1.8 V / 1.5 V, 3.3 V PCI / 3.3 V PCI-X, and LVCMOS 2.5 V / 5.0 V input
- Differential I/O standards: LVPECL, LVDS, BLVDS, and MLVDS
- Voltage-referenced I/O standards
- Registered I/Os
- Hot-swap compliant I/Os

6 Analog Quads

Leveraging its high voltage Flash process, Fusion analog I/Os support direct connection from as low as –12 V up to +12 V. By eliminating the need for external components to scale down (or up) signals before and after processing, Fusion reduces cost, component count, and board space, while increasing reliability and ease of use. Differential current and temperature monitor blocks with integrated amplifiers increase accuracy and efficiency.

7 Flash FPGA VersaTile

The programmable logic VersaTile elements of Fusion allow synthesis and mapping tools to use any tile as a three-input lookup table equivalent, a D-flip-flop, or latch (with or without enable). Fusion devices with VersaTiles offer an abundance of registers, so you can often choose a smaller device and still meet register requirements.

8 SRAM and FIFOs

Fusion devices have embedded dual-port SRAM and FIFO blocks along the north and south sides of the device. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256x18, 512x9, 1kx4, 2kx2, and 4kx1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. Dedicated FIFO control logic enables flexible and efficient FIFO implementations.

9 Integrated Oscillators—Crystal and RC

Fusion devices include a complete collection of clocking resources: crystal oscillator circuit, 1% RC oscillator, RTC, NGMUX, and phase-locked loops (PLLs). Fusion devices can generate, multiply, divide, phase shift, and distribute clock signals for both on-chip and off-chip use, eliminating the need for external clock sources.

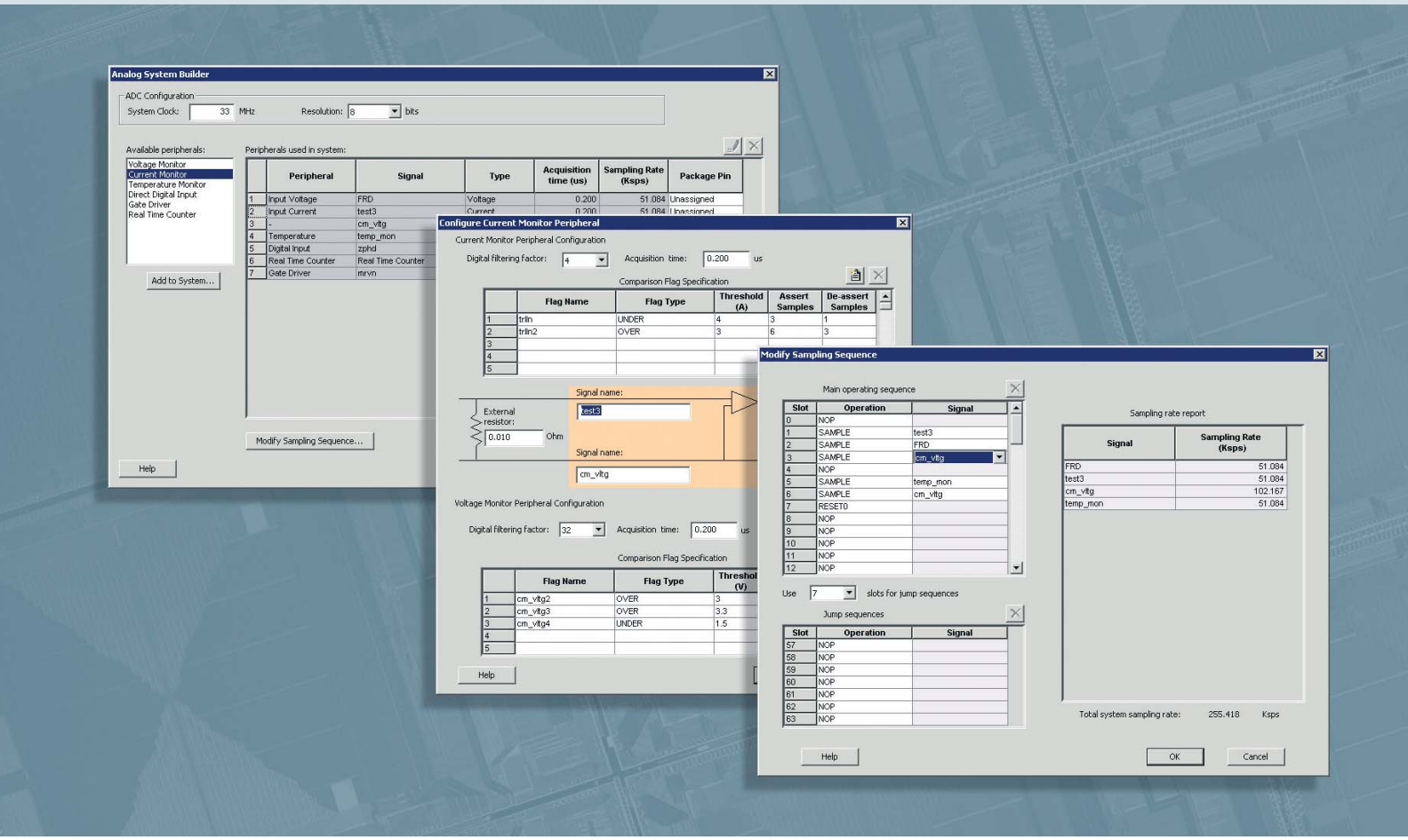
10 Routing Structure

Fusion provides millions of Flash cell switches and an abundance of hierarchical routing resources, enabling extensive design and routing flexibility. VersaNet (segmented global) routing allows high-fanout nets to traverse small or large areas of the Fusion devices with low skew and flexibility. The VersaNet network is used automatically by the software tools to route clocks and high-fanout nets.

11 JTAG

Fusion devices use industry standard JTAG programming (IEEE 1532). In addition, Fusion devices support board-level JTAG (IEEE 1149) I/O boundary scan.

Quickly Build Mixed-Signal Applications



A key benefit of the Actel Fusion PSC is the time to market advantage it offers compared to mixed-signal ASIC development or a complex multi-chip solution. With a host of peripherals and over 90 cores available today, designers can quickly create any number of custom designs. Fusion Smart Peripherals include the analog to digital converter, high voltage analog I/O, current monitor blocks, temperature monitor blocks, embedded Flash memory, RTC, on-chip temperature probe, gate driver, voltage regulator, and oscillators. All IP can access Fusion Smart peripherals directly through the Fusion Smart backbone. Fusion can support a host of applications, including power management, thermal monitoring, motor control, SRAM initialization and configuration, and data acquisition and logging.

Power Management

Fusion is an exceptional device for power management. Unlike today's multi-volt FPGA solutions, Fusion devices can be driven from a single 3.3 V supply, eliminating the need for special power-up sequencers. Fusion can be configured to monitor and sequence a multi-volt system for voltage and current. The unique combination of single volt operation and power management capabilities makes Fusion an excellent candidate for system/board management applications.

Thermal Management

With Fusion, temperature control is built-in. Fusion supports both on-chip (internal diode) and remote temperature monitoring capabilities. The Fusion device can flag the temperature and power at programmable thresholds to indicate a warning, turn on a fan, or shut down the system. Additionally, Fusion can use external temperature sensor inputs to control heating or cooling system elements.

Motor Control

The Fusion device is an excellent choice for motor control applications because it can monitor multiple voltage and current inputs and control multiple outputs in the form of pulse width modulators to control the speed of a motor. In larger motors, the Fusion device can monitor and store temperature data as well as set warning flags, and can even shut down the motor, if necessary. Fusion can monitor current to understand the load on the device, and acquire and store vibration data for the motor.

SRAM FPGA Power Sequencing and Configuration

In addition to the system applications described above, the Fusion device can be used to configure SRAM FPGAs. Since it is live at power-up, Fusion can store the SRAM FPGA program in Flash memory and transmit the bitstream to the volatile FPGA. It can also perform the complex power sequencing required for an SRAM FPGA, eliminating the need for multiple chips to provide the expensive support structure for SRAM FPGAs.

Fusion Design Creation

SmartGen, the Fusion graphical device configuration tool, simplifies design implementation by providing a graphical interface for generating SmartGen intellectual property code with the Analog System Builder and the Flash Memory System Builder features. The Analog System Builder creates SmartGen IP that can configure the device to monitor voltages, current, and temperature, as well as sequence the data samples and set maximum and minimum threshold values for these signals. The Flash Memory System Builder provides an interface to the memory and the analog system, and creates IP to perform memory initialization and enable data storage. With a common soft microcontroller core, such as Core8051, Fusion can enable all of the analog and memory capabilities described above with no additional logic use, in a familiar development environment such as that used for the 8051.

Build Designs Quickly with Actel IP

Fusion users have a substantial amount of intellectual property and application information available to them, enabling them to easily create complex designs. Adding functionality to the Fusion embedded Flash blocks, Actel developed CoreFMEE and CoreCFI. CoreFMEE is a Flash Memory Endurance Extender that can extend the life of the Fusion device's memory or make its operation appear as an EEPROM. CoreCFI is a Common Flash Interface core that allows external users to see Fusion Flash memory as a standard memory device. As with all Actel silicon product families, there is a host of high-quality DirectCore intellectual property cores.

Actel DirectCores

CoreMP7	CoreAI	CoreFMEE
CoreCFI	Core10/100	Core16X50
Core429	Core1553	Core8051
CoreAES128	CoreDDR	CoreFFT
CoreFIR	CoreI2C	CorePCIF
CoreSDLC	CoreSDR	CoreSPI
CoreUART	CoreU1LL	CoreU1PHY

Additional Application Support

In addition to a host of DirectCore and CompanionCore intellectual property, there is extensive application support, including application briefs and application notes on a variety of applications discussed above. Actel Solution Partners add to the Fusion solution with additional products and services, and they have expertise in many application areas.

Innovative Tools Speed Design Development

To support this new ground-breaking technology, Actel has developed a series of major tool innovations to help maximize designer productivity. Implemented as extensions to the popular Actel Libero® Integrated Design Environment (IDE), these new tools will allow designers to easily instantiate and configure peripherals within a design, establish links between peripherals, create or import building blocks (Fusion applets) or reference designs, and perform hardware verification. This tools suite will also add comprehensive hardware/software debug features as well as a suite of utilities to simplify development of embedded soft processor-based solutions.

Hardware Design Creation

Focusing on ease of use and time to market, Actel adopted an integrated approach for design generation, forgoing macro generators and application wrappers. Configuration tools offer designers the capability to select peripherals, and configure and instantiate them into the backbone. Users can select from a variety of analog services, such as temperature, voltage monitoring, and Flash memory services that include save, restore, and load. They can be included in the application without creating a single line of RTL code. Fusion application generators and applet configuration utilities from external vendors are planned for the Actel Fusion tool framework. These design creation tools will be tightly integrated and delivered through the Libero IDE. This enables users to design their applications from prepackaged application generators and configuration tools, with an unprecedented level of ease, cutting down design iteration time.

Maintaining the highest level of flexibility, these configuration engines are optional. System developers are free to configure and control the peripheral directly from their own user design.

Hardware Synthesis and Simulation

The RTL created by a user or by application generators will seamlessly pass through logic and physical synthesis. Due to the added complexity and unprecedented integration of Actel Fusion technology, simulation will play a critical role in design verification. The Actel tool solution provides a full suite of simulation models, providing simulation support for all on-chip resources.

Silicon Debug

The unprecedented integration offered by Actel Fusion technology poses significant challenges for design verification through debugging methods. Actel solves this issue by offering tools that address debugging needs at multiple levels of application abstraction. Users can embed a logic analyzer into the desired blocks within the application, enabling real-time probing. It will also be possible to embed these analyzers in the Fusion backbone and monitor the activity of the Fusion peripherals in real-time. Actel will also offer additional invasive debug capability, enabling users to interactively access and modify information related to Fusion peripherals, register files, embedded SRAM, and Flash memory.

Software Design and Development Tools

Actel supports tools required to create code for MCU units, CoreMP7, and Core8051. The tools from Actel and other vendors help users build applications in C that are efficient and optimized for MCU targets for Actel Fusion devices. Users can debug their program code with the help of software debuggers as well as fully integrated development environments.

Fusion Starter Kit

The Fusion Starter Kit includes the following:

- **Evaluation Board with an AFS600-FG256 Fusion Device**
- **Actel Libero IDE Gold**
- **FlashPro3 and Programming Cable**
- **Power Supply**
- **User's Guide Including PCB Schematics**
- **Sample Design**

All-Inclusive and Low Cost

The low cost Fusion Starter Kit contains everything you need to start using the advanced features of the Actel Fusion family. You can explore the various benefits of Fusion mixed-signal FPGAs, including ISP, device serialization, and FlashLock® on-chip system security. Additionally, this kit has many added features to allow designers to fully experiment with Fusion capabilities.

The Fusion evaluation board has on-board voltage regulation, enabling you to independently set the I/O voltages to 1.5 V or 3.3 V on each of two I/O banks. Two of the remaining three I/O banks are fixed at 3.3 V. The remaining I/O bank is for high voltage analog I/Os that support direct connection to voltages that can range from –12 V to +12 V. These I/Os support current monitoring, temperature monitoring, and MOSFET driver outputs.

System clock generation, manipulation, and distribution are enabled with an on-chip RC oscillator, crystal oscillator circuit, and PLLs. Eight LEDs and four switches provide simple inputs and outputs to the system. The Fusion Flash memory can support multiple functions, including state saving of volatile RAM and registers prior to power-down, initialization of RAM and registers at power-up, boot code store, and data logging. The on-board LCD can be used to display values of converted analog signals (voltage, current, or temperature) and Flash memory contents.

Prototyping headers connect to all the Fusion device pins, enabling you to add components to the evaluation board easily. The board is equipped with a prototyping area to enable design experimentation with the addition of components. External temperature sensors and current sensing circuitry for power control applications are provided.

The Fusion evaluation board features a high brightness, multi-color LED for illustrating temperature changes and PWM fan control by varying the brightness of the LED. The board is also equipped with a 40-pin daughter card connector for use with system boards developed by Actel, customers, or third party partners, allowing users to easily and cost-effectively add functionality or connect to larger target systems. Two programming headers on the board support in-system programming (ISP) of single and JTAG-chained boards using FlashPro3.

FlashPro3

FlashPro3 is targeted at the latest generation of Flash devices to be offered by Actel: Fusion and M7 Fusion devices. FlashPro3 offers extremely high-speed performance through the use of USB 2.0 and is high speed compliant for full use of the 480 Mbps bandwidth. Powered exclusively via USB, FlashPro3 provides the programming voltage of 3.3 V. Multiple FlashPro3 programmers may be connected together via USB hubs to enable multiple systems to be programmed in parallel using just one PC with the FlashPro software. As with all programmers in the FlashPro series, multiple devices may be connected together in a JTAG chain.

The addition of Fusion high performance Flash memory blocks supports multiple functions, including state saving of volatile RAM and registers prior to power-down, initialization of RAM and registers at power-up, boot code store, data logging, and configuration data for the analog peripherals. The embedded FlashROM offers another programmable space, supporting use models such as device serialization.

Inherent in the Fusion programmable logic fabric are the benefits of configurability and field reprogrammability shared by the successful Actel ProASIC3 family of Flash FPGA devices. The Flash memory of Fusion devices can be easily programmed and re-programmed with the FlashPro3 programmer. FlashPro3 supports a robust programming solution for the three regions of the Fusion device (FPGA core, Flash blocks, and FlashROM).

All three regions can be programmed in a single step, such as on a manufacturing line, when only a single device configuration is needed. However, each region can be programmed separately from the other two, increasing programming efficiency and enabling independent updates of design (FPGA code), firmware (Flash memory blocks), or ROM (FlashROM).

Programming can be done in conjunction with the embedded AES decryption engine, enabling secure programming both on the factory floor and in the field. Using an encrypted file for field upgrades enables the file to be sent over unsecured networks (such as the Internet) while keeping the contents of the file secure. This method can be used on both design file upgrades and firmware upgrades. The embedded Flash memory blocks can be programmed with the data while still encrypted, and decrypted only when needed by the system.

Debug Tools

Designs programmed into Fusion and M7 Fusion devices can be debugged using logical analyzer software, working through the interface provided by the FlashPro3 programmer.

The Logic Navigator software from Actel also allows the control and exercise of the architecture-specific features of Fusion, such as the ADC, the Flash memory blocks, and the RTC, with no need to program a design into the FPGA core fabric itself. As a complete programming and debugging tool chain, FlashPro3 keeps development costs down by eliminating the need for additional hardware debug solutions.

Availability

FlashPro3 is available as part of the low cost Fusion starter kit.

Single Chip

Flash-based FPGAs store the configuration information in on-chip Flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure and no external configuration data load is required at system power-up. Flash-based Fusion FPGAs do not require additional system components such as configuration serial nonvolatile memory (EEPROM) or a Flash-based microcontroller in order to load the device configuration data at every system power-up. Increased Fusion functionality can remove several additional components from the board, such as Flash memory, discrete analog ICs, clock sources, EEPROM, and real-time clocks, thereby reducing system cost and board space requirements.

Low Power

Low Power

The Actel Flash-based Fusion devices exhibit power characteristics similar to those of an ASIC, making them an ideal choice for battery-operated and other power-sensitive applications. With Fusion devices, there is no power-on current surge and no high-current transition; these occur on many SRAM FPGAs. Fusion devices have low static and dynamic power consumption, further maximizing power savings. These devices also support sleep and standby modes of operation to greatly reduce power consumption. Another unique feature of Fusion is the ability to dynamically shift between normal clock speeds and low clock operation during periods of inactivity, and switch back to full speed when needed.

Live at Power-Up

Live at Power-Up

Flash-based Fusion devices are live at power-up (LAPU). As soon as system power is applied and within normal operating specifications, Fusion devices are working. The live at power-up feature of Fusion devices greatly simplifies total system design and often allows for the removal of complex programmable logic devices (CPLDs) from the system. Glitches and brownouts in system power will not corrupt the Fusion device's Flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This allows designers to reduce or completely remove the expensive power sequencing, voltage monitor, and brownout detection devices from PCB. Simplifying the total system design by using Flash-based Fusion devices reduces cost and design risk while increasing system reliability and improving system initialization time.

Secure

Security

Fusion devices incorporate the Actel FlashLock feature, providing a unique combination of reprogrammability and design security without external overhead. These advantages can only be offered by an FPGA with nonvolatile Flash memory. Fusion devices have a 128-bit Flash-based lock and industry-leading on-chip AES decryption core, used to secure programmed IP and configuration data. The AES-128-block cipher is a faster, more secure government-approved replacement for DES. Fusion devices have the most comprehensive programmable logic device security solution available today. Fusion devices with AES-based security allow for secure, remote field updates of both system design and Flash memory content (over public networks such as the Internet), and ensure that valuable intellectual property remains out of the hands of system overbuilders, system cloners, and IP thieves. The FPGA design of programmed Fusion devices cannot be read back, though secure (AES-based) design verification is possible. Many device design and layout techniques have been used to make invasive attacks extremely difficult. For example, Flash cells are located beneath seven metal layers, making tampering with the Flash elements extremely difficult. Care has been taken to remove single points of attack in the device's programming control logic.

Neutron Immune

Firm Errors

Firm errors occur when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell in SRAM FPGAs and thus change the logic, routing, or I/Os in an unpredictable and uncontrollable way. These errors are impossible to prevent in SRAM FPGAs and can result in failure-in-time (FIT) rates in the thousands. The consequences of these types of errors may result in a complete system failure and major support and product liability issues. The configuration element of Fusion FPGAs, the Flash cell, cannot be altered by high-energy neutrons and is therefore immune to neutron effects.

Actel Fusion Product Table

Fusion Devices		AFS090	AFS250	AFS600	AFS1500
ARM-Enabled Fusion Devices				M7AFS600	M7AFS1500
General	System Gates	90,000	250,000	600,000	1,500,000
	Tiles (D-Flip-Flops)	2,304	6,144	13,824	38,400
	Usable Tiles with CoreMP7S[1]	—	—	7,500	32,000
	Usable Tiles with CoreMP7Sd[1]	—	—	5,237	29,878
	Secure (AES) ISP	Yes	Yes	Yes	Yes
	PLLs	1	1	2	2
	Globals	18	18	18	18
Memory	Flash Memory Blocks (2 Mbits)	1	1	2	4
	Total Flash Memory Bits (Mbits)	2	2	4	8
	FlashROM Bits (kbits)	1	1	1	1
	RAM Blocks (4,608 bits)	6	8	24	60
	RAM (kbits)	27	36	108	270
Analog and I/Os	Analog Quads	5	6	10	10
	Analog Input Channels	15	18	30	30
	Gate Driver Outputs	5	6	10	10
	I/O Banks (+ JTAG)	4	4	5	5
	Maximum Digital I/Os[2]	75	114	172	278
	Analog I/Os	20	24	40	40
I/O: Single-/Double-Ended (Analog)	QN108	37/9 (16)			
	QN180	60/16 (20)	65/15 (24)		
	PQ208		93/26 (24)	95/46 (40)	
	FG256	75/22 (20)	114/37 (24)	119/58 (40)	119/58 (40)
	FG484			172/86 (40)	228/86 (40)
	FG676				278/139 (40)

Notes: [1] Refer to the CoreMP7 datasheet for more information.
[2] Some debug tools require 10 digital I/Os for external connection.

For more information regarding **Actel Fusion Flash FPGA families**, please visit the Actel website at **www.actel.com** or contact your local sales representative.

Actel®
www.actel.com

Actel Corporation
2061 Stierlin Court
Mountain View, CA
94043-4655 USA
Phone 650.318.4200
Fax 650.318.4600

Actel Europe Ltd.
Dunlop House, Riverside Way
Camberley, Surrey GU15 3YL
United Kingdom
Phone +44 (0) 1276 401 450
Fax +44 (0) 1276 401 490

Actel Japan
www.jp.actel.com
EXOS Ebisu Building 4F
1-24-14 Ebisu Shibuya-ku
Tokyo 150, Japan
Phone +81.03.3445.7671
Fax +81.03.3445.7668

Actel Hong Kong
www.actel.com.cn
Suite 2114, Two Pacific Place
88 Queensway, Admiralty
Hong Kong
Phone +852 2185 6460
Fax +852 2185 6488

ONECHIP is all you need

© 2006 Actel Corporation. All rights reserved. The Actel name and logo are trademarks of Actel Corporation. All other trademarks and service marks are the property of their respective owners. 55700022-2/4.06