Configuring SRAM FPGAs Using Actel Fusion™

Introduction

Due to the nature of SRAM technology, SRAM-based FPGAs are volatile. Therefore, SRAM-based FPGAs lose their configuration when powered off and need to be reconfigured at every power-up. Hence, almost every system using SRAM-based FPGAs contains an additional nonvolatile memory such as Flash PROM or EEPROM to store the configuration data and load it into the SRAM-based FPGA after power-up. In many applications, a complex programmable logic device (CPLD) is used in addition to the external configuration memory to perform the vital functions of the system necessary at power-up. One Actel Fusion device can replace several components: the configuration memory, the power management CPLD and, often, even the SRAM FPGA itself.

Actel Fusion devices are nonvolatile, live at power-up, and contain embedded Flash memory blocks, providing a single-chip, low cost solution for many applications. These features enable the user to integrate both CPLD and configuration memory into the Fusion device if the functionality of the SRAM-based FPGA itself cannot be incorporated in the Fusion devices. In addition, Fusion FPGAs offer many other unique features such as on-chip voltage regulator, analog to digital (A/D) converter, and real-time counter, which enable designers to integrate even more functionalities of their system into a single Fusion FPGA. For example, Fusion devices can incorporate and perform power management and system supervisory functions such as power-up ramp-rate and sequence control; voltage, current and temperature monitoring; and flagging supervisory system protection based on implemented flags and power-on and brown-out detection. This document provides an overview of how an Actel Fusion device can be used to configure an SRAM-based FPGA.

Implementation

The Flash memory in Fusion devices can be used to store the configuration bitstream of SRAM-based FPGAs. The size of the available Flash memory varies between 2 Mbits and 8 Mbits, depending on the size of the Fusion device (AFS090 and AFS1500 are the smallest and largest members of the Fusion family, respectively). This size of memory is sufficient for configuration of a variety of SRAM-based FPGAs[1].

User logic, implemented in the FPGA fabric of Fusion devices, is needed to interface between the embedded Flash memory and the SRAM-based FPGA configuration pins. Depending on the user logic, the SRAM-based FPGA can be configured in various modes, such as master-parallel, slave-parallel, master-serial, and slave-serial.

Figure 1 illustrates the simplified block diagram of the implementation of such applications.

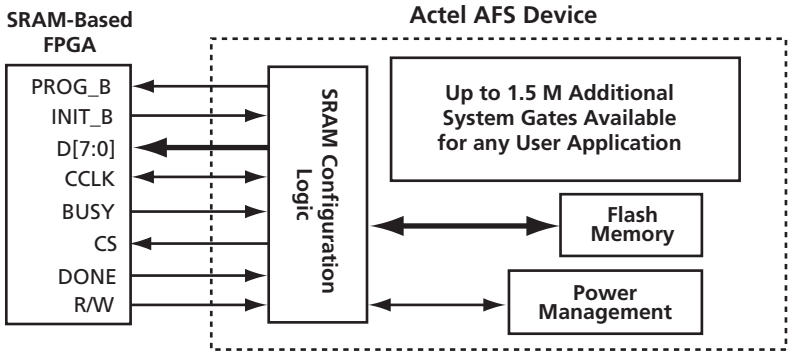

Figure 1 • **Block Diagram of Real-Time Clock System Implementation**

1. *Refer to each SRAM-based FPGA datasheet for the size of the memory required to store the configuration bitstream.*

In Figure 1 on page 1, the SRAM-based FPGA is being configured in parallel mode (master or slave, depending on the direction of the configuration clock). The Actel CoreCFI can be used to create a common parallel Flash interface to the embedded Flash memory blocks within Fusion devices. In this case, the user interface of CoreCFI can be connected to the SRAM-based FPGA configuration pins, similar to any common parallel Flash PROM. However, any other user logic can also be used to interface between the embedded Flash memory block and the SRAM–based FPGA. For example, if a microcontroller such as 8051 is implemented in the Fusion device, the same microcontroller can be used to configure the SRAM-based FPGA with the bitstream stored in the embedded Flash memory block. Furthermore, the Smart backbone of Fusion technology may also help designers to create their own Flash memory interface. For example, using the SmartGen Flash Memory System Builder, designers can create a data storage client that enables them to partition the Flash memory and specify the memory content for that partition.

In the implementation shown in Figure 1 on page 1, a power management block, implemented in Actel Fusion devices, detects the power supplies necessary for the configuration of the SRAM-based FPGA. Once the voltage rails are powered up to their required levels, the power management block signals to the interface logic that conditions are ready to start the configuration. The interface logic then activates the PROG_B and CS signals and starts the configuration process using the bitstream stored in the embedded Flash memory block.

The contents of the Flash memory (the SRAM-based FPGA configuration bitstream) should be in Intel-Hex, Motorola-S, Actel-Hex, or Actel-Binary format. Using SmartGen and Actel Libero® Integrated Design Environment (IDE), the configuration bitstream is incorporated into a STAPL file and programmed into the embedded Flash memory of Fusion devices.

Conclusion

Actel Fusion FPGAs contain an embedded Flash memory block which can be used to store the configuration bitstream of an SRAM-based FPGA. Additionally, the power and clock management of the system can also be integrated into the Fusion devices, providing a cost-effective solution that incorporates configuration, power management, clock management and many other applications into a single chip.

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