Device Architecture

Introduction

Flash Technology

Advanced Flash Switch

Unlike SRAM FPGAs, the ProASIC3E family uses a live at power-up ISP Flash switch as its programming element. Flash cells are distributed throughout the device to provide nonvolatile, reconfigurable programming to connect signal lines to the appropriate VersaTile inputs and outputs. In the Flash switch, two transistors share the floating gate, which stores the programming information (Figure 2-1). One is the sensing transistor, which is only used for writing and verification of the floating gate voltage. The other is the switching transistor. The latter is used to connect or separate routing nets, or to configure VersaTile logic. It is also used to erase the floating gate. Dedicated high-performance lines are connected as required using the Flash switch for fast, low-skew, global signal distribution throughout the device core. Maximum core utilization is possible for virtually any design. The use of the Flash switch technology also removes the possibility of firm errors, which are increasingly common in SRAM-based FPGAs.

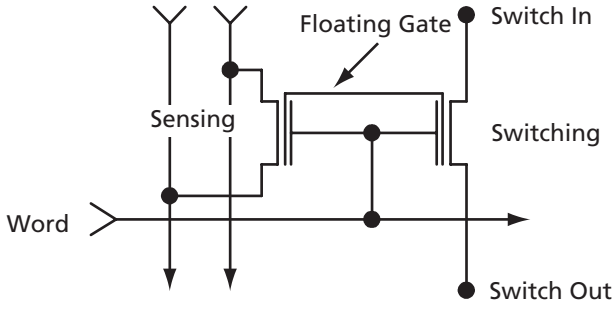


Figure 2-1 • **ProASIC3E Flash-Based Switch**

Device Overview

The ProASIC3E device family consists of five distinct programmable architectural features (Figure 2-2):

- FPGA fabric/core (VersaTiles)
- Routing and clock resources (VersaNets)
- FlashROM memory
- Dedicated SRAM/FIFO memory
- Pro I/O structure

Core Architecture

VersaTile

The proprietary ProASIC3E family architecture provides granularity comparable to gate arrays. The ProASIC3E device core consists of a sea-of-VersaTiles architecture.

As illustrated in Figure 2-3 on page 2-3, there are four inputs in a logic VersaTile cell, and each VersaTile can be configured using the appropriate Flash switch connections:

- Any three-input logic function
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set (on a fourth input)

VersaTiles can flexibly map the logic and sequential gates of a design. The inputs of the VersaTile can be inverted (allowing bubble pushing), and the output of the tile can connect to high-speed, very-long-line routing resources. VersaTiles and larger functions can be connected with any of the four levels of routing hierarchy.

When the VersaTile is used as an enable D-flip-flop, SET/CLR is supported by a fourth input. The SET/CLR signal can only be routed to this fourth input over the VersaNet (global) network. However, if in the user's design the SET/CLR signal is not routed over the VersaNet network, a compile warning message will be given and the intended logic function will be implemented by two VersaTiles instead of one.

The output of the VersaTile is F2 (Figure 2-3 on page 2-3) when the connection is to the ultra-fast local lines, or YL when the connection is to the efficient long-line or very-long-line resources.

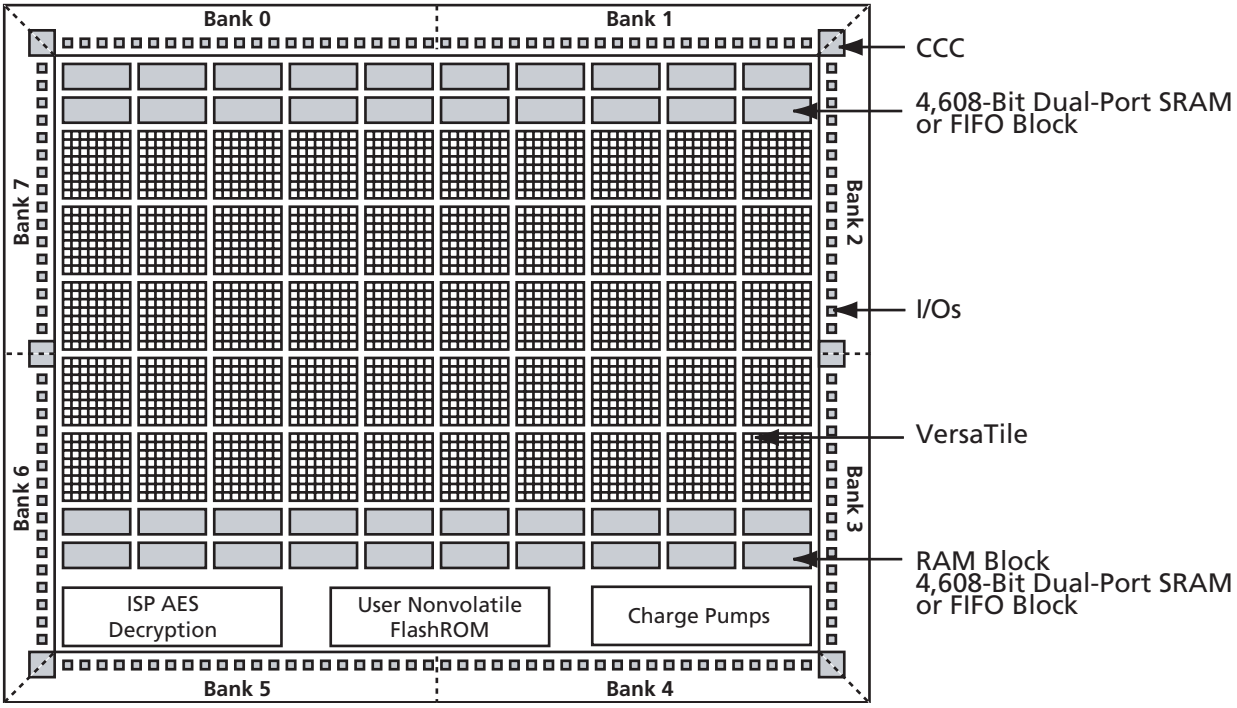
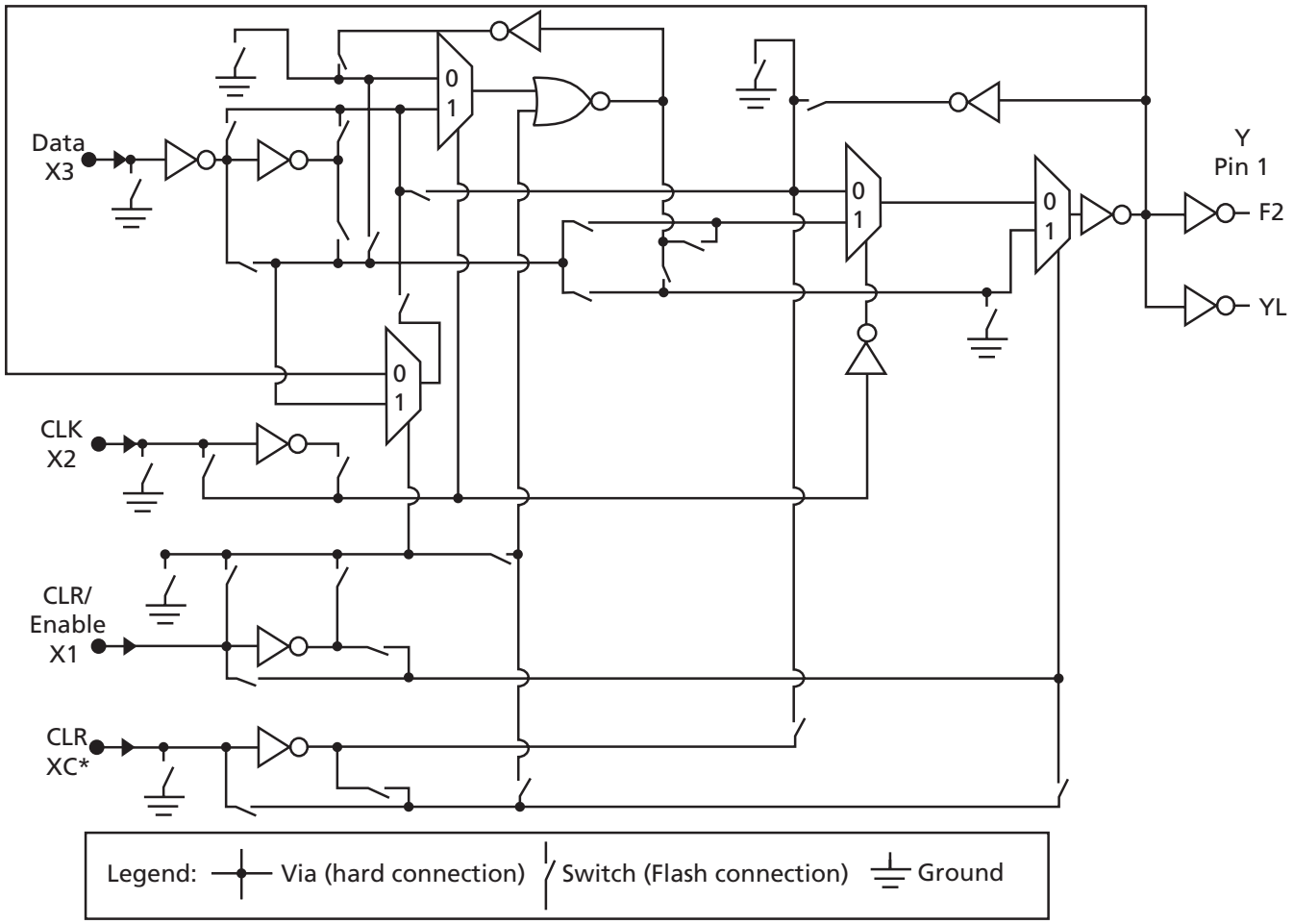


Figure 2-2 • **Device Architecture Overview**



Note: **This input can only be connected to the global clock distribution network.*

Figure 2-3 • **ProASIC3E Core VersaTile**

Array Coordinates

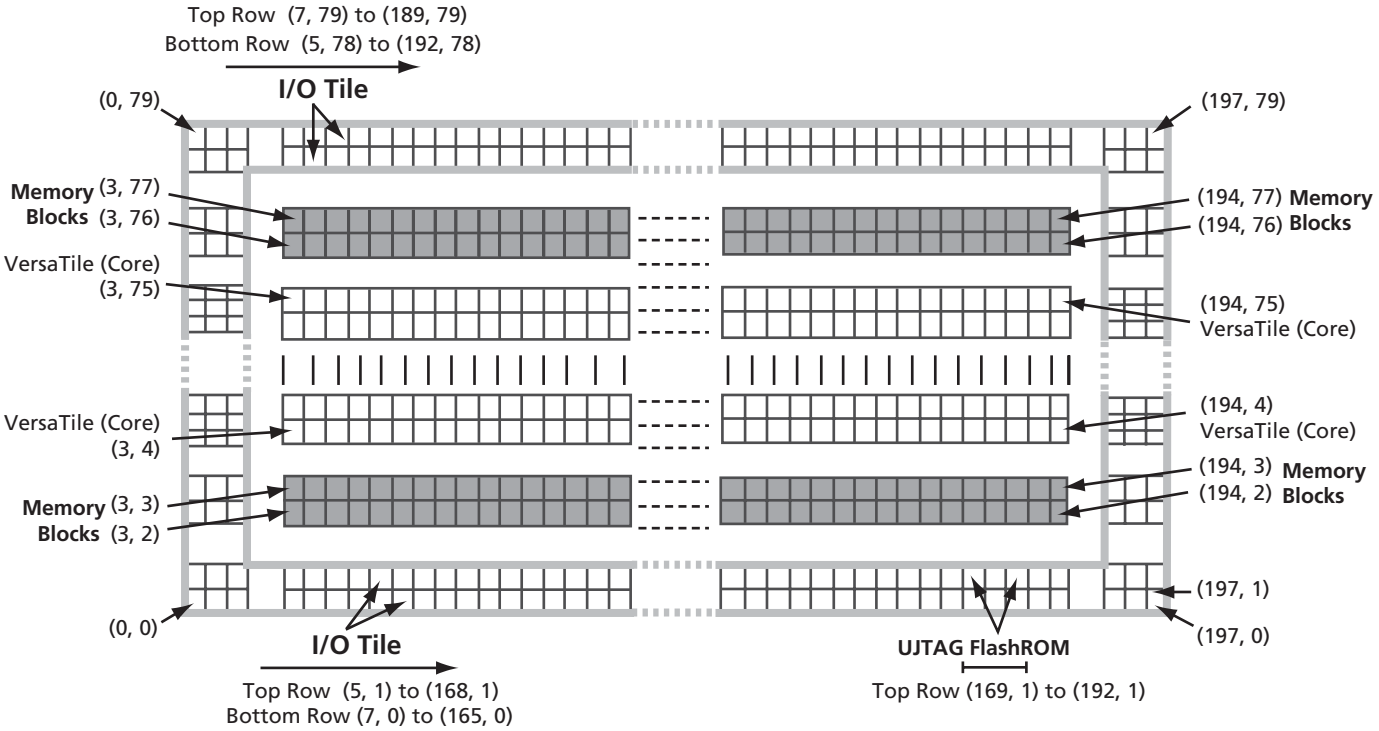
During many place-and-route operations in the Actel Designer software tool, it is possible to set constraints that require array coordinates. Table 2-1 provides array coordinates of core cells and memory blocks. The array coordinates are measured from the lower left (0, 0). They can be used in region constraints for specific logic groups/blocks, designated by a wildcard, and can contain core cells, memories, and I/Os.

I/O and cell coordinates are used for placement constraints. Two coordinate systems are needed because there is not a one-to-one correspondence between I/O cells and core cells. In addition, the I/O coordinate system changes depending on the die/package combination. It is not listed in Table 2-1. The Designer ChipPlanner tool provides array coordinates of all I/O locations. I/O and cell coordinates are used for placement constraints. However, I/O placement is easier by package pin assignment.

Figure 2-4 illustrates the array coordinates of an A3PE600 device. For more information on how to use array coordinates for region/placement constraints, see the *Designer User's Guide* or online help (available in the software) for ProASIC3E software tools.

Table 2-1 • **ProASIC3E Array Coordinates**

	VersaTiles				Memory Rows		All	
	Min.		Max.		Bottom	Top	Min.	Max.
Device	x	y	x	y	(x, y)	(x, y)	(x, y)	(x, y)
A3PE600	3	4	194	75	(3, 2)	(3, 76)	(0, 0)	(197, 79)
A3PE1500	3	4	322	123	(3, 2)	(3, 124)	(0, 0)	(325, 127)
A3PE3000	3	6	450	173	(3, 2) or (3, 4)	(3, 174) or (3, 176)	(0, 0)	(453, 179)



Note: *The vertical I/O tile coordinates are not shown. West side coordinates are {(0, 2) to (2, 2)} to {(0, 77) to (2, 77)}; east side coordinates are {(195, 2) to (197, 2)} to {(195, 77) to (197, 77)}.*

Figure 2-4 • **Array Coordinates for A3PE600**

Routing Architecture

Routing Resources

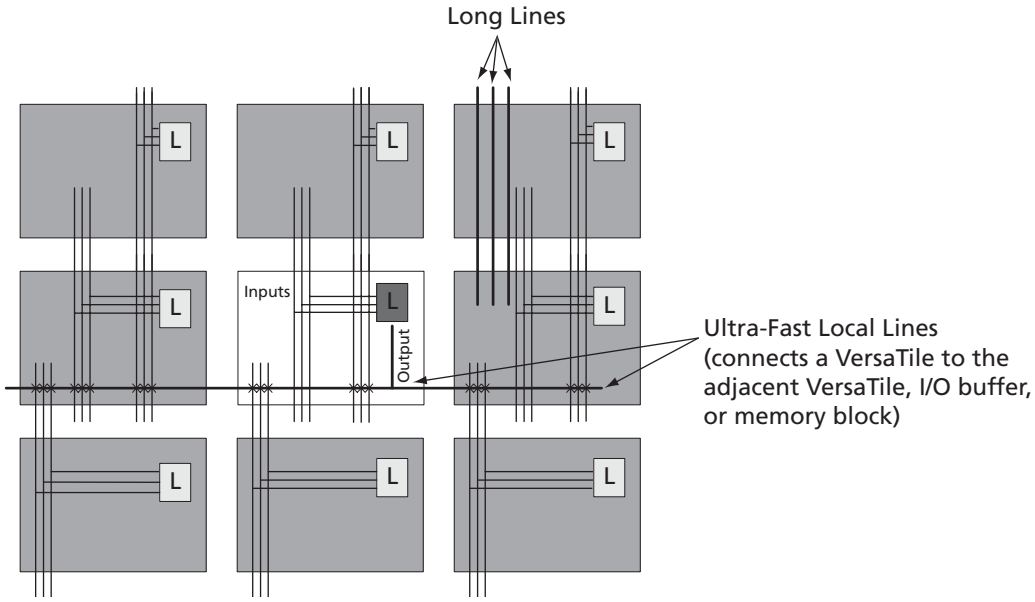
The routing structure of ProASIC3E devices is designed to provide high performance through a flexible four-level hierarchy of routing resources: ultra-fast local resources, efficient long-line resources, high-speed, very-long-line resources, and the high-performance VersaNet networks.

The ultra-fast local resources are dedicated lines that allow the output of each VersaTile to connect directly to every input of the eight surrounding VersaTiles (Figure 2-5). The exception to this is that the SET/CLR input of a VersaTile configured as a D-flip-flop is driven only by the VersaTile global network.

The efficient, long-line resources provide routing for longer distances and higher fanout connections. These resources vary in length (spanning one, two, or four VersaTiles), run both vertically and horizontally, and cover the entire ProASIC3E device (Figure 2-6 on page 2-6). Each VersaTile can drive signals onto the efficient long-line resources, which can access every input of every VersaTile. Active buffers are inserted automatically by routing software to limit the loading effects.

The high-speed, very-long-line resources, which span the entire device with minimal delay, are used to route very long or high-fanout nets: length +/–12 VersaTiles in the vertical direction and length +/–16 in the horizontal direction from a given core VersaTile (Figure 2-7 on page 2-7). Very long lines in ProASIC3E devices have been enhanced over those in previous ProASIC families. This provides a significant performance boost for long-reach signals.

The high-performance VersaNet global networks are low-skew, high-fanout nets that are accessible from external pins or from internal logic (Figure 2-8 on page 2-8). These nets are typically used to distribute clocks, resets, and other high-fanout nets requiring minimum skew. The VersaNet networks are implemented as clock trees, and signals can be introduced at any junction. These can be employed hierarchically, with signals accessing every input on all VersaTiles.



Note: *Input to the core cell for the D-flip-flop set and reset is only available via the VersaNet global network connection.*

Figure 2-5 • **Ultra-Fast Local Lines Connected to the Eight Nearest Neighbors**

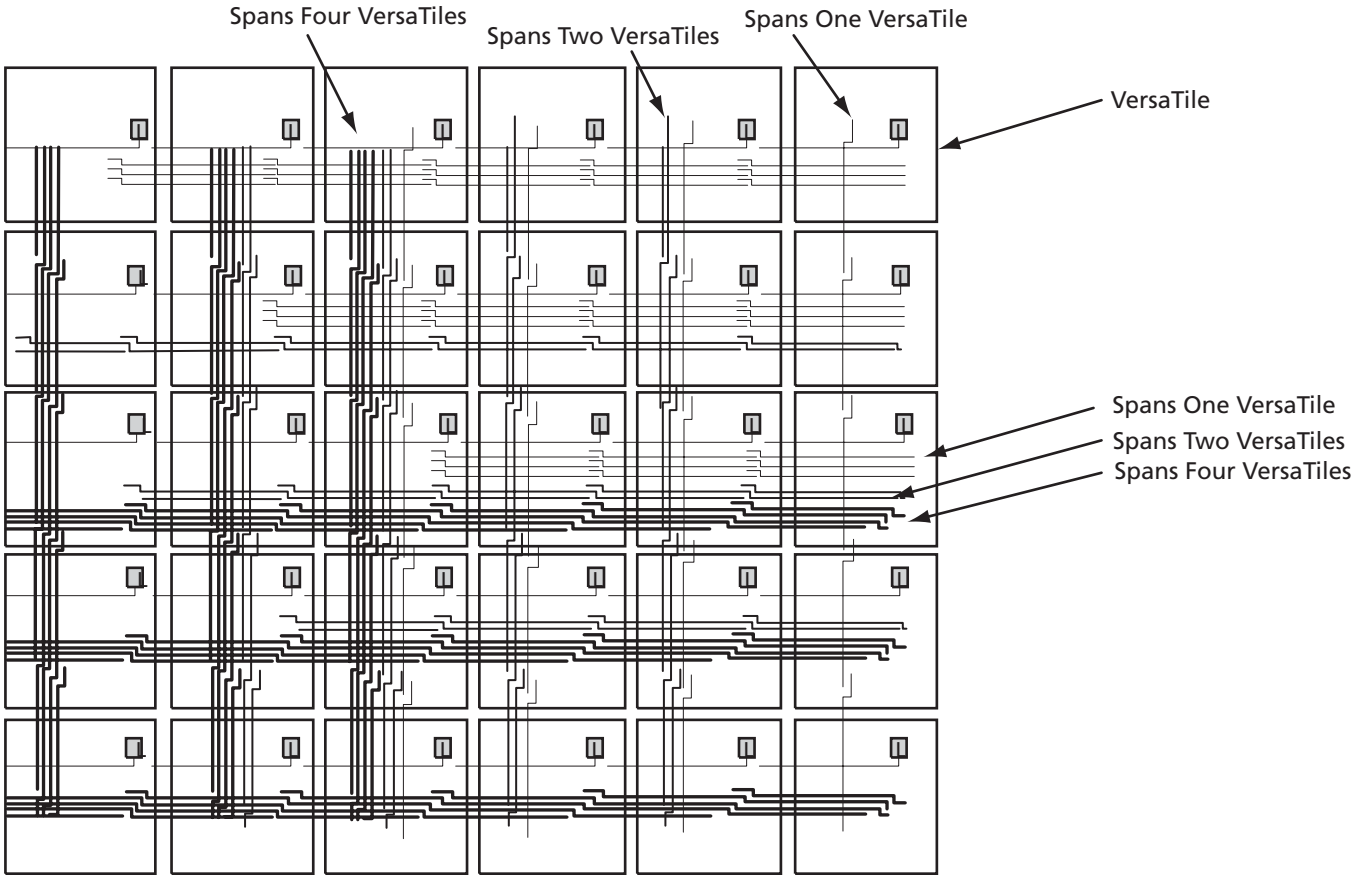


Figure 2-6 • **Efficient Long-Line Resources**

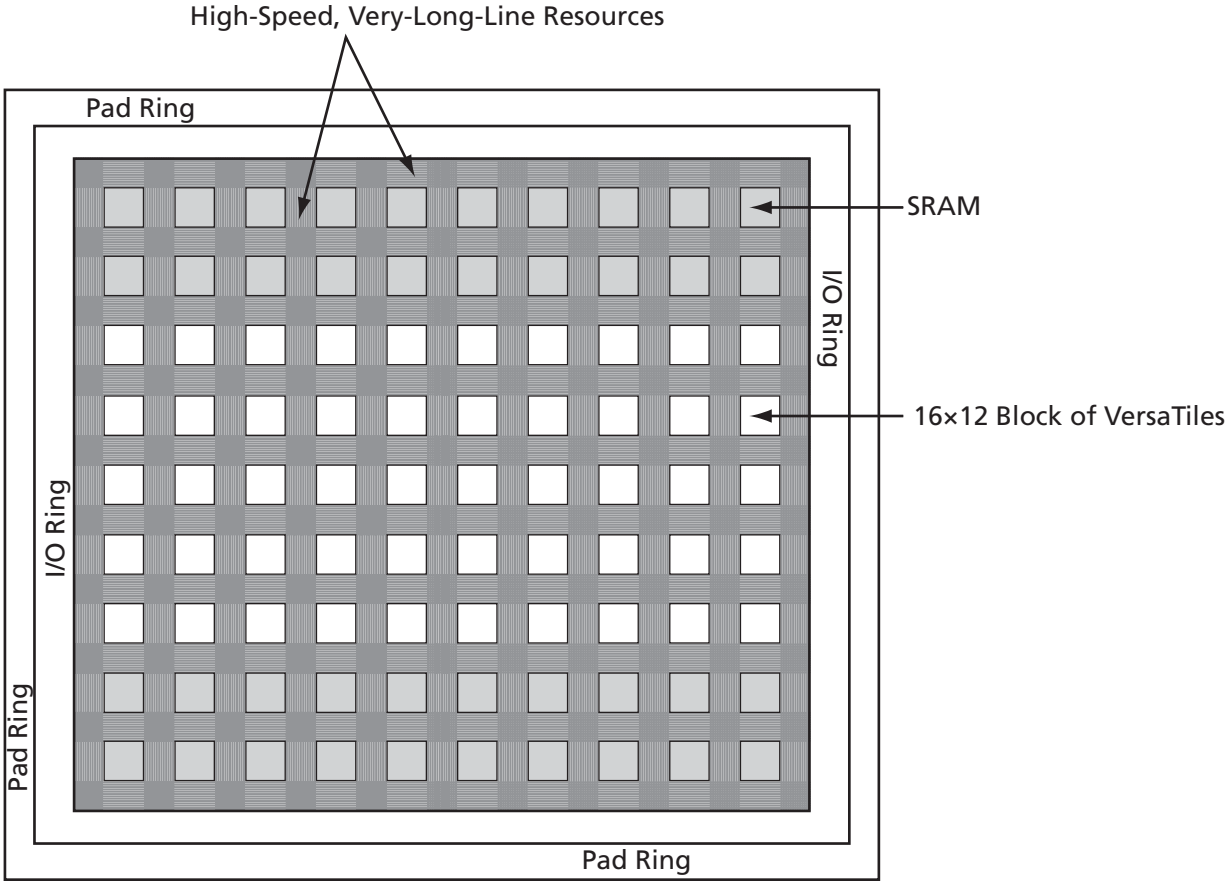


Figure 2-7 • **Very-Long-Line Resources**

Clock Resources (VersaNets)

ProASIC3E devices offer powerful and flexible control of circuit timing through the use of analog circuitry. Each chip has six CCCs containing a phase-locked loop (PLL) core, delay lines, a phase shifter (0°, 90°, 180°, 270°), clock multipliers/dividers, and all the circuitry needed for the selection and interconnection of inputs to the VersaNet global network. The east and west CCCs each have access to three VersaNet global lines on each side of the chip (six total lines). The CCCs at the four corners each have access to three quadrant global lines in each quadrant of the chip.

Advantages of the VersaNet Approach

One of the architectural benefits of ProASIC3E is the set of powerful and low-delay VersaNet global networks. ProASIC3E offers six chip (main) global networks that are distributed from the center of the FPGA array (Figure 2-8). In addition, ProASIC3E devices have three regional globals in each of the four chip quadrants. Each core VersaTile has access to nine global network resources: three quadrant and six chip (main) global networks, and a total of 18 globals on the device. Each of these networks contains spines and ribs that reach all the VersaTiles in the quadrants (Figure 2-9 on page 2-9). This flexible VersaNet global network architecture allows users to map up to 252 different internal/external clocks in a ProASIC3E device. Details on the VersaNet networks are given in Table 2-2 on page 2-9. The flexible use of the ProASIC3E VersaNet global network allows the designer to address several design requirements. User applications that are clock-resource-intensive can easily route external or gated internal clocks using VersaNet global routing networks. Designers can also drastically reduce delay penalties and minimize resource usage by mapping critical, high-fanout nets to the VersaNet global network.

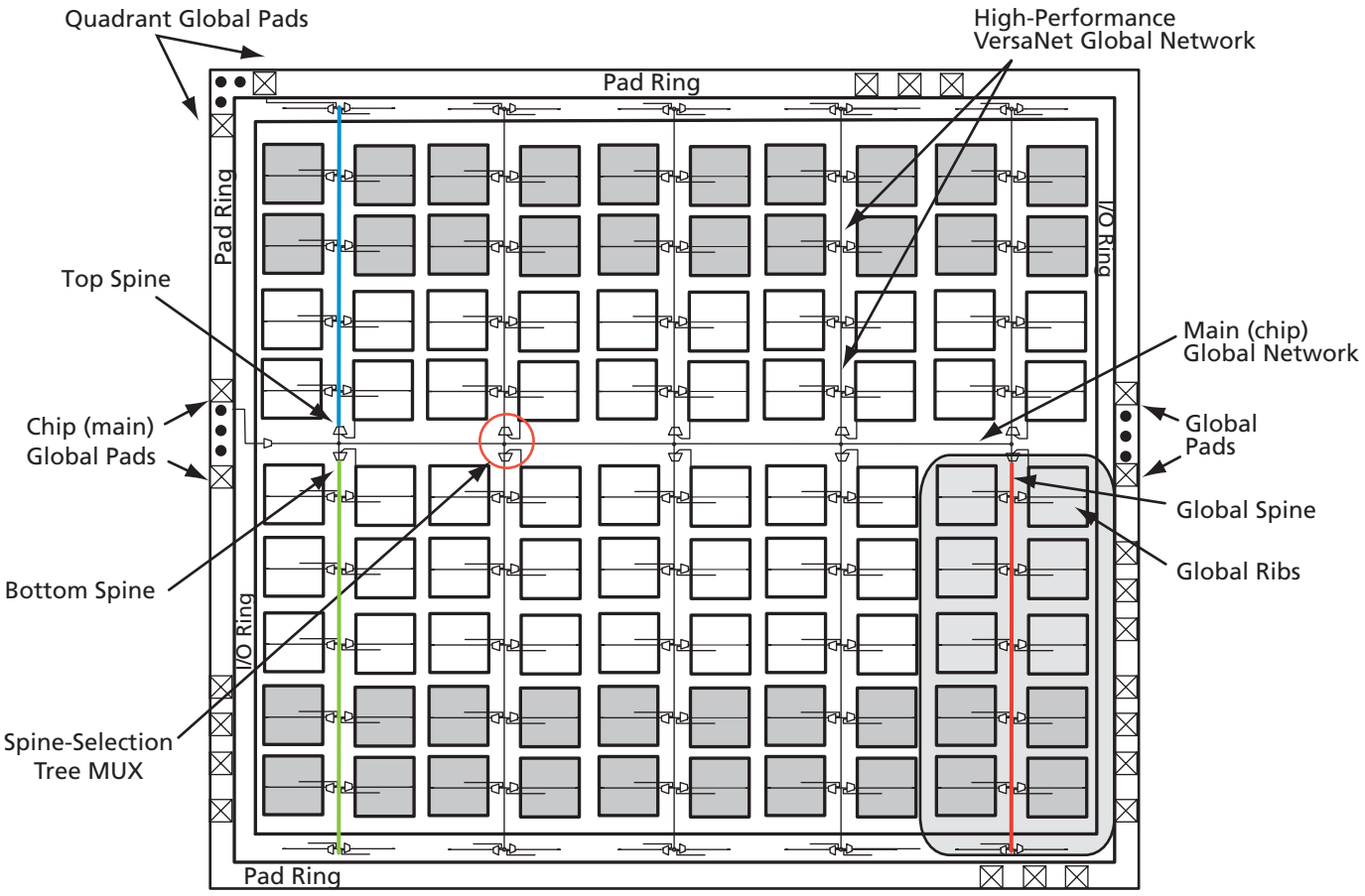


Figure 2-8 • **Overview of ProASIC3E VersaNet Global Network**

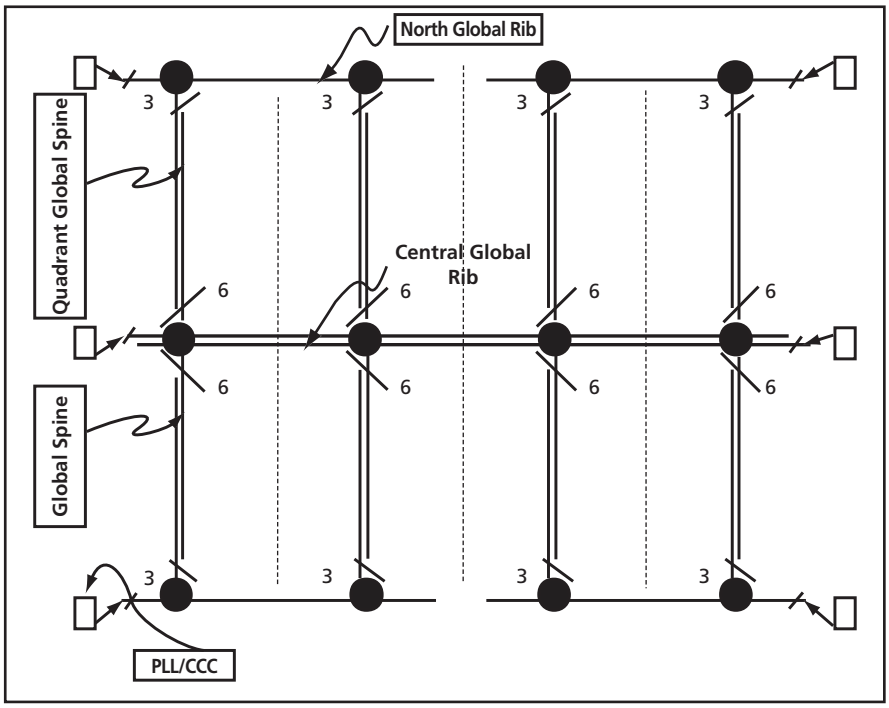


Figure 2-9 • **Global Network Architecture**

Table 2-2 • **ProASIC3E Globals/Spines/Rows by Device**

	A3PE600	A3PE1500	A3PE3000
Global Clock Networks (Trees)*	9	9	9
Clock Spines/Trees	12	20	28
Total Spines	108	180	252
VersaTiles in Each Top or Bottom Spine	1,120	1,888	2,656
Total VersaTiles	13,824	38,400	75,264
Rows in Each Top or Bottom Spine	36	60	84

Note: **There are six chip (main) globals and three globals per quadrant.*

VersaNet Global Networks and Spine Access

The ProASIC3E architecture contains a total of 18 segmented global networks that can access the VersaTiles, SRAM memory, and I/O tiles of the ProASIC3E device. There are nine global network resources in each device quadrant: three quadrant globals and six chip (main) global networks. Each device has a total of 18 globals. These VersaNet global networks offer fast, low-skew routing resources for high-fanout nets, including clock signals. In addition, these highly segmented global networks offer users the flexibility to create low-skew local networks using spines for up to 252 internal/external clocks (in an A3PE3000 device) or other high-fanout nets in ProASIC3E devices. Optimal usage of these low-skew networks can result in significant improvement in design performance on ProASIC3E devices.

The nine spines available in a vertical column reside in global networks with two separate regions of scope: the quadrant global network, which has three spines, and the chip (main) global network, which has six spines. Note that there are three quadrant spines in each quadrant of the device. There are four quadrant global network regions per device (Figure 2-9 on page 2-9).

The spines are the vertical branches of the global network tree, shown in Figure 2-10 on page 2-11. Each spine in a vertical column of a chip (main) global network is further divided into two equal-length spine segments: one in the top and one in the bottom half of the die.

Each spine and its associated ribs cover a certain area of the ProASIC3E device (the "scope" of the spine; see Figure 2-8 on page 2-8). Each spine is accessed by the dedicated global network MUX tree architecture, which defines how a particular spine is driven—either by the signal on the global network from a CCC, for example, or by another net defined by the user (Figure 2-11 on page 2-12). Quadrant spines can be driven from user I/Os on the north and south sides of the die. The ability to drive spines in the quadrant global networks can have a significant effect on system performance for high-fanout inputs to a design.

Details of the chip (main) global network spine-selection MUX are presented in Figure 2-11 on page 2-12. The spine drivers for each spine are located in the middle of the die.

Quadrant spines are driven from a north or south rib. Access to the top and bottom ribs is from the corner CCC or from the I/Os on the north and south sides of the device.

For details on using spines in ProASIC3E devices, see the Actel application note *Using Global Resources in Actel ProASIC3/E Devices*.

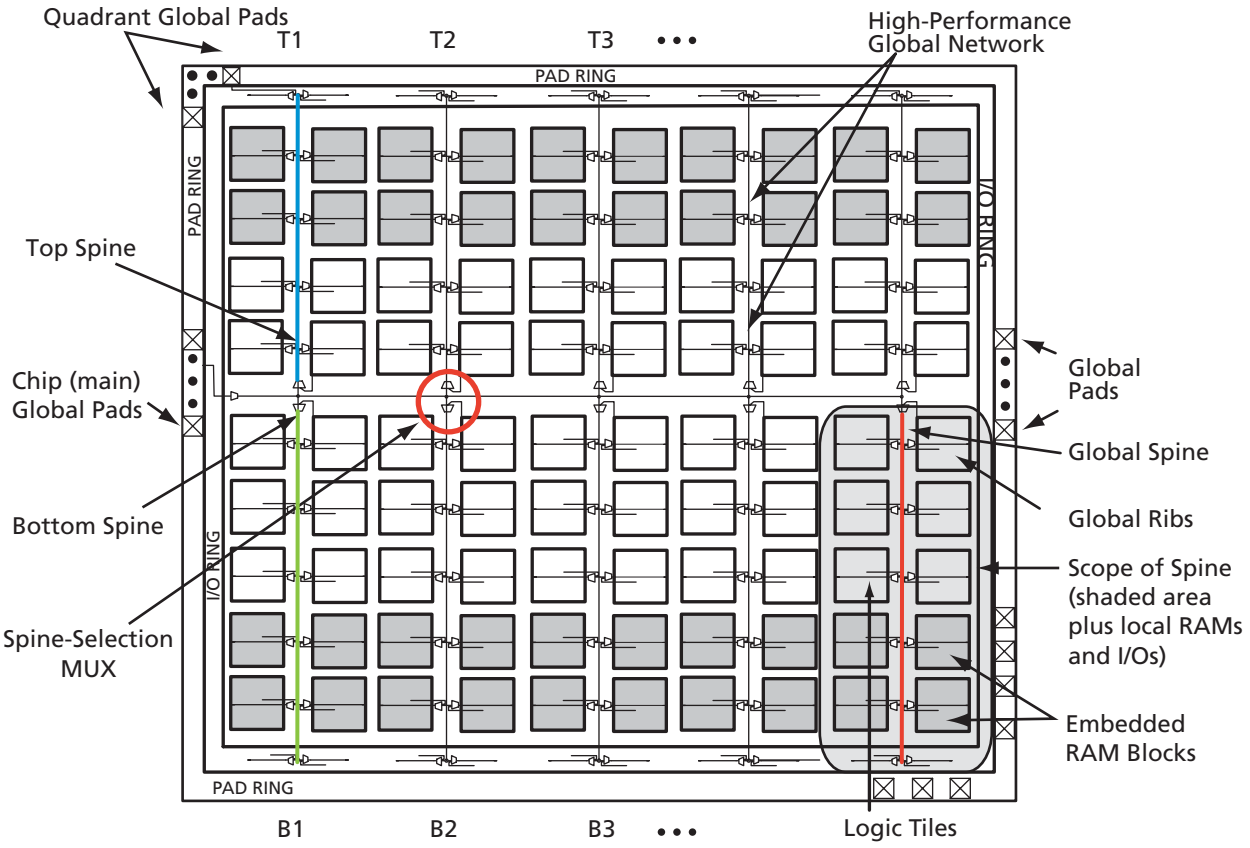


Figure 2-10 • **Spines in a Global Clock Tree Network**

Clock Aggregation

Clock aggregation allows for multi-spine clock domains. A MUX tree provides the necessary flexibility to allow long lines or I/Os to access domains of one, two, or four global spines. Signal access to the clock aggregation system is achieved through long-line resources in the central rib, and also through local resources in the north and south ribs, allowing I/Os to feed directly into the clock system. As Figure 2-12 indicates, this access system is contiguous.

There is no break in the middle of the chip for the north and south I/O VersaNet access. This is different from the quadrant clocks located in these ribs, which only reach the middle of the rib. Refer to the *Using Global Resources in Actel ProASIC3/E Devices* application note.

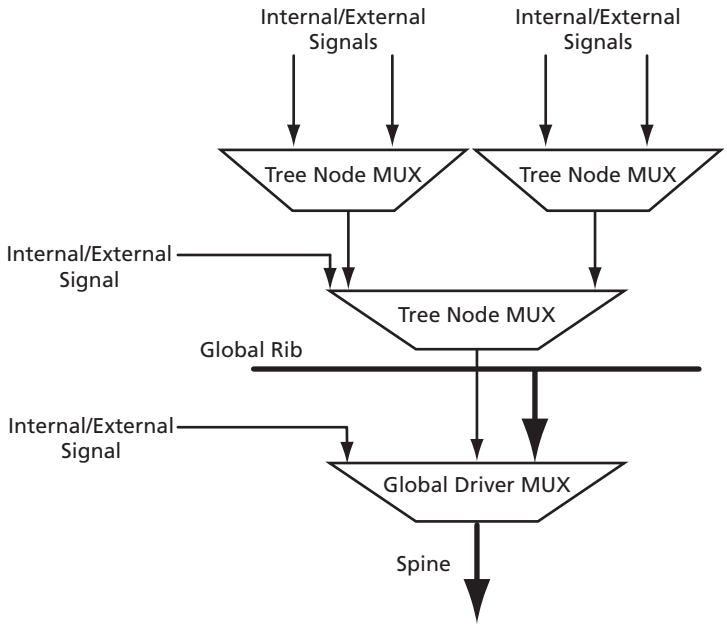


Figure 2-11 • **Spine Selection MUX of Global Tree**

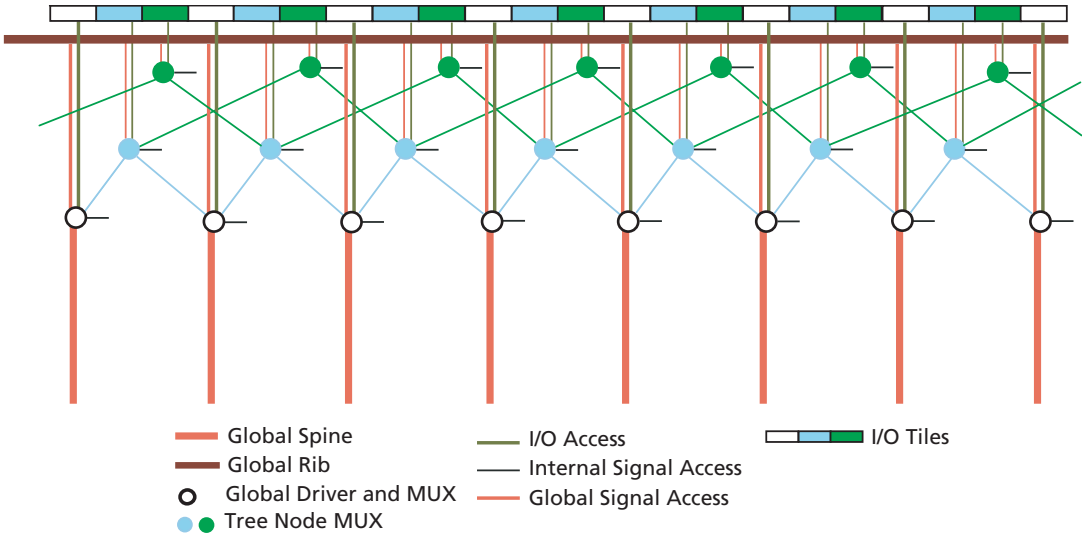


Figure 2-12 • **Clock Aggregation Tree Architecture**

Clock Conditioning Circuits

Overview of Clock Conditioning Circuitry

In ProASIC3E devices, the CCCs are used to implement frequency division, frequency multiplication, phase shifting, and delay operations.

The CCCs are available in six chip locations—each of the four chip corners and the middle of the east and west chip sides.

Each CCC can implement up to three independent global buffers (with or without programmable delay), or a PLL function (programmable frequency division/multiplication, phase shift, and delays) with up to three global outputs. Unused global outputs of a PLL can be used to implement independent global buffers, up to a maximum of three global outputs for a given CCC.

A global buffer can be placed in any of the three global locations (CLKA-GLA, CLKB-GLB, or CLKC-GLC) of a given CCC.

A PLL macro uses the CLKA CCC input to drive its reference clock. It uses the GLA and optionally the GLB and GLC global outputs to drive the global networks. A PLL macro can also drive the YB and YC regular core outputs. The GLB (or GLC) global output cannot be reused if the YB (or YC) output is used (Figure 2-13 on page 2-14). Refer to the "PLL Macro" section on page 2-15 for more information.

Each global buffer, as well as the PLL reference clock, can be driven from one of the following:

- Three dedicated single-ended I/Os using a hardwired connection
- Two dedicated differential I/Os using a hardwired connection
- The FPGA core

The CCC block is fully configurable, either via Flash configuration bits set in the programming bitstream or through an asynchronous interface. This asynchronous interface is dynamically accessible from inside the ProASIC3E device to permit parameter changes (such as divide ratios) during device operation. To increase the versatility and flexibility of the clock conditioning system, the CCC configuration is determined either by the user during the design process, with configuration data being stored in Flash memory as part of the device programming procedure, or by writing data into a dedicated shift register during normal device operation. This latter mode allows the user to dynamically reconfigure the CCC without the need for core programming. The shift register is accessed through a simple serial interface. Refer to the *UJTAG Applications in ProASIC3/E Devices* application note and the "CCC Electrical Specifications" section on page 2-18 for more information.

Global Buffers with No Programmable Delays

The CLKBUF and CLKBUF_LVPECL/LVDS/BLVDS/M-LVDS macros are composite macros that include an I/O macro driving a global buffer, which uses a hardwired connection.

The CLKBUF, CLKBUF_LVPECL/LVDS/BLVDS/M-LVDS, and CLKINT macros are pass-through clock sources and do not use the PLL or provide any programmable delay functionality.

The CLKINT macro provides a global buffer function driven by the FPGA core.

Many specific CLKBUF macros support the wide variety of single-ended and differential I/O standards supported by ProASIC3E devices. The available CLKBUF macros are described in the *Fusion and ProASIC3/E Macro Library Guide*.

Global Buffer with Programmable Delay

The CLKDLY macro is a pass-through clock source that does not use the PLL, but provides the ability to delay the clock input using a programmable delay. The CLKDLY macro takes the selected clock input and adds a user-defined delay element. This macro generates an output clock phase shift from the input clock.

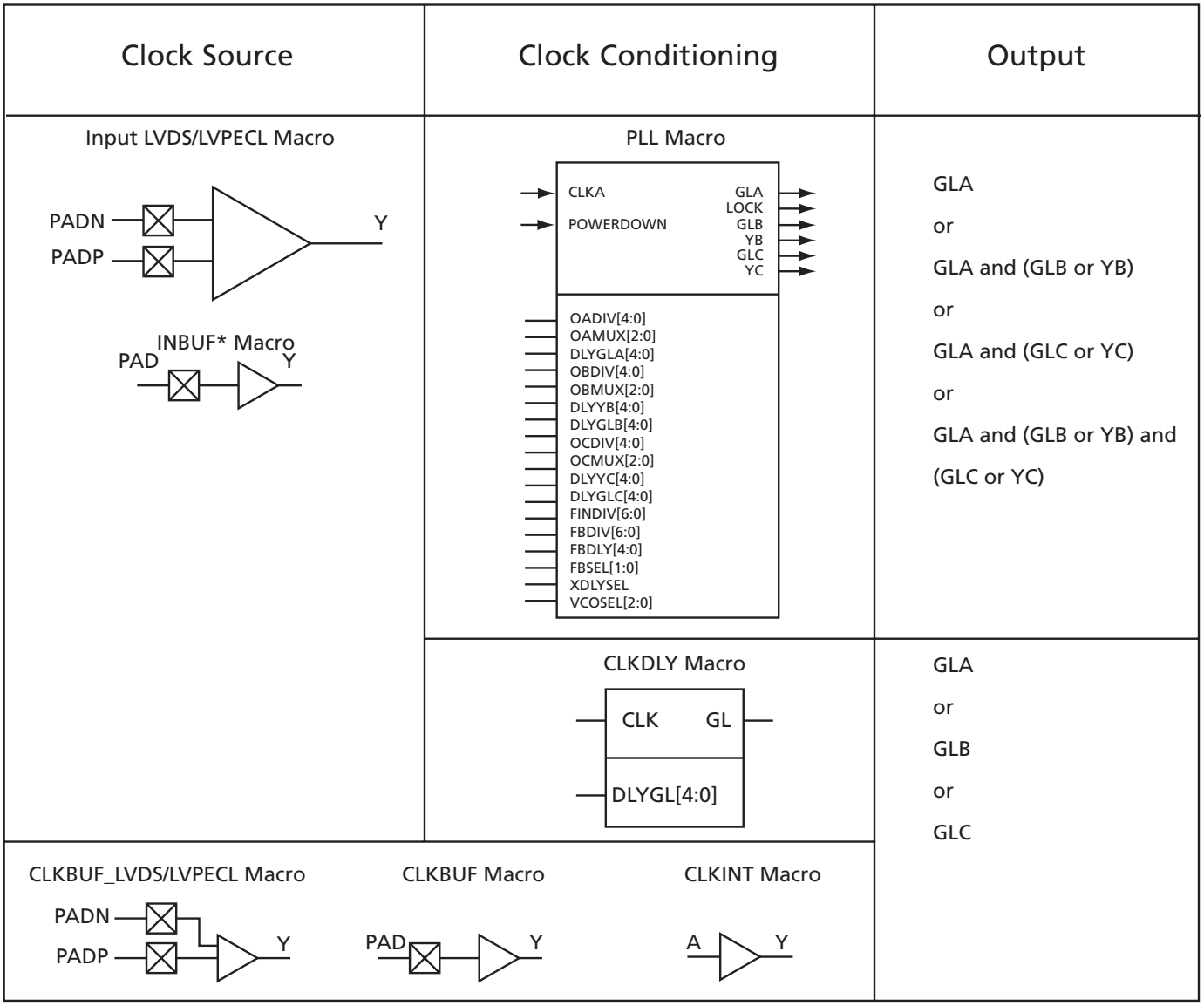
The CLKDLY macro can be driven by an INBUF* macro to create a composite macro, where the I/O macro drives the global buffer (with programmable delay) using a hardwired connection. In this case, the I/O must be placed in one of the dedicated global I/O locations.

Many specific INBUF macros support the wide variety of single-ended and differential I/O standards supported by the ProASIC3E family. The available INBUF macros are described in the *Fusion and ProASIC3/E Macro Library Guide*.

The CLKDLY macro can be driven directly from the FPGA core.

The CLKDLY macro can also be driven from an I/O that is routed through the FPGA regular routing fabric. In this case, users must instantiate a special macro, PLLINT, to differentiate from the hardwired I/O connection described earlier.

The visual CLKDLY configuration in the SmartGen part of the Libero IDE and Designer tools allows the user to select the desired amount of delay and configures the delay elements appropriately. SmartGen also allows the user to select the input clock source. SmartGen will automatically instantiate the special macro, PLLINT, when needed.



Notes:

1. *Visit the Actel website for future application notes concerning dynamic PLL reconfiguration. Refer to the "PLL Macro" section on page 2-15 for signal descriptions.*
2. *Refer to the* Fusion and ProASIC3/E Macro Library Guide *for more information.*
3. *Many standard-specific INBUF macros (for example, INBUF_LVDS) support the wide variety of single-ended and differential I/O standards supported by the ProASIC3E family. The available INBUF macros are described in the* Fusion and ProASIC3/E Macro Library Guide.

Figure 2-13 • **ProASIC3E CCC Options**

PLL Macro

The PLL functionality of the clock conditioning block is supported by the PLL macro. Note that the PLL macro reference clock uses the CLKA input of the CCC block, which is only accessible from the global A[0:2] package pins. Refer to Figure 2-14 on page 2-16 for more information.

The PLL macro provides five derived clocks (three independent) from a single reference clock. The PLL macro also provides power-down input and lock output signals. See Figure 2-16 on page 2-17 for more information.

Inputs:

- CLKA: selected clock input
- POWERDOWN (active low): disables PLLs. The default state is Powerdown On (active low).

Outputs:

- LOCK: indicates that PLL output has locked on the input reference signal
- GLA, GLB, GLC: outputs to respective global networks
- YB, YC: allows output from the CCC to be routed back to the FPGA core

As previously described, the PLL allows up to five flexible and independently configurable clock outputs. Figure 2-18 on page 2-19 illustrates the various clock output options and delay elements.

As illustrated, the PLL supports three distinct output frequencies from a given input clock. Two of these (GLB and GLC) can be routed to the B and C global network access, respectively, and/or routed to the device core (YB and YC).

There are five delay elements to support phase control on all five outputs (GLA, GLB, GLC, YB, and YC).

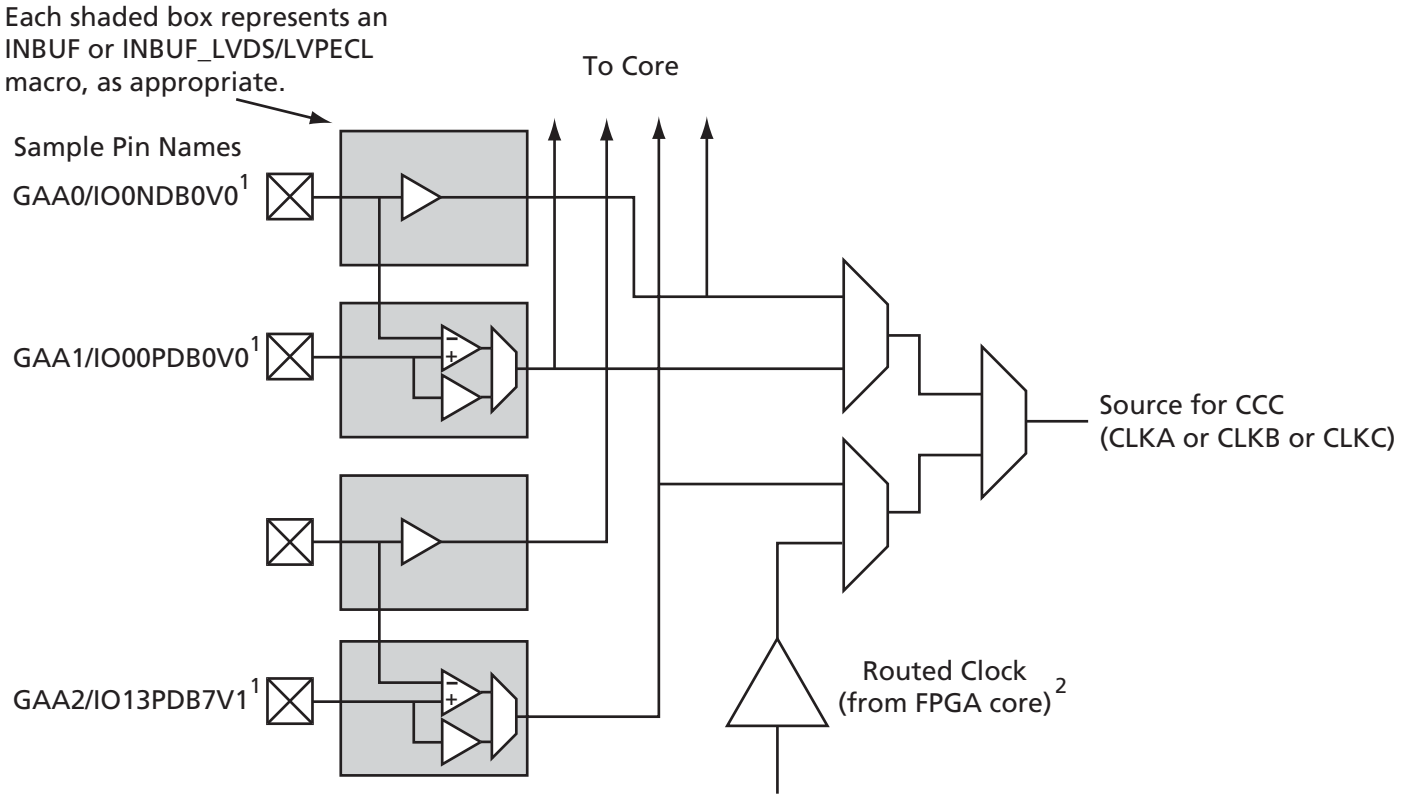
There is also a delay element in the feedback loop that can be used to advance the clock relative to the reference clock.

The PLL macro reference clock can be driven by an INBUF* macro to create a composite macro, where the I/O macro drives the global buffer (with programmable delay) using a hardwired connection. In this case, the I/O must be placed in one of the dedicated global I/O locations.

The PLL macro reference clock can be driven directly from the FPGA core.

The PLL macro reference clock can also be driven from an I/O that is routed through the FPGA regular routing fabric. In this case, users must instantiate a special macro, PLLINT, to differentiate from the hardwired I/O connection described earlier.

The visual PLL configuration in SmartGen, part of the Libero IDE and Designer tools, will derive the necessary internal divider ratios based on the input frequency and desired output frequencies selected by the user. SmartGen also allows the user to select the various delays and phase shift values necessary to adjust the phases between the reference clock (CLKA) and the derived clocks (GLA, GLB, GLC, YB, and YC). SmartGen also allows the user to select the input clock source. SmartGen automatically instantiates the special macro, PLLINT, when needed.



Notes:

1. *Represents the global input pins. Globals have direct access to the clock conditioning block and are not routed via the FPGA fabric. Refer to the "User I/O Naming Convention" section on page 2-50 for more information.*
2. *Instantiate the routed clock source input as follows:*
   a) Connect the output of a logic element to the clock input of a PLL, CLKDLY, or CLKINT macro.
   b) Do not place a clock source I/O (INBUF or INBUF_LVPECL/LVDS/BLVDS/M-LVDS/DDR) in a relevant global pin location.

Figure 2-14 • **Clock Input Sources Including CLKBUF, CLKBUF_LVDS/LVPECL, and CLKINT**

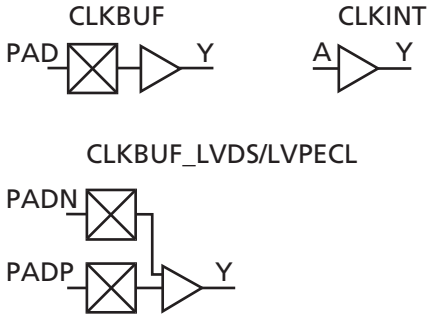


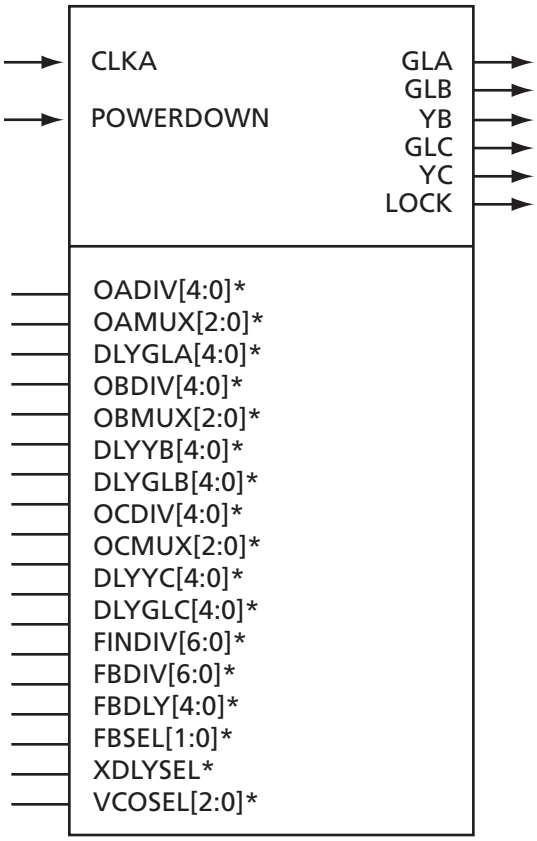
Figure 2-15 • **CLKBUF and CLKINT**

Table 2-3 • **Available I/O Standards within CLKBUF and CLKBUF_LVDS/LVPECL Macros**

CLKBUF Macros
CLKBUF_LVCMOS5
CLKBUF_LVCMOS33 [1]
CLKBUF_LVCMOS25
CLKBUF_LVCMOS18
CLKBUF_LVCMOS15
CLKBUF_PCI
CLKBUF_PCIX
CLKBUF_GTL25
CLKBUF_GTL33
CLKBUF_GTLP25
CLKBUF_GTLP33
CLKBUF_HSTL_I
CLKBUF_HSTL_II
CLKBUF_SSTL3_I
CLKBUF_SSTL3_II
CLKBUF_SSTL2_I
CLKBUF_SSTL2_II
CLKBUF_LVDS [2]
CLKBUF_LVPECL

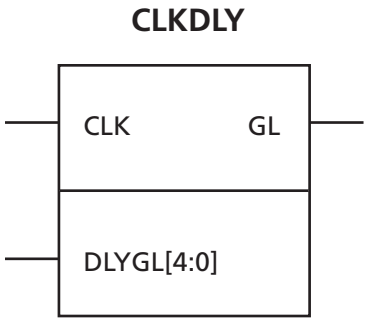
Notes:

1. *By default, the CLKBUF macro uses the 3.3 V LVTTL I/O technology. For more details, refer to the Fusion and ProASIC3/E Macro Library Guide.*
2. *BLVDS and M-LVDS standards are supported by CLKBUF_LVDS.*



Note: **Visit the Actel website for future application notes concerning the dynamic PLL.*

Figure 2-16 • **CCC/PLL Macro**



Note: *The CLKDLY macro uses programmable delay element type 2.*

Figure 2-17 • **CLKDLY**

CCC Electrical Specifications

Timing Characteristics

Table 2-4 • **ProASIC3E CCC/PLL Specification**

Parameter	Min.	Typ.	Max.	Unit
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}	1.5		350	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}	0.75		350	MHz
Delay Increments in Programmable Delay Blocks[1, 2]		200		ps
Number of Programmable Values in Each Programmable Delay Block			32	
Input Period Jitter			1.5	ns
CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT}	Max Peak-to-Peak Period Jitter			
	1 Global Network Used		3 Global Networks Used	
0.75 MHz to 24 MHz	0.50		0.70	%
24 MHz to 100 MHz	1.00		1.20	%
100 MHz to 250 MHz	1.75		2.00	%
250 MHz to 350 MHz	2.50		5.60	%
Acquisition Time			150	µs
Output Duty Cycle	48.5		51.5	%
Delay Range in Block: Programmable Delay 1 [1, 2]	0.6		5.56	ns
Delay Range in Block: Programmable Delay 2 [1, 2]	0.025		5.56	ns
Delay Range in Block: Fixed Delay [1, 2]		2.2		ns

Notes:

1. *This delay is a function of voltage and temperature. See Table 3-6 on page 3-4 for deratings.*
2. *T_J = 25°C, V_{CC} = 1.5 V*

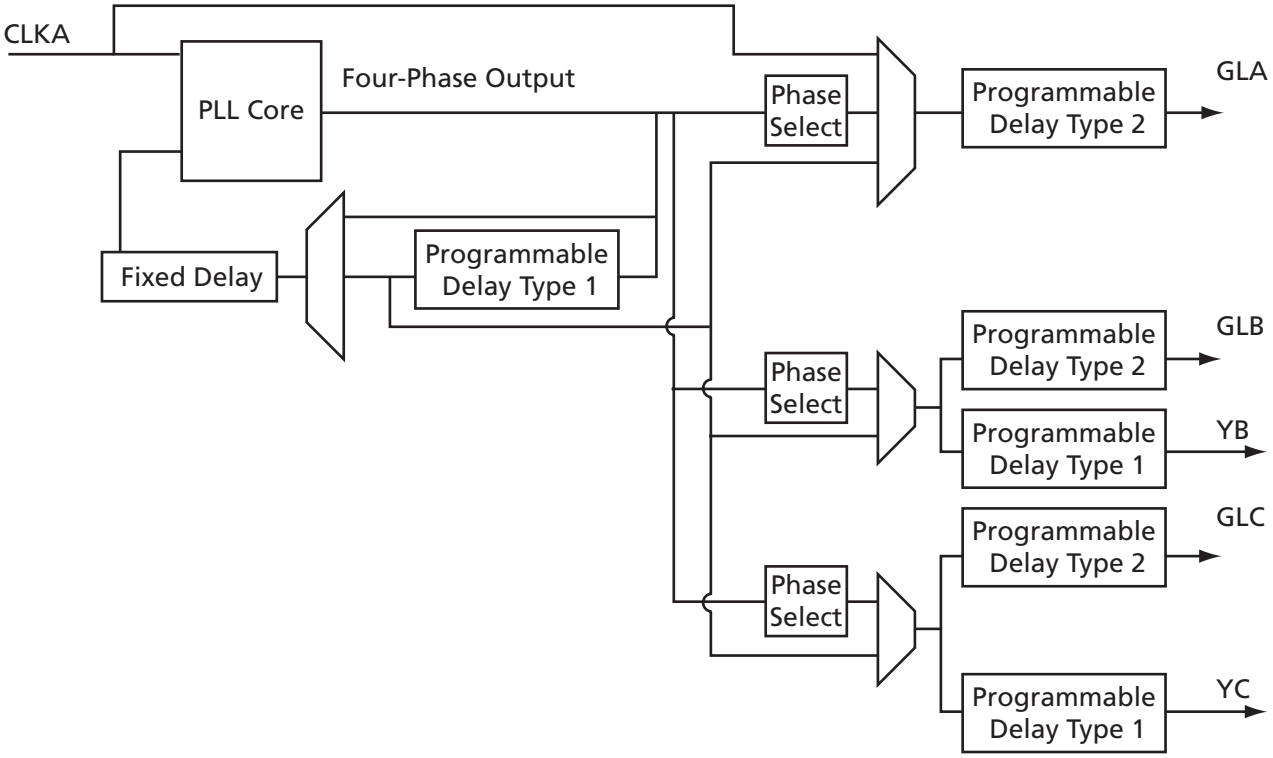
CCC Physical Implementation

The CCC is composed of the following (Figure 2-18):

- PLL core
- Three phase selectors
- Six programmable delays and one fixed delay that advance/delay phase
- Five programmable frequency dividers that provide frequency multiplication/division (not shown in Figure 2-18, because they are automatically configured based on the user's required frequencies)
- One dynamic shift register that provides CCC dynamic reconfiguration capability

CCC Programming

The CCC block is fully configurable, either via static Flash configuration bits in the array, set by the user in the programming bitstream, or through an asynchronous dedicated shift register dynamically accessible from inside the ProASIC3E device. The dedicated shift register permits parameter changes such as PLL divide ratios and delays during device operation. This latter mode allows the user to dynamically reconfigure the PLL without the need for core programming. The register file is accessed through a simple serial interface. Refer to the *UJTAG Applications in ProASIC3/E Devices* application note for more information.



Notes:

1. *Refer to the "Clock Conditioning Circuits" section on page 2-13 and Table 2-4 on page 2-18 for signal descriptions.*
2. *Clock divider and clock multiplier blocks are not shown in this figure or in SmartGen. They are automatically configured based on the user's required frequencies.*

Figure 2-18 • **PLL Block**

Nonvolatile Memory (NVM)

Overview of User Nonvolatile FlashROM

ProASIC3E devices have 1 kbit of on-chip nonvolatile Flash memory that can be read from the FPGA core fabric. The FlashROM is arranged in 8 banks of 128 bits during programming. The 128 bits in each bank are addressable as 16 bytes during the read back of the FlashROM from the FPGA core (Figure 2-19).

The FlashROM can only be programmed via the IEEE1532 JTAG port. It cannot be programmed directly from the FPGA core. When programming, each of the 8 128-bit banks can be selectively reprogrammed. The FlashROM can only be reprogrammed on a bank boundary. Programming involves an automatic, on-chip bank erase prior to reprogramming the bank. The FlashROM supports synchronous read. The address is latched on the rising edge of the clock and the new output data is stable after the falling edge of the same clock cycle. Please refer to Figure 3-51 on page 3-76 for the timing diagram. The FlashROM can be read on byte boundaries. The upper 3 bits of the FlashROM address from the FPGA core define the bank that is being accessed. The lower 4 bits of the FlashROM address from the FPGA core define which of the 16 bytes in the bank is being accessed.

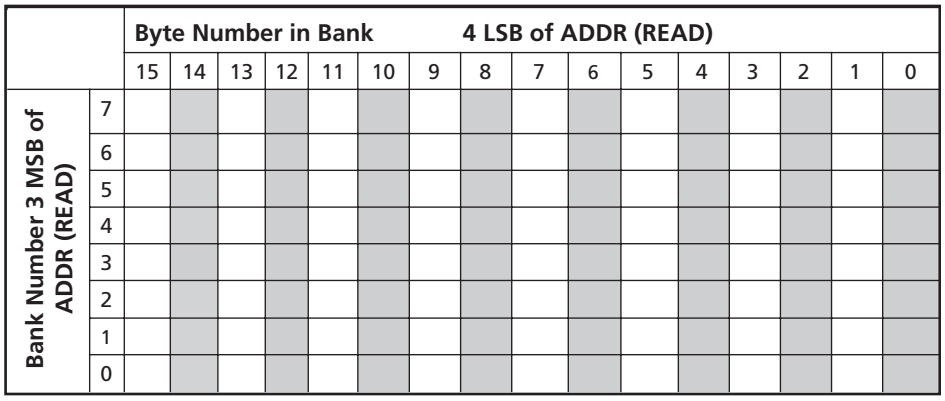


Figure 2-19 • **FlashROM Architecture**

SRAM and FIFO

ProASIC3E devices have embedded SRAM blocks along the north and south sides of the device. To meet the needs of high-performance designs, the memory blocks operate strictly in synchronous mode for both read and write operations. The read and write clocks are completely independent, and each may operate at any desired frequency less than or equal to 350 MHz.

- 4kx1, 2kx2, 1kx4, 512x9 (dual-port RAM—two read, two write or one read, one write)
- 512x9, 256x18 (two-port RAM—one read and one write)
- Sync write, sync pipelined / nonpipelined read

The ProASIC3E memory block includes dedicated FIFO control logic to generate internal addresses and external flag logic (FULL, EMPTY, AFULL, AEMPTY). Block diagrams of the memory modules are illustrated in Figure 2-20 on page 2-22.

During RAM operation, addresses are sourced by the user logic and the FIFO controller is ignored. In FIFO mode, the internal addresses are generated by the FIFO controller and routed to the RAM array by internal MUXes. Refer to Figure 2-21 on page 2-23 for more information about the implementation of the embedded FIFO controller.

The ProASIC3E architecture enables the read and write sizes of RAMs to be organized independently, allowing for bus conversion. For example, the write side size can be set to 256x18 and the read size to 512x9.

Both the write width and read width for the RAM blocks can be specified independently with the WW (write width) and RW (read width) pins. The different DxW configurations are: 256x18, 512x9, 1kx4, 2kx2, and 4kx1.

Refer to the allowable RW and WW values supported for each of the RAM macro types in Table 2-5 on page 2-24.

When widths of one, two, or four are selected, the ninth bit is unused. For example, when writing nine-bit values and reading four-bit values, only the first four bits and the second four bits of each nine-bit value are addressable for read operations. The ninth bit is not accessible.

Conversely, when writing four-bit values and reading nine-bit values, the ninth bit of a read operation will be undefined. The RAM blocks employ little-endian byte order for read and write operations.

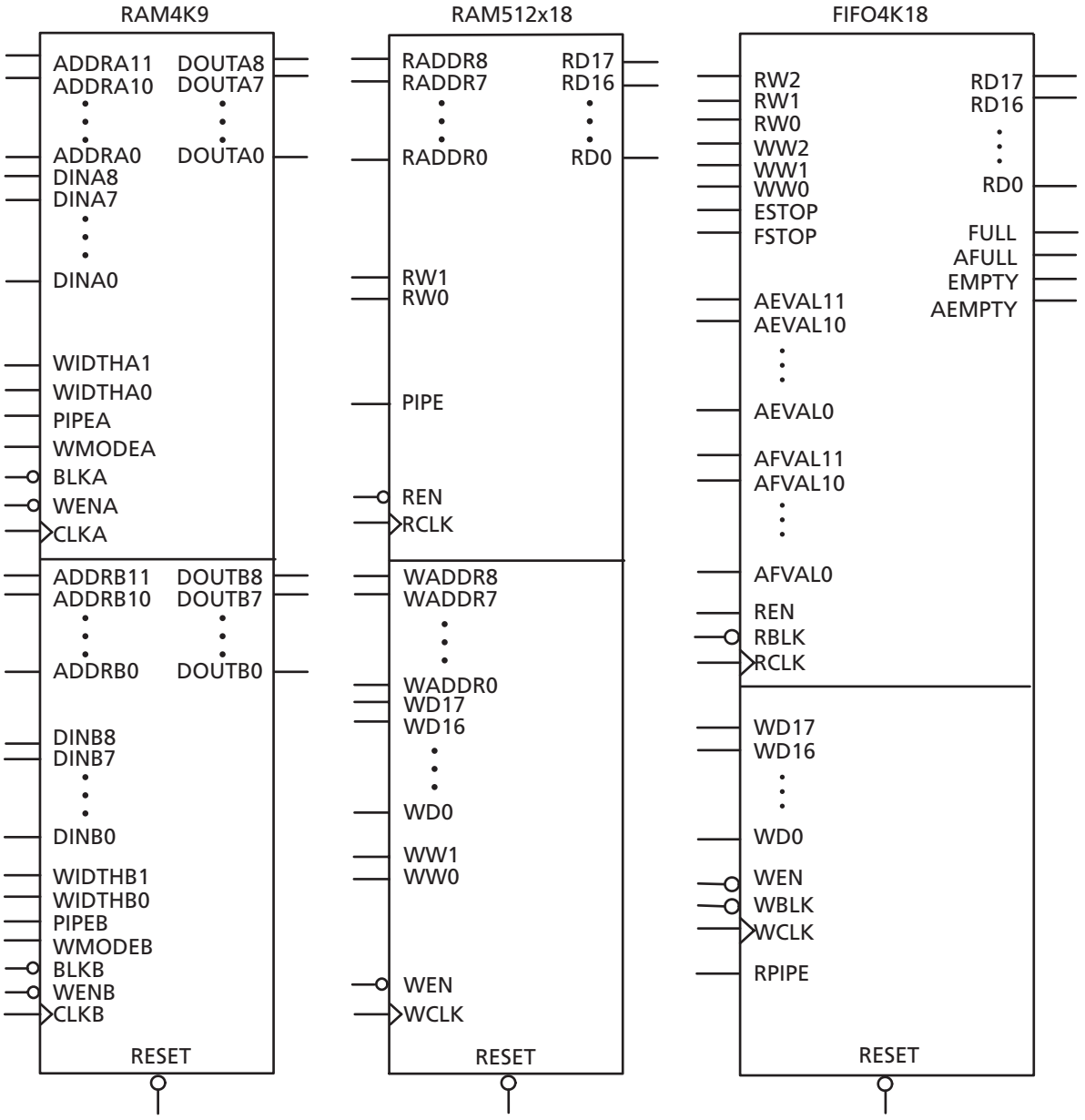


Figure 2-20 • **Supported Basic RAM Macros**

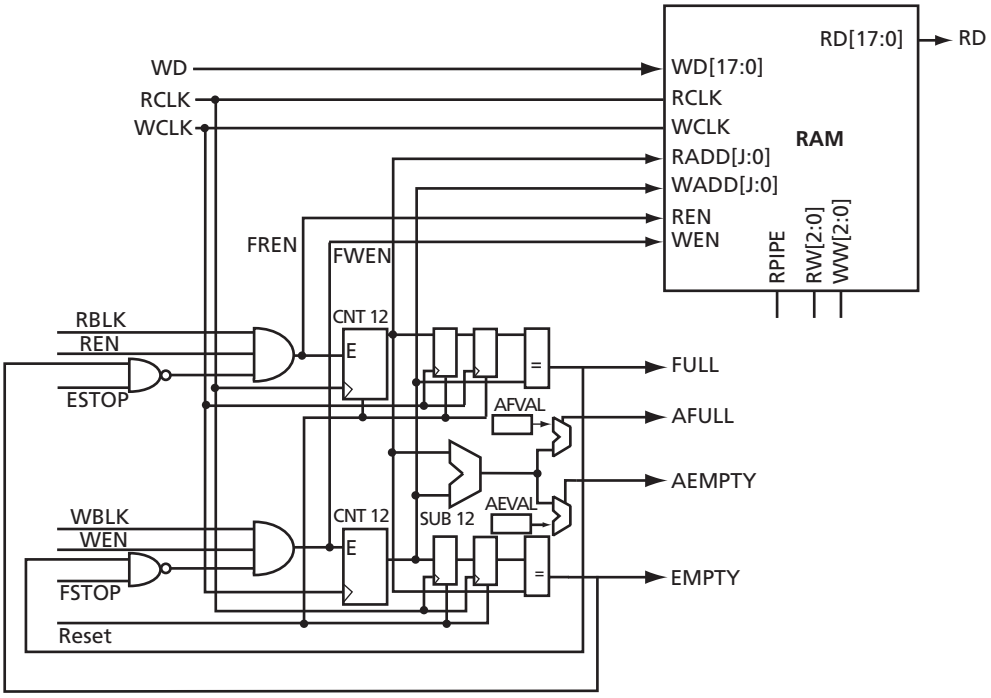


Figure 2-21 • **ProASIC3E RAM Block with Embedded FIFO Controller**

Signal Descriptions for RAM4K9

The following signals are used to configure the RAM4K9 memory element:

WIDTHA and WIDTHB

These signals enable the RAM to be configured in one of four allowable aspect ratios (Table 2-5).

Table 2-5 • **Allowable Aspect Ratio Settings for WIDTHA[1:0]**

WIDTHA[1:0]	WIDTHB[1:0]	DxW
00	00	4kx1
01	01	2kx2
10	10	1kx4
11	11	512x9

Note: *The aspect ratio settings are constant and cannot be changed on-the-fly.*

BLKA and BLKB

These signals are active low and will enable the respective ports when asserted. When a BLKx signal is deasserted, that port's outputs hold the previous value.

WENA and WENB

These signals switch the RAM between read and write modes for the respective ports. A low on these signals indicates a write operation, and a high indicates a read.

CLKA and CLKB

These are the clock signals for the synchronous read and write operations. These can be driven independently or with the same driver.

PIPEA and PIPEB

These signals are used to specify pipelined read on the output. A low on PIPEA or PIPEB indicates a nonpipelined read, and the data appears on the corresponding output in the same clock cycle. A high indicates a pipelined read, and data appears on the corresponding output in the next clock cycle.

WMODEA and WMODEB

These signals are used to configure the behavior of the output when RAM is in the write mode. A low on these signals makes the output retain data from the previous read. A high indicates pass-through behavior, wherein the data being written will appear immediately on the output. This signal is overridden when the RAM is being read.

RESET

This active low signal resets the control logic and forces the output hold state registers to zero when asserted. It does not reset the contents of the memory array.

While the RESET signal is active, read and write operations are disabled. As with any asynchronous reset signal, care must be taken not to assert it too close to the edges of active read and write clocks. Refer to the tables beginning with Table 3-94 on page 3-71 for the specifications.

ADDRA and ADDRB

These are used as read or write addresses, and they are 12 bits wide. When a depth of less than 4 k is specified, the unused high-order bits must be grounded (Table 2-6).

Table 2-6 • **Address Pins Unused/Used for Various Supported Bus Widths**

	ADDRx	
DxW	Unused	Used
4kx1	None	[11:0]
2kx2	[11]	[10:0]
1kx4	[11:10]	[9:0]
512x9	[11:9]	[8:0]

Note: *The "x" in ADDRx implies A or B.*

DINA and DINB

These are the input data signals, and they are nine bits wide. Not all nine bits are valid in all configurations. When a data width less than nine is specified, unused high-order signals must be grounded (Table 2-7).

DOUTA and DOUTB

These are the nine-bit output data signals. Not all nine bits are valid in all configurations. As with DINA and DINB, high-order bits may not be used (Table 2-7). The output data on unused pins is undefined.

Table 2-7 • **Unused/Used Input and Output Data Pins for Various Supported Bus Widths**

	DINx/DOUTx	
DxW	Unused	Used
4kx1	[8:1]	[0]
2kx2	[8:2]	[1:0]
1kx4	[8:4]	[3:0]
512x9	None	[8:0]

Note: *The "x" in DINx or DOUTx implies A or B.*

Signal Descriptions for RAM512X18

RAM512X18 has slightly different behavior than the RAM4K9, as it has dedicated read and write ports.

WW and RW

These signals enable the RAM to be configured in one of the two allowable aspect ratios (Table 2-8).

Table 2-8 • **Aspect Ratio Settings for WW[1:0]**

WW[1:0]	RW[1:0]	DxW
01	01	512x9
10	10	256x18
00, 11	00, 11	Reserved

WD and RD

These are the input and output data signals, and they are 18 bits wide. When a 512x9 aspect ratio is used for write, WD[17:9] are unused and must be grounded. If this aspect ratio is used for read, RD[17:9] are undefined.

WADDR and RADDR

These are read and write addresses, and they are nine bits wide. When the 256x18 aspect ratio is used for write or read, WADDR[8] or RADDR[8] are unused and must be grounded.

WCLK and RCLK

These signals are the write and read clocks, respectively. They can be clocked on the rising edge or falling edge of WCLK and RCLK.

WEN and REN

These signals are the write and read enables, respectively. They are both active low by default. These signals can be configured as active high.

RESET

This active low signal resets the control logic and forces the output hold state registers to zero when asserted. It does not reset the contents of the memory array.

While the RESET signal is active, read and write operations are disabled. As with any asynchronous reset signal, care must be taken not to assert it too close to the edges of active read and write clocks. Refer to the tables beginning with Table 3-95 on page 3-71 for the specifications.

PIPE

This signal is used to specify pipelined read on the output. A low on PIPE indicates a nonpipelined read, and the data appears on the output in the same clock cycle. A high indicates a pipelined read, and data appears on the output in the next clock cycle.

Clocking

The dual-port SRAM blocks are only clocked on the rising edge. SmartGen allows falling-edge triggered clocks by adding inverters to the netlist, hence achieving dual-port SRAM blocks that are clocked on either edge (rising or falling). For dual-port SRAM, each port can be clocked on either edge and/or by separate clocks by port.

ProASIC3E devices support inversion (bubble pushing) throughout the FPGA architecture, including the clock input to the SRAM modules. Inversions added to the SRAM clock pin on the design schematic or in the HDL code will be automatically accounted for during design compile without incurring additional delay in the clock path.

The two-port SRAM can be clocked on the rising edge or falling edge of the WCLK and RCLK.

If negative-edge RAM and FIFO clocking is selected for memory macros, clock edge inversion management (bubble pushing) is automatically used within the ProASIC3E development tools, without performance penalty.

Modes of Operation

There are two read modes and one write mode:

- Read Nonpipelined (synchronous—one clock edge): In the standard read mode, new data is driven onto the RD bus in the same clock cycle following RA and REN valid. The read address is registered on the read port clock active edge and data appears at RD after the RAM access time. Setting PIPE to OFF enables this mode.
- Read Pipelined (synchronous—two clock edges): The pipelined mode incurs an additional clock delay from the address to the data but enables operation at a much higher frequency. The read address is registered on the read port active clock edge, and the read data is registered and appears at RD after the second read clock edge. Setting the PIPE to ON enables this mode.
- Write (synchronous—one clock edge): On the write clock active edge, the write data is written into the SRAM at the write address when WEN is high. The setup times of the write address, write enables, and write data are minimal with respect to the write clock. Write and read transfers are described with timing requirements in the "DDR Module Specifications" section on page 3-56.

RAM Initialization

Each SRAM block can be individually initialized on power-up by means of the JTAG port using the UJTAG mechanism (refer to the "JTAG 1532" section on page 2-54 and the *ProASIC3/E SRAM/FIFO Blocks* application note). The shift register for a target block can be selected and loaded with the proper bit configuration to enable serial loading. The 4,608 bits of data can be loaded in a single operation.

Signal Descriptions for FIFO4K18

The following signals are used to configure the FIFO4K18 memory element:

WW and RW

These signals enable the FIFO to be configured in one of the five allowable aspect ratios (Table 2-9).

Table 2-9 • **Aspect Ratio Settings for WW[2:0]**

WW[2:0]	RW[2:0]	DxW
000	000	4kx1
001	001	2kx2
010	010	1kx4
011	011	512x9
100	100	256x18
101, 110, 111	101, 110, 111	Reserved

WBLK and RBLK

These signals are active low and will enable the respective ports when low. When the RBLK signal is high, that port's outputs hold the previous value.

WEN and REN

Read and write enables. WEN is active low and REN is active high by default. These signals can be configured as active high or low.

WCLK and RCLK

These are the clock signals for the synchronous read and write operations. These can be driven independently or with the same driver.

RPIPE

This signal is used to specify pipelined read on the output. A low on RPIPE indicates a nonpipelined read, and the data appears on the output in the same clock cycle. A high indicates a pipelined read, and data appears on the output in the next clock cycle.

RESET

This active low signal resets the control logic and forces the output hold state registers to zero when asserted. It does not reset the contents of the memory array (Table 2-10).

While the RESET signal is active, read and write operations are disabled. As with any asynchronous RESET signal, care must be taken not to assert it too close to the edges of active read and write clocks. Refer to the tables beginning with Table 3-96 on page 3-75 for the specifications.

WD

This is the input data bus and is 18 bits wide. Not all 18 bits are valid in all configurations. When a data width less than 18 is specified, unused higher-order signals must be grounded (Table 2-10).

RD

This is the output data bus and is 18 bits wide. Not all 18 bits are valid in all configurations. Like the WD bus, high-order bits become unusable if the data width is less than 18. The output data on unused pins is undefined (Table 2-10).

Table 2-10 • **Input Data Signal Usage for Different Aspect Ratios**

DxW	WD/RD Unused
4kx1	WD[17:1], RD[17:1]
2kx2	WD[17:2], RD[17:2]
1kx4	WD[17:4], RD[17:4]
512x9	WD[17:9], RD[17:9]
256x18	–

ESTOP, FSTOP

ESTOP is used to stop the FIFO read counter from further counting once the FIFO is empty (i.e., the Empty flag goes high). A high on this signal inhibits the counting.

FSTOP is used to stop the FIFO write counter from further counting once the FIFO is full (i.e., the Full flag goes high). A high on this signal inhibits the counting.

For more information on these signals, refer to the "ESTOP and FSTOP Usage" section on page 2-27.

FULL, EMPTY

When the FIFO is full and no more data can be written, the Full flag asserts high. The Full flag is synchronous to WCLK to inhibit writing immediately upon detection of a full condition and to prevent overflows. Since the write address is compared to a resynchronized (and thus time-delayed) version of the read address, the Full flag will remain asserted until two WCLK active edges after a read operation eliminates the full condition.

When the FIFO is empty and no more data can be read, the Empty flag asserts high. The Empty flag is synchronous to RCLK to inhibit reading immediately upon detection of an empty condition and to prevent underflows. Since the read address is compared to a resynchronized (and thus time-delayed) version of the write address, the Empty flag will remain asserted until two RCLK active edges, after a write operation removes the empty condition.

For more information on these signals, refer to the "FIFO Flag Usage Considerations" section on page 2-27.

AFULL, AEMPTY

These are programmable flags and will be asserted on the threshold specified by AFVAL and AEVAL, respectively.

When the number of words stored in the FIFO reaches the amount specified by AEVAL while reading, the

AEMPTY output will go high. Likewise, when the number of words stored in the FIFO reaches the amount specified by AFVAL while writing, the AFULL output will go high.

AFVAL, AEVAL

The AEVAL and AFVAL pins are used to specify the almost-empty and almost-full threshold values. They are 12-bit signals. For more information on these signals, refer to the "FIFO Flag Usage Considerations" section.

ESTOP and FSTOP Usage

The ESTOP pin is used to stop the read counter from counting any further once the FIFO is empty (i.e., the EMPTY flag goes high). Likewise, the FSTOP pin is used to stop the write counter from counting any further once the FIFO is full (i.e., the Full flag goes high).

The FIFO counters in the ProASIC3E device start the count at 0, reach the maximum depth for the configuration (e.g., 511 for a 512x9 configuration), and then restart at 0. An example application for the ESTOP, where the read counter keeps counting, would be writing to the FIFO once and reading the same content over and over without doing another write.

FIFO Flag Usage Considerations

The AEVAL and AFVAL pins are used to specify the 12-bit AEMPTY and AFULL threshold values. The FIFO contains separate 12-bit write address (WADDR) and read address (RADDR) counters. WADDR is incremented every time a write operation is performed, and RADDR is incremented every time a read operation is performed. Whenever the difference between WADDR and RADDR is greater than or equal to AFVAL, the AFULL output is asserted. Likewise, whenever the difference between WADDR and RADDR is less than or equal to AEVAL, the AEMPTY output is asserted. To handle different read and write aspect ratios, AFVAL and AEVAL are expressed in terms of total data bits instead of total data words. When users specify AFVAL and AEVAL in terms of read or write words, the SmartGen tool translates them into bit addresses and configures these signals automatically. SmartGen configures the AFULL flag to assert when the write address exceeds the read address by at least a predefined value. In a 2kx8 FIFO, for example, a value of 1,500 for AFVAL means that the AFULL flag will be asserted after a write when the difference between the write address and the read address reaches 1,500 (there have been at least 1,500 more writes than reads). It will stay asserted until the difference between the write and read addresses drops below 1,500.

The AEMPTY flag is asserted when the difference between the write address and the read address is less than a predefined value. In the example above, a value of 200 for AEVAL means that the AEMPTY flag will be asserted when a read causes the difference between the write address and the read address to drop to 200. It will stay asserted until that difference rises above 200. Note that the FIFO can be configured with different read and write widths; In this case the AFVAL setting is based on the number of write data entries and the AEVAL setting is based on the number of read data entries. For aspect ratios of 512x9 and 256x18, only 4,096 bits can be addressed by the 12 bits of AFVAL and AEVAL. The number of words must be multiplied by 8 and 16 instead of 9 and 18. The SmartGen tool automatically uses the proper values. To avoid halfwords being written or read, which could happen if different read and write aspect ratios are specified, the FIFO will assert Full or Empty as soon as at least a minimum of one word cannot be written or read. For example, if a two-bit word is written and a four-bit word is being read, FIFO will remain in the Empty state when the first word is written. This occurs even if the FIFO is not completely empty, because in this case a complete word cannot be read. The same is applicable in the Full state. If a four-bit word is written and a two-bit word is read, the FIFO is full and one word is read. The FULL flag will remain asserted because a complete word cannot be written at this point.

Refer to the *ProASIC3/E SRAM/FIFO Blocks* application note for more information.

Pro I/Os

Introduction

ProASIC3E devices feature a flexible I/O structure, supporting a range of mixed voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V) through a bank-selectable voltage. Table 2-11, Table 2-12, Table 2-13, and Table 2-14 on page 2-30 show the voltages and the compatible I/O standards. I/Os provide programmable slew rates, drive strengths, weak pull-up, and weak pull-down circuits. All I/O standards, except 3.3 V PCI and 3.3 V PCI-X, are capable of hot insertion. 3.3 V PCI and 3.3 V PCI-X are 5 V tolerant. See the "5 V Input Tolerance" section on page 2-38 for possible implementations of 5 V tolerance.

Single-ended input buffers support both the Schmitt trigger and programmable delay options on a per-I/O basis.

All I/Os are in a known state during power-up and any power-up sequence is allowed without current impact. Refer to the "I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)" section on page 3-3 for more information. The I/Os will come up with disabled in/out buffers but with a weak pull-up enabled.

I/O Tile

The ProASIC3E I/O tile provides a flexible, programmable structure for implementing a large number of I/O standards. In addition, the registers available in the I/O tile can be used to support high-performance register

inputs and outputs, with register enable if desired (Figure 2-23 on page 2-33). The registers can also be used to support the JESD-79C Double Data Rate (DDR) standard within the I/O structure (see the "Double Data Rate (DDR) Support" section on page 2-34 for more information).

As depicted in Figure 2-23 on page 2-33, all I/O registers share one CLR port. The output register and output enable register share one CLK port. Refer to the "I/O Registers" section on page 2-33 for more information.

I/O Banks and I/O Standards Compatibility

I/Os are grouped into I/O voltage banks. There are eight I/O banks (two per side). Each I/O voltage bank has a dedicated input/output supply and ground voltages (VMV/GNDQ for input buffers and V_{CCI}/GND for output buffers). Because of these dedicated supplies, only I/Os with compatible standards can be assigned to the same I/O voltage bank. Table 2-12 on page 2-29 shows the required voltage compatibility values for each of these voltages.

For more information about I/O and global assignments to I/O banks, refer to the specific pin table of the device in the "Package Pin Assignments" section on page 4-1 and the "User I/O Naming Convention" section on page 2-50.

Every I/O bank is divided into minibanks. Any user I/O in a V_{REF} minibank (a minibank is the region of scope of a V_{REF} pin) can be configured as a V_{REF} pin (Figure 2-22). Only one V_{REF} pin is needed to control the entire V_{REF} minibank. The location and scope of the V_{REF} minibanks can be determined by the I/O name. For details, see the "User I/O Naming Convention" section on page 2-50.

Table 2-11 on page 2-29 shows the I/O standards supported by ProASIC3E devices and the corresponding voltage levels.

I/O standards are compatible if:

- Their V_{CCI} and VMV values are identical
- Both of the standards need a V_{REF} and their V_{REF} values are identical

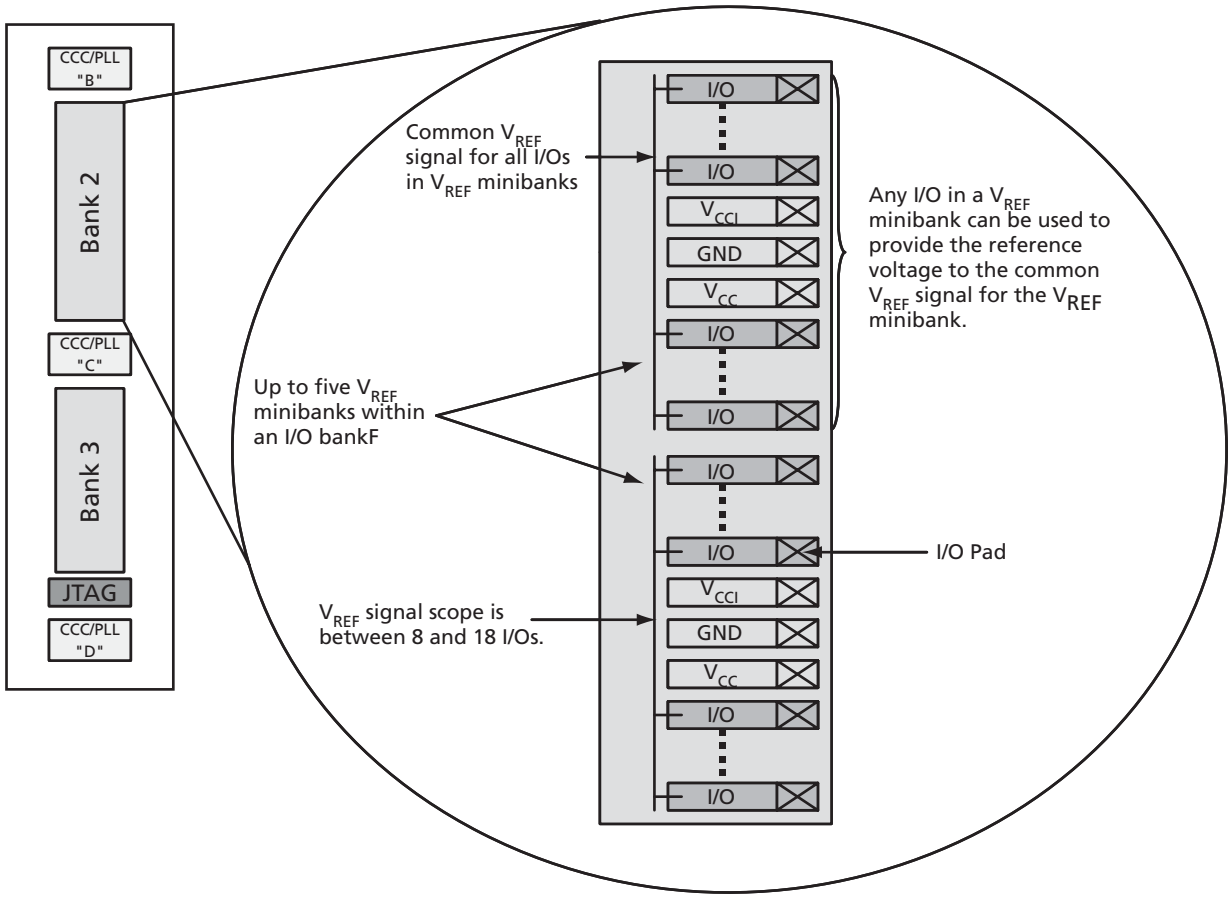


Figure 2-22 • **Typical I/O Bank Detail Showing V_{REF} Minibanks**

Table 2-11 • **ProASIC3E Supported I/O Standards**

	A3PE600	A3PE1500	A3PE3000
Single-Ended			
LVTTL/LVCMOS 3.3 V, LVCMOS 2.5 V/1.8 V/1.5 V, LVCMOS 2.5/5.0 V, 3.3 V PCI/3.3 VPCI-X	✓	✓	✓
Differential			
LVPECL, LVDS, BLVDS, M-LVDS	✓	✓	✓
Voltage-Referenced			
GTL+ 2.5 V / 3.3 V, GTL 2.5 V / 3.3 V, HSTL Class I and II, SSTL2 Class I and II, SSTL3 Class I and II	✓	✓	✓

Table 2-12 • **V_{CCI} Voltages and Compatible Standards**

V_{CCI} and VMV (typical)	**Compatible Standards**
3.3 V	LVTTL/LVCMOS 3.3, PCI 3.3, SSTL3 (Class I and II), GTL+ 3.3, GTL 3.3, LVPECL
2.5 V	LVCMOS 2.5, LVCMOS 2.5/5.0, SSTL2 (Class I and II), GTL+ 2.5, GTL 2.5, LVDS, DDR LVDS, BLVDS, and M-LVDS
1.8 V	LVCMOS 1.8
1.5 V	LVCMOS 1.5, HSTL (Class I), HSTL (Class II)

Table 2-13 • **V_{REF} Voltages and Compatible Standards**

V_{REF} (typical)	**Compatible Standards**
1.5 V	SSTL3 (Class I and II)
1.25 V	SSTL2 (Class I and II)
1.0 V	GTL+ 2.5, GTL+ 3.3
0.8 V	GTL 2.5, GTL 3.3
0.75 V	HSTL (Class I), HSTL (Class II)

Table 2-14 • **Legal I/O Usage Matrix within the Same Bank**

I/O Bank Voltage (typical)	Minibank Voltage (typical)	LVTTL/LVCMOS 3.3 V	LVCMOS 2.5 V	LVCMOS 1.8 V	LVCMOS 1.5 V	3.3 V PCI/PCI-X	GTL+ (3.3 V)	GTL+ (2.5 V)	GTL (3.3 V)	GTL (2.5 V)	HSTL Class I and II (1.5 V)	SSTL2 Class I and II (2.5 V)	SSTL3 Class I and II (3.3 V)	LVDS, BLVDS, and M-LVDS, DDR (2.5 V ± 5%)	LVPECL (3.3 V)
3.3 V	–														
	0.80 V														
	1.00 V														
	1.50 V														
2.5 V	–														
	0.80 V														
	1.00 V														
	1.25 V														
1.8 V	–														
1.5 V	–														
	0.75 V														

Note: *White box: Allowable I/O standard combinations*
Gray box: Illegal I/O standard combinations

Features Supported on Every I/O

Table 2-15 lists all features supported by transmitter/receiver for single-ended and differential I/Os.

Table 2-15 • **I/O Features ProASIC3E**

Feature	Description
Single-Ended and Voltage-Referenced Transmitter Features	• Hot insertion in every mode except PCI or 5 V input tolerant (these modes use clamp diodes and do not allow hot insertion) • Activation of hot insertion (disabling the clamp diode) is selectable by I/Os • Weak pull-up and pull-down • Two slew rates • Skew between output buffer enable/disable time: 2 ns delay on the rising edge and 0 ns delay on the falling edge (see the "Selectable Skew Between Output Buffer Enable/Disable Time" section on page 2-43 for more information). • Five drive strengths • 5 V tolerant receiver ("5 V Input Tolerance" section on page 2-38) • LVTTL/LVCMOS 3.3 V outputs compatible with 5 V TTL inputs ("5 V Input Tolerance" section on page 2-38) • High Performance (Table 2-16 on page 2-32)
Single-Ended Receiver Features	• ESD protection • Schmitt Trigger option • Programmable Delay: 0 ns if bypassed, 0.46 ns with 000 setting, 4.66 ns with 111 setting, 0.6 ns intermediate delay increments (at 25°C, 1.5 V) • High performance (Table 2-16 on page 2-32) • Separate ground plane for GNDQ pin and power plane for VMV pin are used for input buffer to reduce output induced noise.
Voltage-Referenced Differential Receiver Features	• Programmable Delay: 0 ns if bypassed, 0.46 ns with 000 setting, 4.66 ns with 111 setting, 0.6 ns intermediate delay increments (at 25°C, 1.5 V) • High performance (Table 2-16 on page 2-32) • Separate ground plane for GNDQ pin and power plane for VMV pin are used for input buffer to reduce output induced noise.
CMOS-Style LVDS, BLVDS, M-LVDS or LVPECL Transmitter	• Two I/Os and external resistors are used to provide a CMOS-style LVDS, DDR LVDS, BLVDS, and M-LVDS or LVPECL transmitter solution. • Activation of hot insertion (disabling the clamp diode) is selectable by I/Os. • Weak pull-up and pull-down • High slew rate
LVDS, DDR LVDS, BLVDS, and M-LVDS/LVPECL Differential Receiver Features	• ESD protection • High performance (Table 2-16 on page 2-32) • Programmable Delay: 0 ns if bypassed, 0.46 ns with 000 setting, 4.66 ns with 111 setting, 0.6 ns intermediate delay increments (at 25°C, 1.5 V) • Separate input buffer ground and power planes to avoid output-induced noise in the input circuitry

Table 2-16 • **Maximum I/O Frequency for Single-Ended, Voltage-Referenced, and Differential I/Os**

Specification	Performance Up To*
LVTTL/LVCMOS 3.3 V	200 MHz
LVCMOS 2.5 V	250 MHz
LVCMOS 1.8 V	200 MHz
LVCMOS 1.5 V	130 MHz
PCI	200 MHz
PCI-X	200 MHz
HSTL-I	300 MHz
HSTL-II	300 MHz
SSTL2-I	300 MHz
SSTL2-II	300 MHz
SSTL3-I	300 MHz
SSTL3-II	300 MHz
GTL+ 3.3 V	300 MHz
GTL+ 2.5 V	300 MHz
GTL 3.3 V	300 MHz
GTL 2.5 V	300 MHz
LVDS	350 MHz
BLVDS	200 MHz
M-LVDS	200 MHz
LVPECL	350 MHz

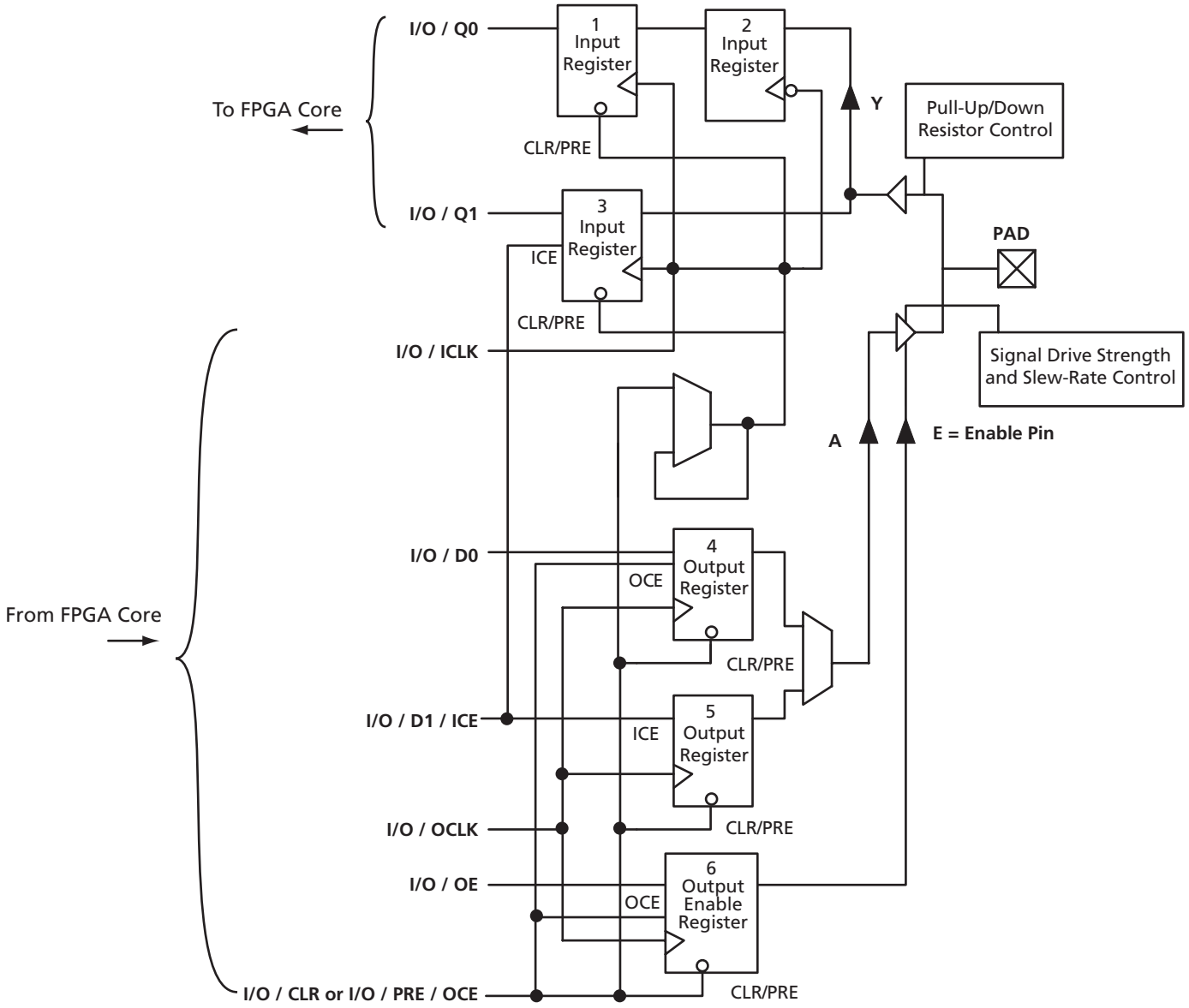
Note: **Application performance is dependent on user design implementation.*

I/O Registers

Each I/O module contains several input, output, and enable registers. Refer to Figure 2-23 for a simplified representation of the I/O block.

The number of input registers is selected by a set of switches (not shown in Figure 2-23) between registers to implement single or differential data transmission to and from the FPGA core. The Designer software sets these switches for the user.

A common CLR/PRE signal is employed by all I/O registers when I/O register combining is used. Input Register 2 does not have a CLR/PRE pin, as this register is used for DDR implementation. The I/O registers combining must satisfy some rules. For more information, refer to the *ProASIC3/E I/O Usage Guide*.



Note: *ProASIC3E I/Os have registers to support DDR functionality (see the "Double Data Rate (DDR) Support" section on page 2-34 for more information).*

Figure 2-23 • **I/O Block Logical Representation**

Double Data Rate (DDR) Support

ProASIC3E devices support 350 MHz DDR inputs and outputs. In DDR mode, new data is present on every transition of the clock signal. Clock and data lines have identical bandwidths and signal integrity requirements, making them very efficient for implementing very high-speed systems.

DDR interfaces can be implemented using HSTL, SSTL, LVDS, and LVPECL I/O standards. The DDR feature is primarily implemented in the FPGA core periphery and is not tied to a specific I/O technology or limited to any I/O standards.

Input Support for DDR

The basic structure to support a DDR input is shown in Figure 2-24. Three input registers are used to capture incoming data, which is presented to the core on each rising edge of the I/O register clock.

Each I/O tile on ProASIC3E devices supports DDR inputs.

Output Support for DDR

The basic DDR output structure is shown in Figure 2-25 on page 2-35. New data is presented to the output every half clock cycle. Note: DDR macros and I/O registers do not require additional routing. The combiner automatically recognizes the DDR macro and pushes its registers to the I/O register area at the edge of the chip. The routing delay from the I/O registers to the I/O buffers is already taken into account in the DDR macro.

Refer to the Actel application note *Using DDR for ProASIC3/E Devices* for more information.

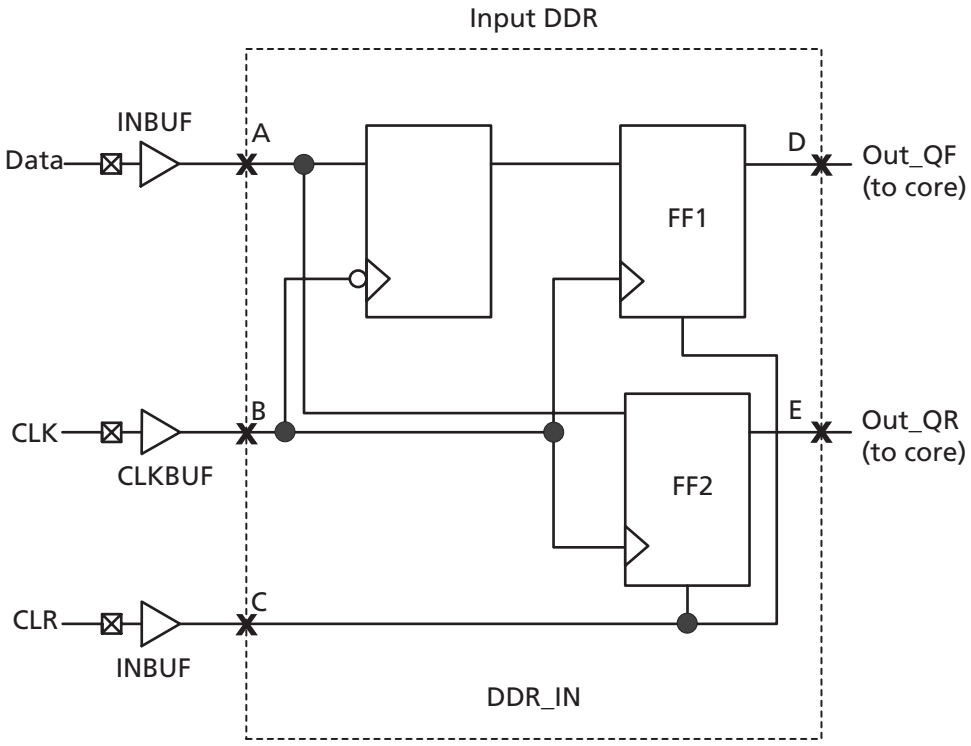


Figure 2-24 • **DDR Input Register Support in ProASIC3E Devices**

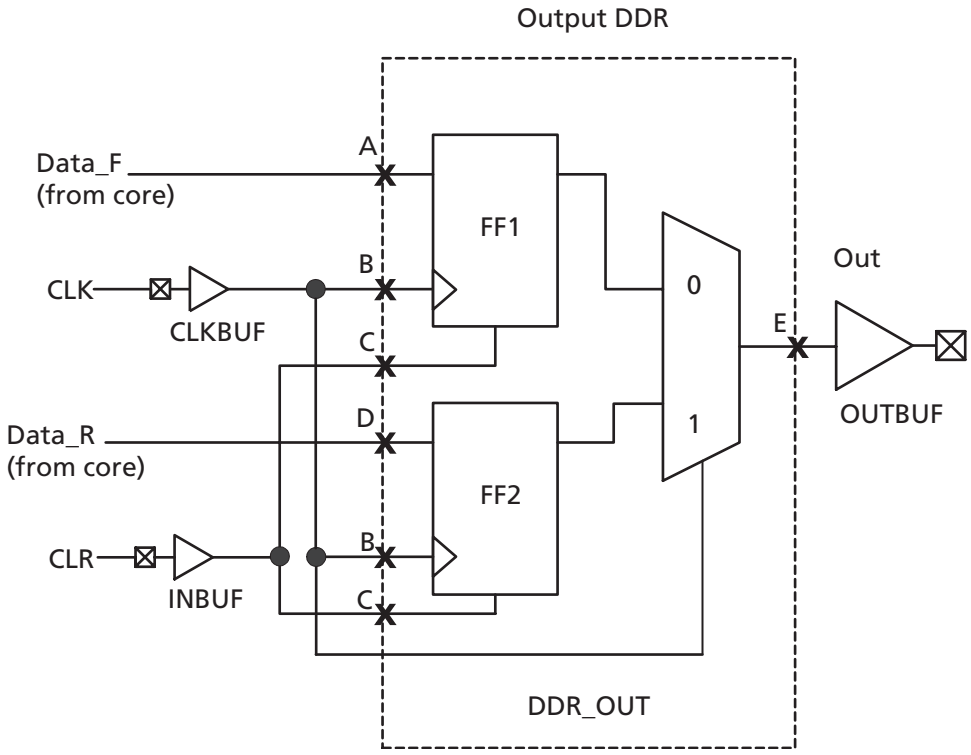


Figure 2-25 • **DDR Output Support in ProASIC3E Devices**

Hot-Swap Support

Hot-swapping (also called hot plugging) is the operation of hot insertion or hot removal of a card in (or from) a powered-up system. The levels of hot-swap support and examples of related applications are described in Table 2-17. The I/Os also need to be configured in hot insertion mode if hot plugging compliance is required.

Table 2-17 • **Levels of Hot-Swap Support**

Hot-Swapping Level	Description	Power Applied to Device	Bus State	Card Ground Connection	Device Circuitry Connected to Bus Pins	Example of Application with Cards that Contain ProASIC3E Devices	Compliance of ProASIC3E Devices
1	Cold-swap	No	–	–	–	System and card with Actel FPGA chip are powered down and the card is plugged into the system. Then the power supplies are turned on for the system but not for the FPGA on the card.	Compliant I/Os can but do not have to be set to hot insertion mode.
2	Hot-swap while reset	Yes	Held in reset state	Must be made and maintained for 1 msec before, during, and after insertion/ removal	–	In PCI hot-plug specification Reset control circuitry isolates the card busses until the card supplies are at their nominal operating levels and stable.	Compliant I/Os can but do not have to be set to hot-insertion mode.
3	Hot-swap while bus idle	Yes	Held idle (no ongoing I/O processes during insertion/ removal)	Same as Level 2	Must remain glitch-free during power-up or power-down	Board bus shared with card bus is "frozen," and there is no toggling activity on the bus. It is critical that the logic states set on the bus signal do not get disturbed during card insertion/removal.	Compliant with cards with two levels of staging. I/Os have to be set to hot-insertion mode.
4	Hot-swap on an active bus	Yes	Bus may have active I/O processes ongoing, but device being inserted or removed must be idle	Same as Level 2	Same as Level 3	There is activity on the system bus, and it is critical that the logic states set on the bus signal do not get disturbed during card insertion/removal.	: Compliant with cards with two levels of staging. I/Os have to be set to hot insertion mode.

For ProASIC3E devices requiring level 3 and/or level 4 compliance, the board drivers connected to ProASIC3E I/Os must have 10 kΩ (or lower) output drive resistance at hot insertion, and 1 kΩ (or lower) output drive resistance at hot removal. This resistance is the transmitter resistance sending signal towards the ProASIC3E I/O and no additional resistance is needed on the board. If that cannot be assured, three levels of staging can be used to meet level 3 and/or level 4 compliance. Cards with two levels of staging should have the following sequence:

- Grounds
- Powers, I/Os, and other pins

For boards and cards with three levels of staging, card power supplies must have time to reach their final value before the I/Os are connected. Pay attention to the sizing of power supply decoupling capacitors on the card to ensure that the power supplies are not overloaded with capacitance.

Cards with three levels of staging should have the following sequence:

- Grounds
- Powers
- I/Os and other pins

Cold-Sparing Support

Cold-sparing means that a subsystem with no power applied (usually a circuit board) is electrically connected to the system that is in operation. This means that all input buffers of the subsystem must present very high input impedance with no power applied so as not to disturb the operating portion of the system.

ProASIC3E devices support cold-sparing for all I/O configurations. Standards such as PCI which require I/O clamp diodes can also achieve cold-sparing compliance, since clamp diodes get disconnected internally when the supplies are at 0 V.

If the resistor is chosen, the resistor value must be calculated based on decoupling capacitance on a given power supply on the board (this decoupling capacitor is in parallel with this resistor). The RC time constant should ensure full discharge of supplies before cold-sparing functionality is required. The resistor is necessary to ensure that the power pins are discharged to ground every time there is an interruption of power to the device.

Electrostatic Discharge (ESD) Protection

ProASIC3E devices are tested per JEDEC Standard JESD22-A114-B.

ProASIC3E devices contain clamp diodes at every I/O, global, and power pad. Clamp diodes protect all device pads against damage from ESD as well as from excessive voltage transients.

ProASIC3E devices are tested to the following models: Human Body Model (HBM) with a tolerance of 2,000 V, the Machine Model (MM) with a tolerance of 250 V, and the Charged Device Model (CDM) with a tolerance of 200 V.

Each I/O has two clamp diodes. One diode has its positive (P) side connected to the pad and its negative (N) side connected to V_{CCI}. The second diode has its P side connected to GND, and its N side connected to the pad. During operation, these diodes are normally biased in the Off state, except when transient voltage is significantly above V_{CCI} or below GND levels.

By selecting the appropriate I/O configuration, the diode is turned on or off. Refer to Table 2-18 for more information about the I/O standards and the clamp diode.

The second diode is always connected to the pad, regardless of the I/O configuration selected.

Table 2-18 • **I/O Hot-Swap and 5 V Input Tolerance Capabilities**

I/O Assignment	Clamp Diode	Hot Insertion	5 V Input Tolerance	Input Buffer	Output Buffer
3.3 V LVTTL/LVCMOS	No	Yes	Yes[1]	Enabled/Disabled	
3.3 V PCI, 3.3 V PCI-X	Yes	No	Yes[1]	Enabled/Disabled	
LVCMOS 2.5 V [3]	No	Yes	No	Enabled/Disabled	
LVCMOS 2.5 V / 5.0 V [3]	Yes	No	Yes[2]	Enabled/Disabled	
LVCMOS 1.8 V	No	Yes	No	Enabled/Disabled	
LVCMOS 1.5 V	No	Yes	No	Enabled/Disabled	
Voltage-Referenced Input Buffer	No	Yes	No	Enabled/Disabled	
Differential, LVDS/BLVDS/M-LVDS/LVPECL	No	Yes	No	Enabled/Disabled	

Notes:

1. *Can be implemented with an external IDT bus switch, resistor divider, or zener with resistor.*
2. *Can be implemented with an external resistor and an internal clamp diode.*
3. *In the SmartGen Core Reference Guide, select the LVCMOS5 macro for the LVCMOS 2.5 V / 5.0 V I/O standard or the LVCMOS25 macro for the LVCMOS 2.5 V I/O standard.*

5 V Input Tolerance

I/Os can support 5-V-input tolerance when LVTTL 3.3 V, LVCMOS 3.3 V, LVCMOS 2.5 V / 5 V, and LVCMOS 2.5 V configurations are used (see Table 2-18 on page 2-37 for more details). There are four recommended solutions for achieving 5 V receiver tolerance (see Figure 2-26 to Figure 2-29 on page 2-41 for details of board and macro setups). All the solutions meet a common requirement of limiting the voltage at the I/O input to 3.6 V or less. In fact, the I/O absolute maximum voltage rating is 3.6 V, and any voltage above 3.6 V may cause long term gate oxide failures.

Solution 1

The board-level design must ensure that the reflected waveform at the pad does not exceed the limits provided in Table 3-4 on page 3-2. This is a requirement to ensure long term reliability.

This scheme will also work for a 3.3 V PCI/PCI-X configuration, but the internal diode should not be used for clamping, and the voltage must be limited by the two external resistors as explained below. Relying on the diode clamping would create an excessive pad DC voltage of 3.3 V + 0.7 V = 4 V.

Here are some examples of possible resistor values (based on a simplified simulation model with no line effects, and 10 Ω transmitter output resistance, where Rtx_out_high = $(V_{CCI} - V_{OH})/ I_{OH}$, Rtx_out_low = V_{OL} / I_{OL}).

Example 1 (high speed, high current):

Rtx_out_high = Rtx_out_low = 10 Ω

R1 = 36 Ω (±5%), P(r1)min = 0.069 Ω

R2 = 82 Ω (±5%), P(r2)min = 0.158 Ω

Imax_tx = 5.5 V / (82 × 0.95 + 36 × 0.95 +10) = 45.04 mA

$t_{RISE} = t_{FALL}$ = 0.85 ns at C_pad_load = 10 pF (includes up to 25% safety margin)

$t_{RISE} = t_{FALL}$ = 4 ns at C_pad_load = 50 pF (includes up to 25% safety margin)

Example 2 (low-medium speed, medium current):

Rtx_out_high = Rtx_out_low = 10 Ω

R1 = 220 Ω (±5%), P(r1)min = 0.018 Ω

R2 = 390 Ω (±5%), P(r2)min = 0.032 Ω

Imax_tx = 5.5 V / (220 × 0.95 + 390 × 0.95 +10) = 9.17 mA

$t_{RISE} = t_{FALL}$ = 4 ns at C_pad_load = 10 pF (includes up to 25% safety margin)

$t_{RISE} = t_{FALL}$ = 20 ns at C_pad_load = 50 pF (includes up to 25% safety margin)

Other values of resistors are also allowed as long as the resistors are sized appropriately to limit the voltage at the receiving end to 2.5 V < Vin(rx) < 3.6 V* when the transmitter sends a logic '1'. This range of Vin_dc(rx) must be assured for any combination of transmitter supply (5 V ± 0.5 V), transmitter output resistance, and board resistor tolerances.

Temporary overshoots are allowed according to Table 3-4 on page 3-2.

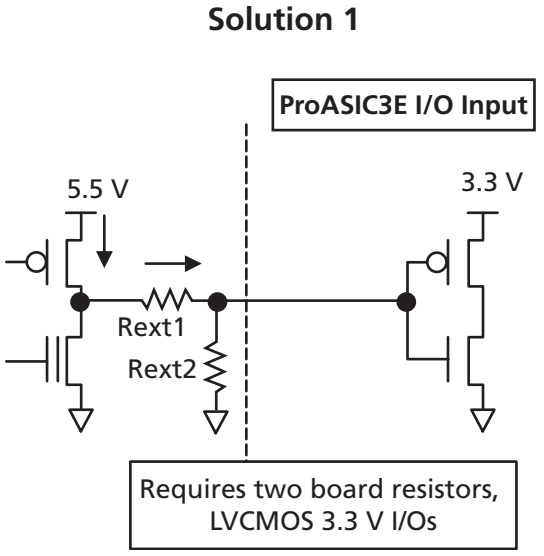


Figure 2-26 • **Solution 1**

Solution 2

The board-level design must ensure that the reflected waveform at the pad does not exceed limits provided in Table 3-4 on page 3-2. This is a requirement to ensure long term reliability.

This scheme will also work for a 3.3 V PCI/PCIX configuration, but the internal diode should not be used for clamping, and the voltage must be limited by the external resistors and zener, as shown in Figure 2-27. Relying on the diode clamping would create an excessive pad DC voltage of 3.3 V + 0.7 V = 4 V.

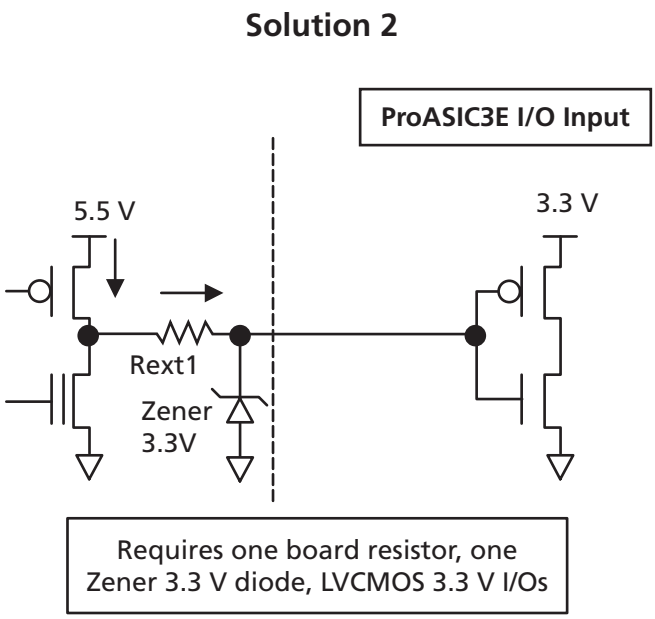


Figure 2-27 • **Solution 2**

Solution 3

The board-level design must ensure that the reflected waveform at the pad does not exceed limits provided in Table 3-4 on page 3-2. This is a requirement to ensure long term reliability.

This scheme will also work for a 3.3 V PCI/PCIX configuration, but the internal diode should not be used for clamping, and the voltage must be limited by the bus switch, as shown in Figure 2-28. Relying on the diode clamping would create an excessive pad DC voltage of 3.3 V + 0.7 V = 4 V

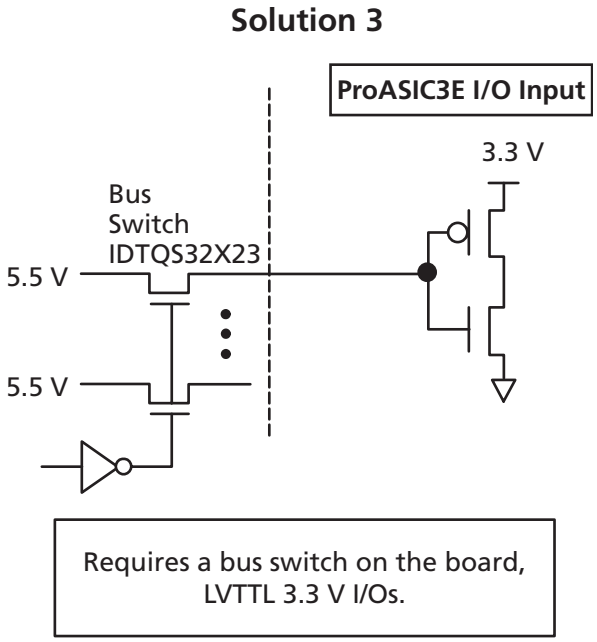


Figure 2-28 • **Solution 3**

Solution 4

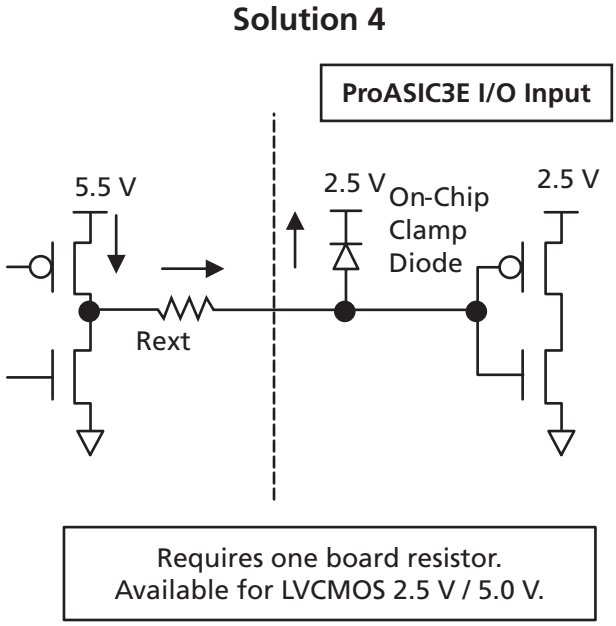


Figure 2-29 • **Solution 4**

Table 2-19 • **Comparison Table for 5 V Compliant Receiver Scheme**

Scheme	Board Components	Speed	Current Limitations
1	Two resistors	Low to High[1]	Limited by transmitter's drive strength
2	Resistor and Zener 3.3 V	Medium	Limited by transmitter's drive strength
3	Bus switch	High	N/A
4	Minimum resistor value[2] • R = 47 Ω at T_J = 70°C • R = 150 Ω at T_J = 85°C • R = 420 Ω at T_J = 100°C	Medium	Maximum diode current at 100% duty cycle, signal constantly at '1' • 5 × 52.7 mA at T_J = 70°C / 10-year lifetime • 16.5 mA at T_J = 85°C / 10-year lifetime • 5.9 mA at T_J = 100°C / 10-year lifetime For duty cycles other than 100%, the currents can be increased by a factor = 1/duty cycle. Example: 20% duty cycle at 70°C Maximum current = (1/0.2) × 52.7 mA = 4 × 52.7 mA = 263.5 mA

Notes:

1. *Speed and current consumption increase as the board resistance values decrease.*
2. *Resistor values ensure I/O diode long term reliability.*

5 V Output Tolerance

ProASIC3E I/Os must be set to 3.3 V LVTTL or 3.3 V LVCMOS mode to reliably drive 5 V TTL receivers. It is also critical that there be NO external I/O pull-up resistor to 5 V, since this resistor would pull the I/O pad voltage beyond the 3.6 V absolute maximum value, and consequently cause damage to the I/O.

When set to 3.3 V LVTTL or 3.3 V LVCMOS mode, ProASIC3E I/Os can directly drive signals into 5 V TTL receivers. In fact, V_{OL} = 0.4 V and V_{OH} = 2.4 V in both 3.3 V LVTTL and 3.3 V LVCMOS modes exceeds the V_{IL} = 0.8 V and V_{IH} = 2 V level requirements of 5 V TTL receivers. Therefore, level '1' and level '0' will be recognized correctly by 5 V TTL receivers.

Simultaneous Switching Outputs and Printed Circuit Board Layout

Simultaneously switching outputs (SSO) can cause signal integrity problems on adjacent signals that are not part of the SSO bus. Both inductive and capacitive coupling parasitics of bond wires inside packages and of traces on printed circuit boards (PCBs) will transfer noise from SSO busses onto signals adjacent to those busses. Additionally, SSOs can produce ground bounce noise and V_{CCI} dip noise. These two noise types are caused by rapidly-changing currents through GND and V_{CCI} package pin inductances during switching activities (EQ 2-1 and EQ 2-2).

Ground bounce noise voltage = L (GND) × di/dt

EQ 2-1

V_{CCI} dip noise voltage = L (V_{CCI}) × di/dt

EQ 2-2

Any group of four or more input pins switching on the same clock edge is considered an SSO bus. The shielding should be done both on the board and inside the package unless otherwise described.

In-package shielding can be achieved in several ways; the required shielding will vary depending on whether pins next to the SSO bus are LVTTL/LVCMOS inputs, LVTTL/LVCMOS outputs, or GTL/SSTL/HSTL/LVDS/LVPECL inputs and outputs. Board traces in the vicinity of the SSO bus have to be adequately shielded from mutual coupling and inductive noise that can be generated by the SSO bus. Also, noise generated by the SSO bus needs to be reduced inside the package.

PCBs perform an important function in feeding stable supply voltage to the IC and at the same time maintain signal integrity between devices.

Key issues that need to considered are as follows:

- Power and ground plane design and decoupling network design
- Transmission line reflections and terminations

Selectable Skew Between Output Buffer Enable/Disable Time

The configurable skew block is used to delay the output buffer assertion (enable) without affecting deassertion (disable) time.

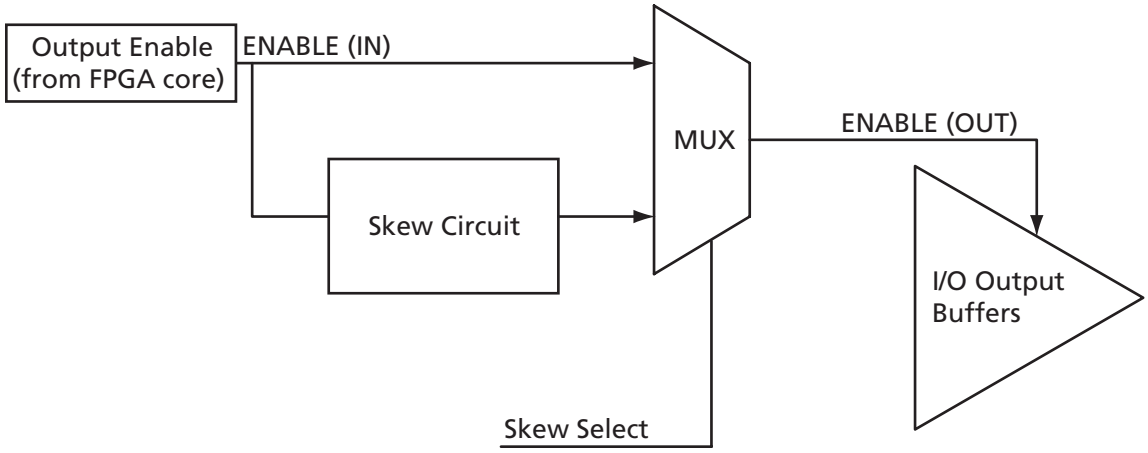


Figure 2-30 • **Block Diagram of Output Enable Path**

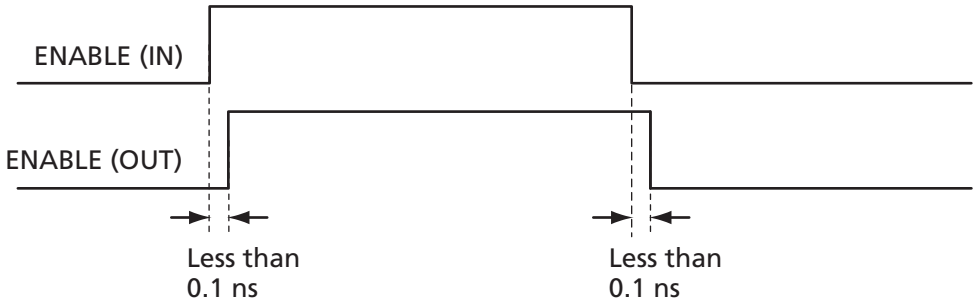


Figure 2-31 • **Timing Diagram (Option1: Bypasses Skew Circuit)**

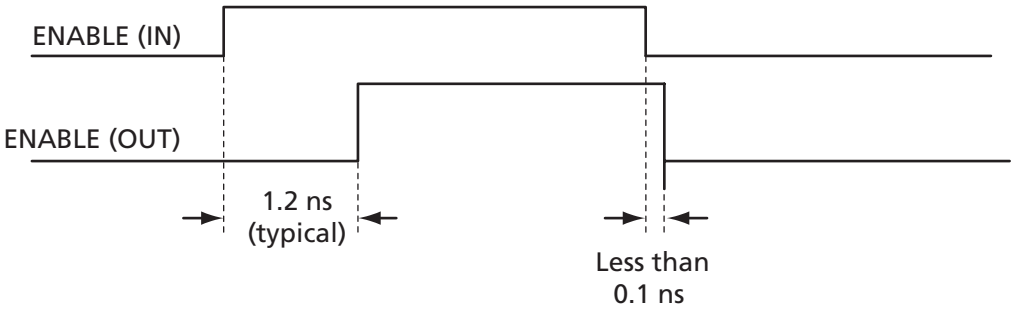


Figure 2-32 • **Timing Diagram (Option 2: Enables Skew Circuit)**

At the system level, the skew circuit can be used in applications where transmission activities on bidirectional data lines need to be coordinated. This circuit, when selected, provides a timing margin that can prevent bus contention and subsequent data loss and/or transmitter over-stress due to transmitter-to-transmitter current shorts. Figure 2-33 presents an example of the skew circuit implementation in a bidirectional communication system. Figure 2-34 shows how bus contention is created, and Figure 2-35 on page 2-45 shows how it can be avoided with the skew circuit.

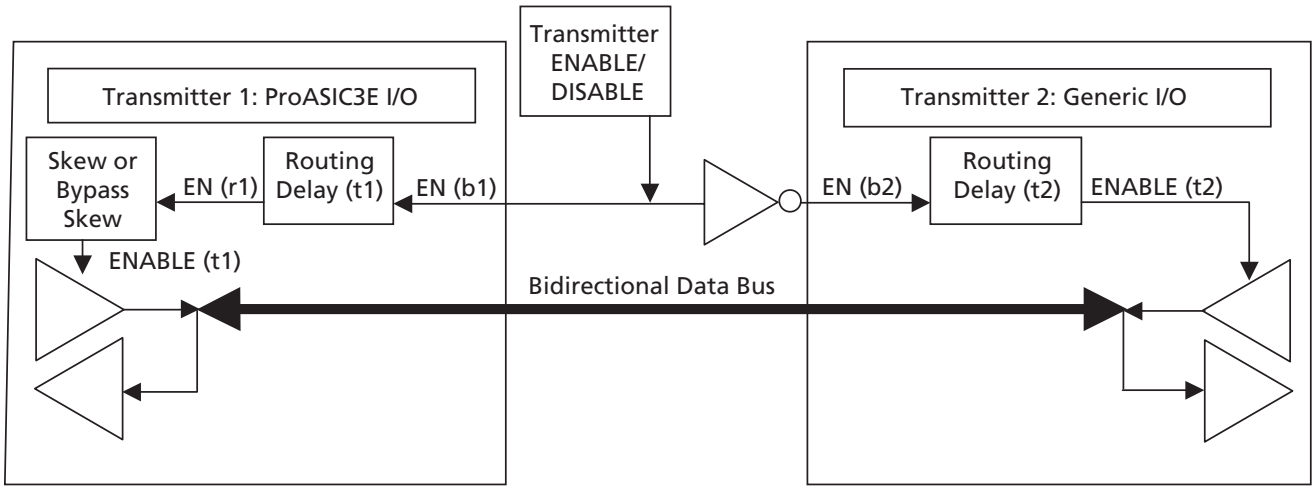


Figure 2-33 • **Example of Implementation of Skew Circuits in Bidirectional Transmission Systems Using ProASIC3E Devices**

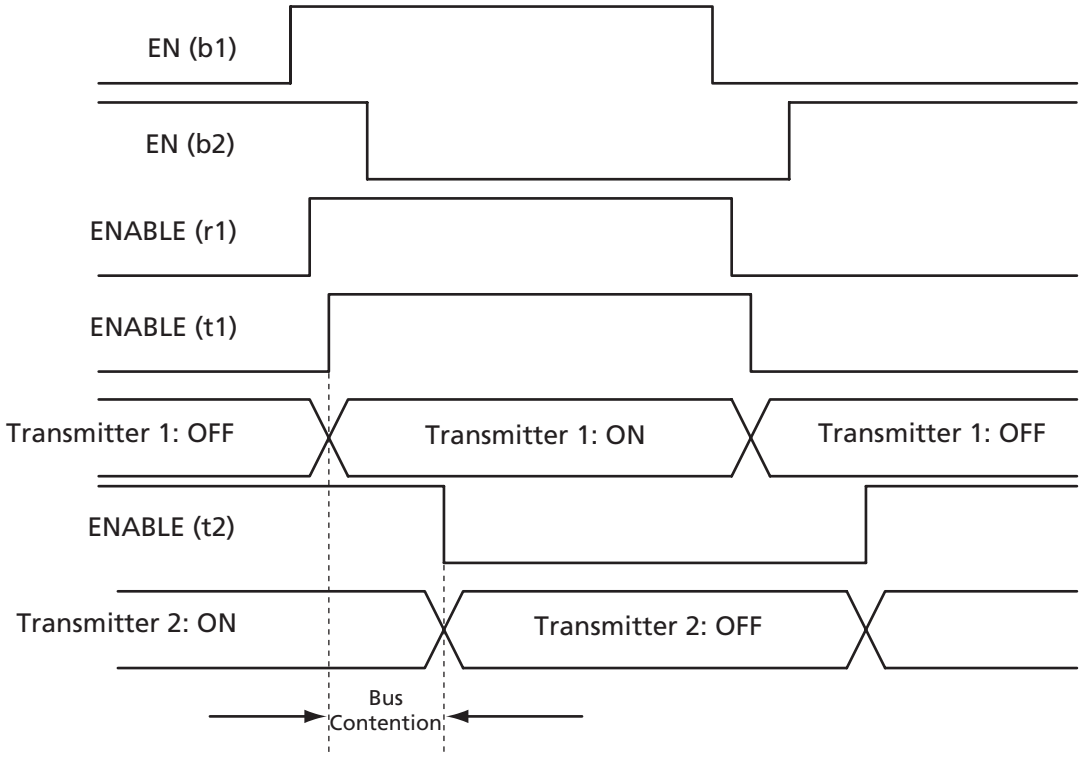
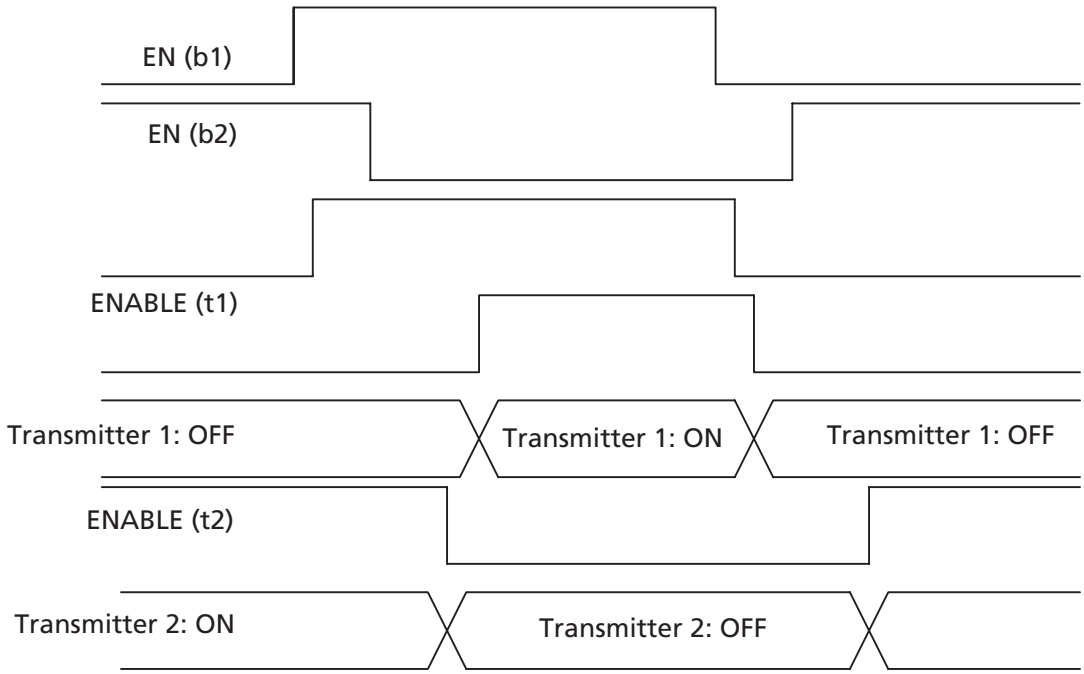


Figure 2-34 • **Timing Diagram (Bypasses Skew Circuit)**



Result: No Bus Contention

Figure 2-35 • **Timing Diagram (with Skew Circuit Selected)**

I/O Software Support

In the ProASIC3E development software, default settings have been defined for the various I/O standards that are supported. Changes can be made to the default settings via the use of attributes; however, not all I/O attributes are applicable for all I/O standards. Table 2-20 lists the valid I/O attributes that can be manipulated by the user for each I/O standard.

Single-ended I/O standards in ProASIC3E support up to five different drive strengths.

Table 2-20 • **I/O Attributes vs. I/O Standard Applications**

I/O Standards	SLEW (output only)	OUT_DRIVE (output only)	SKEW (all macros with OE)	RES_PULL	OUT_LOAD (output only)	COMBINE_REGISTER	IN_DELAY (input only)	IN_DELAY_VAL (input only)	SCHMITT_TRIGGER (input only)	HOT_SWAPPABLE
LVTTL/LVCMOS 3.3 V	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
LVCMOS 2.5 V	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
LVCMOS 2.5/5.0 V	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
LVCMOS 1.8 V	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
LVCMOS 1.5 V	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
PCI (3.3 V)			✓		✓	✓	✓	✓		
PCI-X (3.3 V)	✓		✓		✓	✓	✓	✓		
GTL+ (3.3 V)			✓		✓	✓	✓	✓		✓
GTL+ (2.5 V)			✓		✓	✓	✓	✓		✓
GTL (3.3 V)			✓		✓	✓	✓	✓		✓
GTL (2.5 V)			✓		✓	✓	✓	✓		✓
HSTL Class I			✓		✓	✓	✓	✓		✓
HSTL Class II			✓		✓	✓	✓	✓		✓
SSTL2 Class I and II			✓		✓	✓	✓	✓		✓
SSTL3 Class I and II			✓		✓	✓	✓	✓		✓
LVDS, BLVDS, M-LVDS			✓			✓	✓	✓		✓
LVPECL						✓	✓	✓		✓

Weak Pull-Up and Weak Pull-Down Resistors

ProASIC3E devices support optional weak pull-up and pull-down resistors per I/O pin. When the I/O is pulled up, it is connected to the V_{CCI} of its corresponding I/O bank. When it is pulled-down it is connected to GND. Refer to Table 3-20 on page 3-20 for more information.

Slew Rate Control and Drive Strength

ProASIC3E devices support output slew rate control: high and low.Actel recommends the high slew rate option to minimize the propagation delay. This high-speed option may introduce noise into the system if appropriate signal integrity measures are not adopted. Selecting a low slew rate reduces this kind of noise but adds some delays in the system. Low slew rate is recommended when bus transients are expected. Drive strength should also be selected according to the design requirements and noise immunity of the system.

The output slew rate and multiple drive strength controls are available in LVTTL/LVCMOS 3.3 V, LVCMOS 2.5 V, LVCMOS 2.5 V / 5.0 V input, LVCMOS 1.8 V, and LVCMOS 1.5 V. All other I/O standards have a high output slew rate by default.

Refer to Table 2-21 for more information about the slew rate and drive strength specification. Table 2-23 on page 2-49 lists the default values for the above selectable I/O attributes as well as those that are preset for that I/O standard.

Refer to Table 2-21 for SLEW and OUT_DRIVE settings. Table 2-22 on page 2-48 lists the I/O default attributes. Table 2-23 on page 2-49 lists the voltages for the supported I/O standards.

Table 2-21 • **I/O Standards—SLEW and Output Drive (OUT_DRIVE) Settings**

I/O Standards	OUT_DRIVE (mA)							Slew	
	2	4	6	8	12	16	24		
LVTTL/LVCMOS 3.3 V	✓	✓	✓	✓	✓	✓	✓	High	Low
LVCMOS 2.5 V	✓	✓	✓	✓	✓	✓	✓	High	Low
LVCMOS 2.5 V/5.0 V	✓	✓	✓	✓	✓	✓	✓	High	Low
LVCMOS 1.8 V	✓	✓	✓	✓	✓	✓	–	High	Low
LVCMOS 1.5 V	✓	✓	✓	✓	✓	–	–	High	Low

Table 2-22 • **I/O Default Attributes**

I/O Standards	SLEW (output only)	OUT_DRIVE (output only)	SKEW) (tribuf and bibuf only)	RES_PULL	OUT_LOAD (output only)	COMBINE_REGISTER	IN_DELAY (input only)	IN_DELAY_VAL (input only)	SCHMITT_TRIGGER (input only)
LVTTL/LVCMOS 3.3 V	See Table 2-21 on page 2-47	See Table 2-21 on page 2-47	Off	None	35pF	–	Off	0	Off
LVCMOS 2.5 V			Off	None	35 pF	–	Off	0	Off
LVCMOS 2.5/5.0 V			Off	None	35 pF	–	Off	0	Off
LVCMOS 1.8 V			Off	None	35 pF	–	Off	0	Off
LVCMOS 1.5 V			Off	None	35 pF	–	Off	0	Off
PCI (3.3 V)			Off	None	10 pF	–	Off	0	Off
PCI-X (3.3 V)			Off	None	10 pF	–	Off	0	Off
GTL+ (3.3 V)			Off	None	10 pF	–	Off	0	Off
GTL+ (2.5 V)			Off	None	10 pF	–	Off	0	Off
GTL (3.3 V)			Off	None	10 pF	–	Off	0	Off
GTL (2.5 V)			Off	None	10 pF	–	Off	0	Off
HSTL Class I			Off	None	20 pF	–	Off	0	Off
HSTL Class II			Off	None	20 pF	–	Off	0	Off
SSTL2 Class I and II			Off	None	30 pF	–	Off	0	Off
SSTL3 Class I and II			Off	None	30 pF	–	Off	0	Off
LVDS, BLVDS, M-LVDS			Off	None	0 pF	–	Off	0	Off
LVPECL			Off	None	0 pF	–	Off	0	Off

Table 2-23 • **Supported I/O Standards and the Corresponding V_{REF} and V_{TT} Voltages**

I/O Standard	Input/Output Supply Voltage (VMVtyp/V_{CCI_TYP})	Input Reference Voltage (V_{REF_TYP})	Board Termination Voltage (V_{TT_TYP})
LVTTL/LVCMOS 3.3 V	3.30 V	–	–
LVCMOS 2.5 V	2.50 V	–	–
LVCMOS 2.5 V/5.0 V Input	2.50 V	–	–
LVCMOS 1.8 V	1.80 V	–	–
LVCMOS 1.5 V	1.50 V	–	–
PCI 3.3 V	3.30 V	–	–
PCI-X 3.3 V	3.30 V	–	–
GTL+ 3.3 V	3.30 V	1.00 V	1.50 V
GTL+ 2.5 V	2.50 V	1.00 V	1.50 V
GTL 3.3 V	3.30 V	0.80 V	1.20 V
GTL 2.5 V	2.50 V	0.80 V	1.20 V
HSTL Class I	1.50 V	0.75 V	0.75 V
HSTL Class II	1.50 V	0.75 V	0.75 V
SSTL3 Class I	3.30 V	1.50 V	1.50 V
SSTL3 Class II	3.30 V	1.50 V	1.50 V
SSTL2 Class I	2.50 V	1.25 V	1.25 V
SSTL2 Class II	2.50 V	1.25 V	1.25 V
LVDS, DDR LVDS, BLVDS, and M-LVDS	2.50 V	–	–
LVPECL	3.30 V	–	–

User I/O Naming Convention

Due to the comprehensive and flexible nature of ProASIC3E device user I/Os, a naming scheme is used to show the details of the I/O (Figure 2-36). The name identifies to which I/O bank it belongs, as well as the pairing and pin polarity for differential I/Os.

I/O Nomenclature = Gmn/IOuxwByVz

Gmn is only used for I/Os that also have CCC access—i.e., global pins.

G = Global

m = Global pin location associated with each CCC on the device: A (northwest corner), B (northeast corner), C (east middle), D (southeast corner), E (southwest corner), and F (west middle)

n = Global input MUX and pin number of the associated Global location m, either A0, A1,A2, B0, B1, B2, C0, C1, or C2. Figure 2-14 on page 2-16 shows the three input pins per each clock source MUX at the CCC location m.

u = I/O pair number in the bank, starting at 00 from the northwest I/O bank and proceeds in a clockwise direction.

x = P (Positive) or N (Negative) for differential pairs, or R (Regular—single-ended) for the I/Os that support single-ended and voltage-referenced I/O standards only.

w = D (Differential Pair) or P (Pair) or S (Single-Ended). D (Differential Pair) if both members of the pair are bonded out to adjacent pins or are separated only by one GND or NC pin; P (Pair) if both members of the pair are bonded out but do not meet the adjacency requirement; or S (Single-Ended) if the I/O pair is not bonded out. For Differential (D) pairs, adjacency for ball grid packages means only vertical or horizontal. Diagonal adjacency does not meet the requirements for a true differential pair.

B = Bank

y = Bank number [0..7]. The bank number starts at 0 from northwest I/O bank and proceeds in a clockwise direction.

V = V_{REF}

z = V_{REF} minibank number [0...4]. A given voltage-referenced signal spans 16 pins (typically) in an I/O bank. Voltage banks may have multiple V_{REF} minibanks.

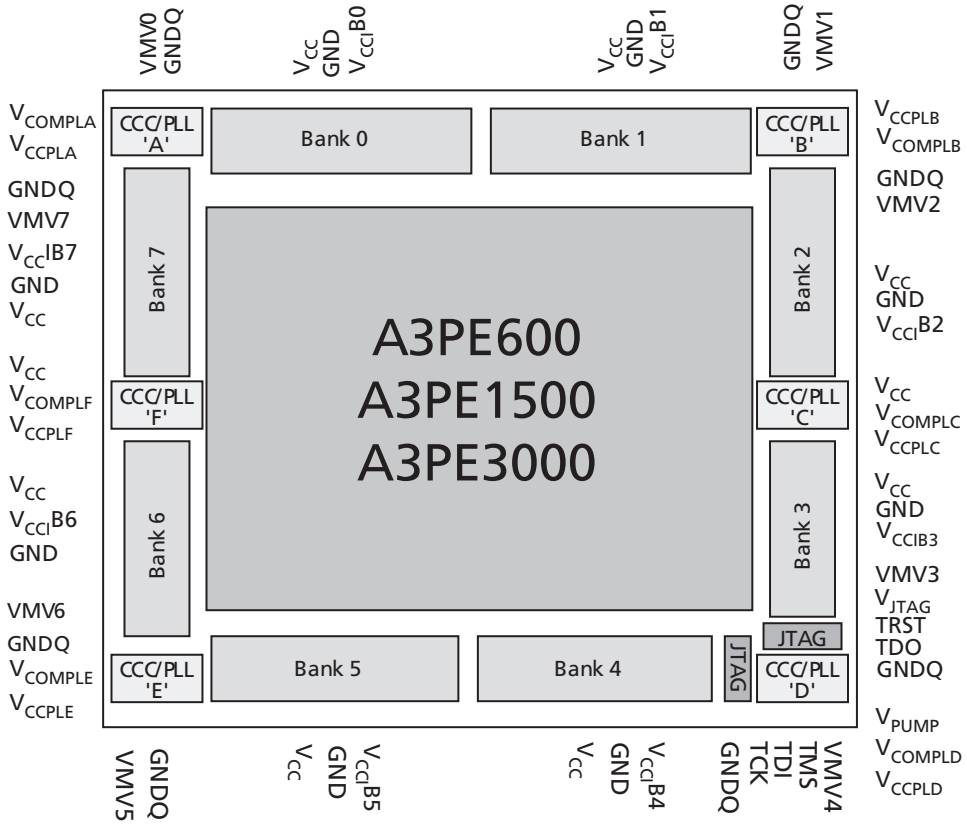


Figure 2-36 • **User I/O Naming Conventions of ProASIC3E Devices**

Pin Descriptions

Supply Pins

GND **Ground**

Ground supply voltage to the core, I/O outputs, and I/O logic.

GNDQ **Ground (quiet)**

Quiet ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package, and improves input signal integrity. GNDQ must always be connected to GND on the board.

V_{CC} **Core Supply Voltage**

Supply voltage to the FPGA core, nominal 1.5 V. V_{CC} is also required for powering the JTAG state machine in addition to V_{JTAG}. Even when a ProASIC3 device is in bypass mode in a JTAG chain of interconnected devices, both V_{CC} and V_{JTAG} must remain powered to allow JTAG signals to pass through the ProASIC3 device.

V_{CCI}Bx **I/O Supply Voltage**

Supply voltage to the bank's I/O output buffers and I/O logic. Bx is the I/O bank number. There are eight I/O banks on ProASIC3E devices plus a dedicated V_{JTAG} bank. Each bank can have a separate V_{CCI} connection. All I/Os in a bank will run off the same V_{CCI}Bx supply. V_{CCI} can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V nominal voltage. Unused I/O banks should have their corresponding V_{CCI} pins tied to GND.

VMVx **I/O Supply Voltage (quiet)**

Quiet supply voltage to the input buffers of each I/O bank. X is the bank number. Within the package, the VMV plane is decoupled from the simultaneous switching noise originated from the output buffer V_{CCI} domain. This minimizes the noise transfer within the package, and improves input signal integrity. Each bank must have at least one VMV connection and no VMV should be left unconnected. All I/Os in a bank run off the same VMVx supply. VMV is used to provide a quiet supply voltage to the input buffers of each I/O bank. VMVx can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V nominal voltage. Unused I/O banks should have their corresponding VMV pins tied to GND. VMV and V_{CCI} should be at the same voltage within a given I/O bank. Used VMV pins must be connected to the corresponding V_{CCI} pins of the same bank (i.e., VMV0 to V_{CCI}B0, VMV1 to V_{CCI}B1, etc.).

$V_{CCPLA/B/C/D/E/F}$ **PLL Supply Voltage**

Supply voltage to analog PLL, nominal 1.5 V. There are six V_{CCPL} pins (PLL power) on ProASIC3E devices. Unused V_{CCPL} pins should be connected to GND.

$V_{COMPLA/B/C/D/E/F}$ **PLL Ground**

Ground to analog PLL. There are six V_{COMPL} pins (PLL ground) on ProASIC3E. Unused V_{COMPL} pins should be connected to GND.

V_{JTAG} **JTAG Supply Voltage**

ProASIC3E devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). Isolating the JTAG power supply in a separate I/O bank gives greater flexibility with supply selection and simplifies power supply and printed circuit board design. If the JTAG interface is neither used nor planned for use, the V_{JTAG} pin together with the TRST pin could be tied to GND. It should be noted that V_{CC} is required to be powered for JTAG operation; V_{JTAG} alone is insufficient. If a ProASIC3E device is in a JTAG chain of interconnected boards, the board containing the ProASIC3E device can be powered down, provided both V_{JTAG} and V_{CC} to the ProASIC3E part remain powered; otherwise JTAG signals will not be able to transition the ProASIC3E device, even in bypass mode.

V_{PUMP} **Programming Supply Voltage**

ProASIC3E devices support single-voltage ISP programming of the configuration Flash and FlashROM. For programming, V_{PUMP} should be 3.3 V nominal. During normal device operation, V_{PUMP} can be left floating or can be tied (pulled up) to any voltage between 0 V and 3.6 V.

When the V_{PUMP} pin is tied to ground, it will shut off the charge pump circuitry, resulting in no sources of oscillation from the charge pump circuitry.

User-Defined Supply Pins

V_{REF} **I/O Voltage Reference**

Reference voltage for I/O minibanks. V_{REF} pins are configured by the user from regular I/Os, and any I/O in a bank, except JTAG I/Os, which can be designated as the voltage reference I/O. Only certain I/O standards require a voltage reference—HSTL (I) and (II), SSTL2 (I) and (II), SSTL3 (I) and (II), and GTL/GTL+. One V_{REF} pin can support the number of I/Os available in its minibank.

User Pins

I/O **User Input/Output**

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output signal levels are compatible with the I/O standard selected.

During programming, I/Os become tristated and weakly pulled up to V_{CCI}. With V_{CCI}, VMV, and V_{CC} supplies continuously powered-up, and the device transitions from programming to operating mode, the I/Os get instantly configured to the desired user configuration.

Unused I/Os are configured as follows:

- Output buffer is disabled (with tristate value of Hi-Z)
- Input buffer is disabled (with tristate value of Hi-Z)
- Weak pull-up is programmed

GL **Globals**

GL I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as Pro I/Os, since they have identical capabilities. Unused GL pins are configured as inputs with pull-up resistors.

Refer to the "User I/O Naming Convention" section on page 2-50 for a explanation of the naming of global pins.

JTAG Pins

ProASIC3E devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). V_{CC} must also be powered in order for the JTAG state-machine to operate even if the device is in bypass mode; V_{JTAG} alone is insufficient. Both VJTAG and V_{CC} to the ProASIC3E part must be supplied to allow JTAG signals to transition the ProASIC3E device. Isolating the JTAG power supply in a separate I/O bank gives greater flexibility with supply selection and simplifies power supply and printed circuit board design. If the JTAG interface is neither used nor planned for use, the V_{JTAG} pin together with the TRST pin could be tied to GND.

TCK **Test Clock**

Test clock input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/down resistor. Actel recommends adding a nominal 20 kΩ pull-up resistor to this pin. If JTAG is not used, Actel recommends tying off TCK to GND or V_{JTAG} through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state.

Note that to operate at all V_{JTAG} voltages, 500 Ω to 1 kΩ will satisfy the requirements. Refer to Table 2-24 for more information.

Table 2-24 • **Recommended Tie-Off Values for the TCK and TRST Pins**

V_{JTAG}	Pull-Down Resistance*
V_{JTAG} at 3.3 V	200 Ω to 1 kΩ
V_{JTAG} at 2.5 V	200 Ω to 1 kΩ
V_{JTAG} at 1.8 V	500 Ω to 1 kΩ
V_{JTAG} at 1.5 V	500 Ω to 1 kΩ

Notes:

1. *Equivalent parallel resistance if more than one device is on JTAG chain.*
2. *The TSK pin can be pulled up/down.*
3. *The TRST pin can only be pulled down.*

Note that to operate at all V_{JTAG} voltages, 500 Ω to 1 kΩ will satisfy the requirements.

TDI **Test Data Input**

Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.

TDO **Test Data Output**

Serial output for JTAG boundary scan, ISP, and UJTAG usage.

TMS **Test Mode Select**

The TMS pin controls the use of the IEEE1532 boundary scan pins (TCK,TDI, TDO, TRST). There is an internal weak pull-up resistor on the TMS pin.

TRST **Boundary Scan Reset Pin**

The TRST pin functions as an active low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor could be included to ensure the TAP is held in reset mode. The resistor values must be chosen from Table 2-24 and must satisfy the parallel resistance value requirement. The values in Table 2-24 correspond to the resistor recommended when a single device is used and the equivalent parallel resistor when multiple devices are connected via a JTAG chain.

In critical applications, an upset in the JTAG circuit could allow entering an undesired JTAG state. In such cases, Actel recommends tying off TRST to GND through a resistor placed close to the FPGA pin.

Note that to operate at all V_{JTAG} voltages, 500 Ω to 1 kΩ will satisfy the requirements.

Special Function Pins

NC **No Connect**

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

DC **Don't Connect**

This pin should not be connected to any signals on the printed circuit board (PCB). These pins should be left unconnected.

Software Tools

Overview of Tools Flow

The ProASIC3E family of FPGAs is fully supported by both Actel Libero IDE and Designer FPGA Development software. Actel Libero IDE is an integrated design manager that seamlessly integrates design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Additionally, Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment (see the *Libero IDE flow diagram* located on the Actel website). Libero IDE includes Synplify® AE from Synplicity®, ViewDraw® AE from Mentor Graphics®, Model*Sim*® HDL Simulator from Mentor Graphics, WaveFormer Lite™ AE from SynaptiCAD®, PALACE™ AE Physical Synthesis from Magma Design Automation™, and Designer software from Actel.

Actel Designer software is a place-and-route tool and provides a comprehensive suite of backend support tools for FPGA development. The Designer software includes the following:

- Timer—a world-class integrated static timing analyzer and constraints editor that supports timing-driven place-and-route
- NetlistViewer—a design netlist schematic viewer
- ChipPlanner—a graphical floorplanner viewer and editor
- SmartPower—a tool that enables the designer to quickly estimate the power consumption of a design
- PinEditor—a graphical application for editing pin assignments and I/O attributes
- I/O Attribute Editor—a tool that displays all assigned and unassigned I/O macros and their attributes in a spreadsheet format

With the Designer software, a user can lock the design pins before layout while minimally impacting the results of place-and-route. Additionally, Actel back-annotation flow is compatible with all the major simulators. Another tool included in the Designer software is the SmartGen core generator, which easily creates popular and commonly used logic functions for implementation into your schematic or HDL design.

Actel Designer software is compatible with the most popular FPGA design entry and verification tools from EDA vendors, such as Mentor Graphics, Synplicity, Synopsys, and Cadence®. The Designer software is available for both the Windows® and UNIX operating systems.

Programming

Programming can be performed using tools such as Silicon Sculptor II (BP Micro Systems) or FlashPro3 (Actel).

The user can generate *.stp programming files from the Designer software and use these files to program a device.

ProASIC3E devices can be programmed in system. For more information on ISP of ProASIC3E devices, refer to the *In-System Programming (ISP) in ProASIC3/E Using FlashPro3* and *Programming a ProASIC3/E Using a Microprocessor* application notes.

The ProASIC3E device can be serialized with a unique identifier stored in the FlashROM of each device. Serialization is an automatic assignment of serial numbers that are stored within the STAPL file used for programming. The area of the FlashROM used for holding such identifiers is defined using SmartGen and the range of serial numbers to be used is defined at the time of STAPL file generation with FlashPoint. Serial number values for STAPL file generation can even be read from a file of predefined values. Serialized programming using a serialized STAPL file can be done through Actel In House Programming (IHP), an external vendor using Silicon Sculptor software, or via the ISP capabilities of the FlashPro software.

Security

ProASIC3E devices have a built-in 128-bit AES decryption core. The decryption core facilitates secure, in-system programming of the FPGA core array fabric and the FlashROM. The FlashROM and the FPGA core fabric can be programmed independently from each other, allowing the FlashROM to be updated without the need for change to the FPGA core fabric. The AES master key is stored in on-chip nonvolatile memory (Flash). The AES master key can be preloaded into parts in a secure programming environment (such as the Actel in-house programming center) and then "blank" parts can be shipped to an untrusted programming or manufacturing center for final personalization with an AES encrypted bitstream. Late stage product changes or personalization

can be implemented easily and securely by simply sending a STAPL file with AES encrypted data. Secure remote field updates over public networks (such as the Internet) are possible by sending and programming a STAPL file with AES encrypted data.

128-Bit AES Decryption

The 128-bit AES standard (FIPS-192) block cipher is the NIST (National Institute of Standards and Technology) replacement for the DES (Data Encryption Standard FIPS46-2). AES has been designed to protect sensitive government information well into the 21st century. It replaces the aging DES, which NIST adopted in 1977 as a Federal Information Processing Standard used by federal agencies to protect sensitive, unclassified information. The 128-bit AES standard has $3.4x10^{38}$ possible 128-bit key variants, and it has been estimated that it would take 1,000 trillion years to crack 128-bit AES cipher text using exhaustive techniques. Keys are stored (securely) in ProASIC3E devices in nonvolatile Flash memory. All programming files sent to the device can be authenticated by the part prior to programming to ensure that bad programming data is not loaded into the part that may possibly damage it. All programming verification is performed on-chip, ensuring that the contents of ProASIC3E devices remain secure.

AES decryption can also be used on the 1,024-bit FlashROM to allow for secure remote updates of the FlashROM contents. This allows for easy, secure support for subscription model products. See the application note *ProASIC3/E Security* for more details.

ISP

ProASIC3E devices support IEEE 1532 ISP via JTAG and require a single V_{PUMP} voltage of 3.3 V during programming. In addition, programming via a Microcontroller (MCU) in a target system can be achieved. See the application note *In-System Programming (ISP) in ProASIC3/E Using FlashPro3* for more details.

JTAG 1532

ProASIC3E devices support the JTAG-based IEEE 1532 standard for ISP. As part of this support, when a ProASIC3E device is in an unprogrammed state, all user I/O pins are disabled. This is achieved by keeping the global IO_EN signal deactivated, which also has the effect of disabling the input buffers. The SAMPLE/PRELOAD instruction captures the status of pads in parallel and shifts them out as new data is shift in for loading into the Boundary Scan Register. When the ProASIC3E device is in an unprogrammed state, the SAMPLE/PRELOAD instruction has no effect on I/O status, however, it will continue to shift in new data to be loaded into the BSR; therefore, when SAMPLE/PRELOAD is used on an unprogrammed device, the BSR will be loaded with undefined data. Refer to the *In-System Programming (ISP) in ProASIC3/E Using FlashPro3* application note for more details.

For JTAG timing information of setup, hold, and fall times, refer to the *FlashPro User's Guide*.

Boundary Scan

ProASIC3E devices are compatible with IEEE Standard 1149.1, which defines a hardware architecture and the set of mechanisms for boundary scan testing. The basic ProASIC3E boundary scan logic circuit is composed of the TAP (test access port) controller, test data registers, and instruction register (Figure 2-37 on page 2-55). This circuit supports all mandatory IEEE 1149.1 instructions (EXTEST, SAMPLE/PRELOAD, and BYPASS) and the optional IDCODE instruction (Table 2-25 on page 2-55).

Each test section is accessed through the TAP, which has five associated pins: TCK (test clock input), TDI, TDO (test data input and output), TMS (test mode selector), and TRST (test reset input). TMS, TDI, and TRST are equipped with pull-up resistors to ensure proper operation when no input data is supplied to them. These pins are dedicated for boundary scan test usage. Refer to the "JTAG Pins" section on page 2-52 for pull-up/down recommendations for TDO and TCK pins. The TAP controller is a 4-bit state machine (16 states) that operates as shown in Figure 2-37 on page 2-55. The 1s and 0s represent the values that must be present at TMS at a rising edge of TCK for the given state transition to occur. IR and DR indicate that the instruction register or the data register is operating in that state.

The TAP controller receives two control inputs (TMS and TCK) and generates control and clock signals for the rest of the test logic architecture. On power-up, the TAP controller enters the Test-Logic-Reset state. To guarantee a reset of the controller from any of the possible states, TMS must remain high for five TCK cycles. The TRST pin may also be used to asynchronously place the TAP controller in the Test-Logic-Reset state.

ProASIC3E devices support three types of test data registers: bypass, device identification, and boundary scan. The bypass register is selected when no other register needs to be accessed in a device. This speeds up test data transfer to other devices in a test data path. The 32-bit device identification register is a shift register with four fields (LSB, ID number, part number, and version). The boundary scan register observes and controls the state of each I/O pin. Each I/O cell has three boundary scan register cells, each with a serial-in, serial-out, parallel-in, and parallel-out pin.

The serial pins are used to serially connect all the boundary scan register cells in a device into a boundary scan register chain, which starts at the TDI pin and ends at the TDO pin. The parallel ports are connected to the internal core logic I/O tile and the input, output, and control ports of an I/O buffer to capture and load data into the register to control or observe the logic state of each I/O.

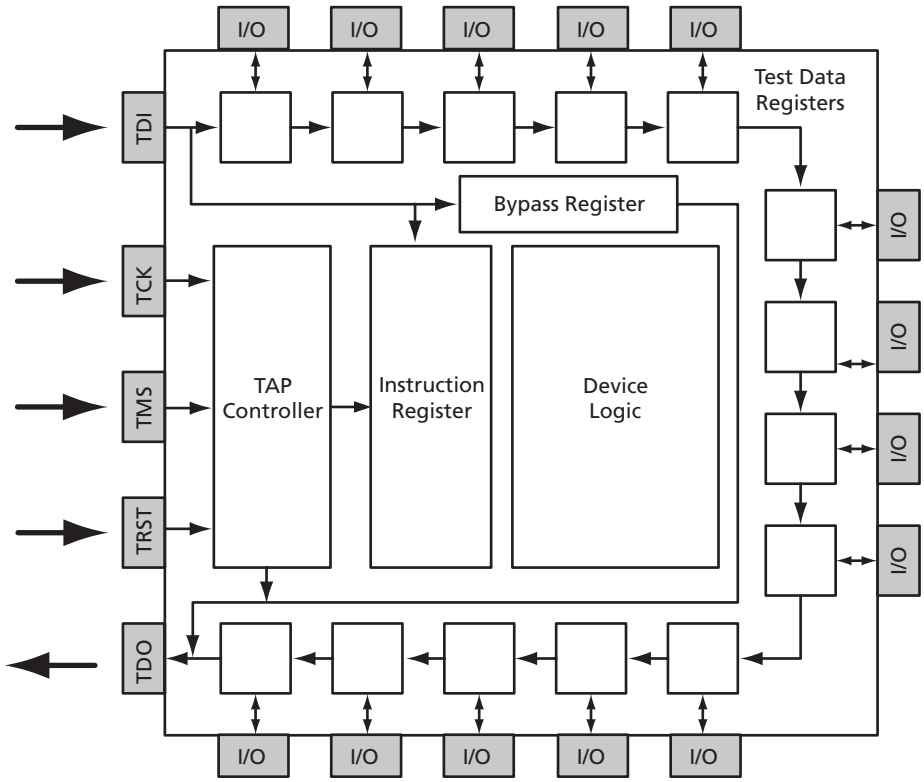


Figure 2-37 • **Boundary Scan Chain in ProASIC3E**

Table 2-25 • **Boundary Scan Opcodes**

	Hex Opcode
EXTEST	00
HIGHZ	07
USERCODE	0E
SAMPLE/PRELOAD	01
IDCODE	0F
CLAMP	05
BYPASS	FF