

DC and Switching Characteristics

General Specifications

DC and switching characteristics for –F speed grade targets are based only on simulation.

The characteristics provided for –F speed grade are subject to change after establishing FPGA specifications. Some restrictions might be added and will be reflected in future revisions of this document. The –F speed grade is only supported in the commercial temperature range.

Operating Conditions

Stresses beyond those listed in the [Table 3-1](#) may cause permanent damage to the device.

Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating ranges specified in [Table 3-2 on page 3-2](#).

Table 3-1 • Absolute Maximum Ratings

Symbol	Parameter	Limits	Units
V _{CC}	DC core supply voltage	–0.3 to 1.65	V
V _{JTAG}	JTAG DC voltage	–0.3 to 3.75	V
V _{PUMP}	Programming voltage	–0.3 to 3.75	V
V _{CCPLL}	Analog power supply (PLL)	–0.3 to 1.65	V
V _{CCI}	DC I/O output buffer supply voltage	–0.3 to 3.75	V
V _{MV}	DC I/O input buffer supply voltage	–0.3 to 3.75	V
V _I	I/O input voltage	–0.3 V to 3.6 V (when I/O hot insertion mode is enabled) –0.3 V to (V _{CCI} + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot-insertion mode is disabled)	V
T _{STG} ²	Storage Temperature	–65 to +150	°C
T _J ²	Junction Temperature	+125	°C

Notes:

1. The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in [Table 3-4 on page 3-2](#).
2. For Flash programming and retention maximum limits refer to [Table 3-4 on page 3-2](#) and for recommended operating limits refer to [Table 3-2 on page 3-2](#).

Table 3-2 • Recommended Operating Conditions

Symbol	Parameter	Commercial	Industrial	Units	
T_A, T_J	Ambient and Junction temperature	0 to +70	-40 to +85	°C	
V_{CC}	1.5 V DC core supply voltage	1.425 to 1.575	1.425 to 1.575	V	
V_{JTAG}	JTAG DC voltage	1.4 to 3.6	1.4 to 3.6	V	
V_{PUMP}	Programming voltage	Programming Mode	3.0 to 3.6	3.0 to 3.6	V
		Operation ³	0 to 3.6	0 to 3.6	V
V_{CCPLL}	Analog power supply (PLL)	1.4 to 1.6	1.4 to 1.6	V	
V_{CCI} and VMV	1.5 V DC supply voltage	1.425 to 1.575	1.425 to 1.575	V	
	1.8 V DC supply voltage	1.7 to 1.9	1.7 to 1.9	V	
	2.5 V DC supply voltage	2.3 to 2.7	2.3 to 2.7	V	
	3.3 V DC supply voltage	3.0 to 3.6	3.0 to 3.6	V	
	LVDS/BLVDS/M-LVDS differential I/O	2.375 to 2.625	2.375 to 2.625	V	
	LVPECL differential I/O	3.0 to 3.6	3.0 to 3.6	V	

Notes:

1. The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 3-14 on page 3-15. VMV and V_{CCI} should be at the same voltage within a given I/O bank.
2. All parameters representing voltages are measured with respect to GND unless otherwise specified.
3. V_{PUMP} can be left floating during operation (not programming mode).

Table 3-3 • Flash Programming Limits - Retention, Storage and Operating Temperature¹

Product Grade	Programming Cycles	Program Retention (Biased/Unbiased)	Maximum Storage Temperature T_{STG} (°C) ²	Maximum Operating Junction Temperature T_J (°C) ²
Commercial	500	20 years	110	110
Industrial	500	20 years	110	110

Notes:

1. This is a stress rating only, functional operation at any other condition other than those indicates is not implied.
2. These limits apply for program/data retention only. Refer to tables 3-1 and 3-2 for device operating conditions and absolute limits.

Table 3-4 • Overshoot and Undershoot Limits (as measured on quiet I/Os)¹

V_{CCI} and VMV	Average V_{CCI} -GND Overshoot or Undershoot Duration as Percentage of Clock Cycle ²	Maximum Overshoot/Undershoot ²
2.7 V or less	10%	1.4 V
	5%	1.49 V
3 V	10%	1.1 V
	5%	1.19 V
3.3 V	10%	0.79 V
	5%	0.88 V
3.6 V	10%	0.45 V
	5%	0.54 V

Notes:

1. Based on reliability requirements at 85°C.
2. The duration is allowed at one cycle out of six clock cycles (estimated SSO density over cycles). If the overshoot/undershoot occurs at one out of two cycles, then the maximum overshoot/undershoot has to be reduced by 0.15 V.

I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every ProASIC3 device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power-up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in Figure 3-1.

There are five regions to consider during power-up.

ProASIC3 I/Os are activated only if ALL of the following three conditions are met:

1. V_{CC} and V_{CCI} are above the minimum specified trip points (Figure 3-1).
2. $V_{CCI} > V_{CC} - 0.75\text{ V}$ (Typical).
3. Chip is in the operating mode.

V_{CCI} Trip Point:

Ramping up: $0.6\text{ V} < \text{trip_point_up} < 1.2\text{ V}$

Ramping down: $0.5\text{ V} < \text{trip_point_down} < 1.1\text{ V}$

V_{CC} Trip Point:

Ramping up: $0.6\text{ V} < \text{trip_point_up} < 1.1\text{ V}$

Ramping down: $0.5\text{ V} < \text{trip_point_down} < 1\text{ V}$

V_{CC} and V_{CCI} ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to V_{CCI} .
- JTAG supply, PLL power supplies, and charge pump V_{PUMP} supply have no influence on I/O behavior.

Internal Power-Up Activation Sequence

1. Core
2. Input buffers
3. Output buffers, after 200 ns delay from input buffer activation.

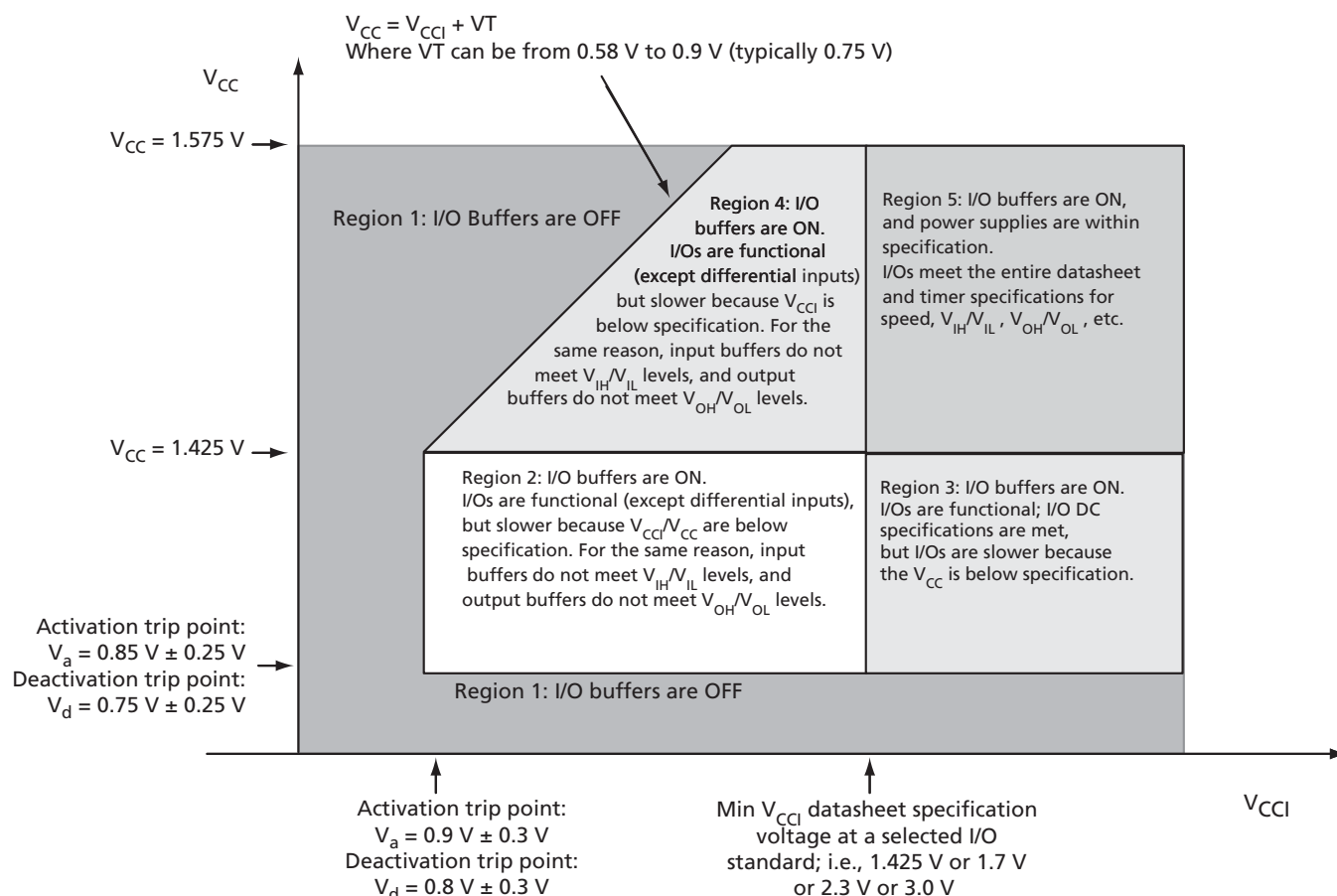


Figure 3-1 • I/O State as a Function of V_{CCI} and V_{CC} Voltage Levels

Thermal Characteristics

Introduction

The temperature variable in the Actel Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction to be higher than the ambient temperature.

EQ 3-1 can be used to calculate junction temperature.

$$T_J = \text{Junction Temperature} = \Delta T + T_A$$

EQ 3-1

Where T_A = Ambient Temperature

ΔT = Temperature gradient between junction (silicon) and ambient $\Delta T = \theta_{ja} * P$

θ_{ja} = Junction-to-ambient of the package. θ_{ja} numbers are located in Table 3-5.

P = Power dissipation

Package Thermal Characteristics

The device junction-to-case thermal resistivity is θ_{jc} and the junction-to-ambient air thermal resistivity is θ_{ja} . The thermal characteristics for θ_{ja} are shown for two air flow rates. The absolute maximum junction temperature is 110°C. EQ 3-2 shows a sample calculation of the absolute maximum power dissipation allowed for a 484-pin FBGA package at commercial temperature and still air.

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (}^\circ\text{C)} - \text{Max. ambient temp. (}^\circ\text{C)}}{\theta_{ja} (^\circ\text{C/W)}} = \frac{150^\circ\text{C} - 70^\circ\text{C}}{20.5^\circ\text{C/W}} = 3.90 \text{ W}$$

EQ 3-2

Table 3-5 • Package Thermal Resistivities

Package Type	Pin Count	θ_{jc}	θ_{ja}			Units
			Still Air	200 ft./min.	500 ft./min.	
Quad Flat No Lead (QFN)	132	13.2	28.9	24.6	23.1	C/W
Very Thin Quad Flat Pack (VQFP)	100	10.0	35.3	29.4	27.1	C/W
Thin Quad Flat Pack (TQFP)	144	11.0	33.5	28.0	25.7	C/W
Plastic Quad Flat Package (PQFP)	208	8.0	26.1	22.5	20.8	C/W
Plastic Quad Flat Package (PQFP) with embedded heat spreader	208	3.8	16.2	13.3	11.9	C/W
Fine Pitch Ball Grid Array (FBGA)	144	3.8	26.9	22.9	21.5	C/W
	256	3.8	26.6	22.8	21.5	C/W
	484	3.2	20.5	17.0	15.9	C/W

Temperature and Voltage Derating Factors

Table 3-6 • Temperature and Voltage Derating Factors for Timing Delays (Normalized to $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425 \text{ V}$)

Array Voltage V_{CC} (V)	Junction Temperature ($^\circ\text{C}$)					
	-40°C	0°C	25°C	70°C	85°C	110°C
1.425	0.88	0.93	0.95	1.00	1.02	1.05
1.500	0.83	0.87	0.89	0.94	0.96	0.98
1.575	0.80	0.84	0.86	0.91	0.92	0.95

Calculating Power Dissipation

Quiescent Supply Current

Table 3-7 • Quiescent Supply Current Characteristics

	A3P030	A3P060	A3P125	A3P250	A3P400	A3P600	A3P1000
Typical (25°C)	2 mA	2 mA	2 mA	3 mA	3 mA	5 mA	8 mA
Maximum (Commercial)	10 mA	10 mA	10 mA	20 mA	20 mA	30 mA	50 mA
Maximum (Industrial)	15 mA	15 mA	15 mA	30 mA	30 mA	45 mA	75 mA

Notes:

- I_{DD} includes V_{CC} , V_{PUMP} , V_{CCI} , and VMV currents. Values do not include I/O static contribution, which is shown in Table 3-8 and Table 3-9 on page 3-6.
- F speed grade devices may experience higher standby I_{DD} of up to five times the standard I_{DD} and higher I/O leakage.

Power Per I/O Pin

Table 3-8 • Summary of I/O Input Buffer Power (Per Pin) – Default I/O Software Settings

	VMV (V)	Static Power P_{DC2} (mW) ¹	Dynamic Power P_{AC9} (μW/MHz) ²
Single-Ended			
3.3 V LVTTTL / 3.3 V LVCMOS	3.3	–	16.69
2.5 V LVCMOS	2.5	–	5.12
1.8 V LVCMOS	1.8	–	2.13
1.5 V LVCMOS (JESD8-11)	1.5	–	1.45
3.3 V PCI	3.3	–	18.11
3.3 V PCI-X	3.3	–	18.11
Differential			
LVDS/BLVDS/M-LVDS	2.5	2.26	1.20
LVPECL	3.3	5.72	1.87

Notes:

- P_{DC2} is the static power (where applicable) measured on VMV.
- P_{AC9} is the total dynamic power measured on V_{CC} and VMV.

Table 3-9 • Summary of I/O Output Buffer Power (Per Pin) – Default I/O Software Settings¹
Applicable to Advanced I/O Banks

	C _{LOAD} (pF)	V _{CCI} (V)	Static Power P _{DC3} (mW) ²	Dynamic Power P _{AC10} (μW/MHz) ³
Single-Ended				
3.3 V LVTTTL / 3.3 V LVCMOS	35	3.3	–	468.67
2.5 V LVCMOS	35	2.5	–	267.48
1.8 V LVCMOS	35	1.8	–	149.46
1.5 V LVCMOS (JESD8-11)	35	1.5	–	103.12
3.3 V PCI	10	3.3	–	201.02
3.3 V PCI-X	10	3.3	–	201.02
Differential				
LVDS	–	2.5	7.74	88.92
LVPECL	–	3.3	19.54	166.52

Notes:

1. Dynamic power consumption is given for standard load and software default drive strength and output slew.
2. P_{DC3} is the static power (where applicable) measured on V_{CCI}.
3. P_{AC10} is the total dynamic power measured on V_{CC} and V_{CCI}.

Table 3-10 • Summary of I/O Output Buffer Power (Per Pin) – Default I/O Software Settings¹
Applicable to Standard+ I/O Banks

	C _{LOAD} (pF)	V _{CCI} (V)	Static Power P _{DC3} (mW) ²	Dynamic Power P _{AC10} (μW/MHz) ³
Single-Ended				
3.3 V LVTTTL / 3.3 V LVCMOS	35	3.3	–	452.67
2.5 V LVCMOS	35	2.5	–	258.32
1.8 V LVCMOS	35	1.8	–	133.59
1.5 V LVCMOS (JESD8-11)	35	1.5	–	92.84
3.3 V PCI	10	3.3	–	184.92
3.3 V PCI-X	10	3.3	–	184.92

Notes:

1. Dynamic power consumption is given for standard load and software default drive strength and output slew.
2. P_{DC3} is the static power (where applicable) measured on V_{CCI}.
3. P_{AC10} is the total dynamic power measured on V_{CC} and V_{CCI}.

Power Consumption of Various Internal Resources

Table 3-11 • Different Components Contributing to Dynamic Power Consumption in ProASIC3 Devices

Parameter	Definition	Device Specific Dynamic Power ($\mu\text{W}/\text{MHz}$)						
		A3P030	A3P060	A3P125	A3P250	A3P400	A3P600	A3P1000
P _{AC1}	Clock contribution of a Global Rib	1.80	1.80	3.53	3.53	5.27	5.27	6.98
P _{AC2}	Clock contribution of a Global Spine	0.41	0.81	0.81	1.58	1.35	1.85	2.48
P _{AC3}	Clock contribution of a VersaTile row	0.81						
P _{AC4}	Clock contribution of a VersaTile used as a sequential module	0.12						
P _{AC5}	First contribution of a VersaTile used as a sequential module	0.07						
P _{AC6}	Second contribution of a VersaTile used as a sequential module	0.29						
P _{AC7}	Contribution of a VersaTile used as a combinatorial Module	0.29						
P _{AC8}	Average contribution of a routing net	0.70						
P _{AC9}	Contribution of an I/O input pin (standard dependent)	See Table 3-8 on page 3-5.						
P _{AC10}	Contribution of an I/O output pin (standard dependent)	See Table 3-9 and Table 3-10 on page 3-6.						
P _{AC11}	Average contribution of a RAM block during a read operation	25.00						
P _{AC12}	Average contribution of a RAM block during a write operation	30.00						
P _{AC13}	First contribution of a PLL	4.00						
P _{AC14}	Second contribution of a PLL	2.00						

Note: *For a different output load, drive strength, or slew rate, Actel recommends using the Actel Power spreadsheet calculator or SmartPower tool in Libero IDE software.

Power Calculation Methodology

The section below describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in Actel Libero IDE software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in [Table 3-12 on page 3-10](#)
- Enable rates of output buffers—guidelines are provided for typical applications in [Table 3-13 on page 3-10](#)
- Read rate and write rate to the memory—guidelines are provided for typical applications in [Table 3-13 on page 3-10](#). The calculation should be repeated for each clock domain defined in the design.

Methodology

Total Power Consumption— P_{TOTAL}

$$P_{TOTAL} = P_{STAT} + P_{DYN}$$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

Total Static Power Consumption— P_{STAT}

$$P_{STAT} = P_{DC1} + N_{INPUTS} * P_{DC2} + N_{OUTPUTS} * P_{DC3}$$

N_{INPUTS} is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

Total Dynamic Power Consumption— P_{DYN}

$$P_{DYN} = P_{CLOCK} + P_{S-CELL} + P_{C-CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL} + P_{AC4}$$

Global Clock Contribution— P_{CLOCK}

$$P_{CLOCK} = (P_{AC1} + N_{SPINE} * P_{AC2} + N_{ROW} * P_{AC3} + N_{S-CELL} * P_{AC4}) * F_{CLK}$$

N_{SPINE} is the number of global spines used in the user design—guideline are provided in [Table 3-12 on page 3-10](#).

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in [Table 3-12 on page 3-10](#).

F_{CLK} is the global clock signal frequency.

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design.

P_{AC1} , P_{AC2} , P_{AC3} , and P_{AC4} are device dependent.

Sequential Cells Contribution— P_{S-CELL}

$$P_{S-CELL} = N_{S-CELL} * (P_{AC5} + \alpha_1/2 * P_{AC6}) * F_{CLK}$$

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in [Table 3-12 on page 3-10](#).

F_{CLK} is the global clock signal frequency.

Combinational Cells Contribution— P_{C-CELL}

$$P_{C-CELL} = N_{C-CELL} * \alpha_1/2 * P_{AC7} * F_{CLK}$$

N_{C-CELL} is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in [Table 3-12 on page 3-10](#).

F_{CLK} is the global clock signal frequency.

Routing Net Contribution— P_{NET}

$$P_{NET} = (N_{S-CELL} + N_{C-CELL}) * \alpha_1/2 * P_{AC8} * F_{CLK}$$

N_{S-CELL} is the number VersaTiles used as sequential modules in the design.

N_{C-CELL} is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in [Table 3-12 on page 3-10](#).

F_{CLK} is the global clock signal frequency.

I/O Input Buffer Contribution— P_{INPUTS}

$$P_{INPUTS} = N_{INPUTS} * \alpha_2/2 * P_{AC9} * F_{CLK}$$

N_{INPUTS} is the number of I/O input buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in [Table 3-12 on page 3-10](#).

F_{CLK} is the global clock signal frequency.

I/O Output Buffer Contribution— $P_{OUTPUTS}$

$$P_{OUTPUTS} = N_{OUTPUTS} * \alpha_2/2 * \beta_1 * P_{AC10} * F_{CLK}$$

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in [Table 3-12 on page 3-10](#).

β_1 is the I/O buffer enable rate—guidelines are provided in [Table 3-13 on page 3-10](#).

F_{CLK} is the global clock signal frequency.

RAM Contribution— P_{MEMORY}

$$P_{MEMORY} = P_{AC11} * N_{BLOCKS} * F_{READ-CLOCK} * \beta_2 + P_{AC12} * N_{BLOCK} * F_{WRITE-CLOCK} * \beta_3$$

N_{BLOCKS} is the number RAM blocks used in the design.

$F_{READ-CLOCK}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations.

$F_{WRITE-CLOCK}$ is the memory write clock frequency.

β_3 the RAM enable rate for write operations—guidelines are provided in [Table 3-13 on page 3-10](#).

PLL/CCC Contribution— P_{PLL}

$$P_{PLL} = P_{AC13} * F_{CLKIN} + \sum P_{AC14} * F_{CLKOUT}$$

F_{CLKIN} is the input clock frequency.

F_{CLKOUT} is the output clock frequency.¹

1. The PLL dynamic contribution depends on the input clock frequency, the number of output clock signals generated by the PLL, and the frequency of each output clock. If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution ($P_{AC14} * F_{CLKOUT}$ product) to the total PLL contribution.

Guidelines

Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that this net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift-register is 100% because all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
 - Bit 0 (LSB) = 100%
 - Bit 1 = 50%

- Bit 2 = 25%
- ...
- Bit 7 (MSB) = 0.78125%
- The average toggle rate is = $(100\% + 50\% + 25\% + 12.5\% + \dots + 0.78125\%) / 8$.

Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When nontristate output buffers are used, the enable rate should be 100%.

Table 3-12 • Toggle Rate Guidelines Recommended for Power Calculation

Component	Definition	Guideline
α_1	Toggle rate of VersaTile outputs	10%
α_2	I/O buffer toggle rate	10%

Table 3-13 • Enable Rate Guidelines Recommended for Power Calculation

Component	Definition	Guideline
β_1	I/O output buffer enable rate	100%
β_2	RAM enable rate for read operations	12.5%
β_3	RAM enable rate for write operations	12.5%

User I/O Characteristics

Timing Model

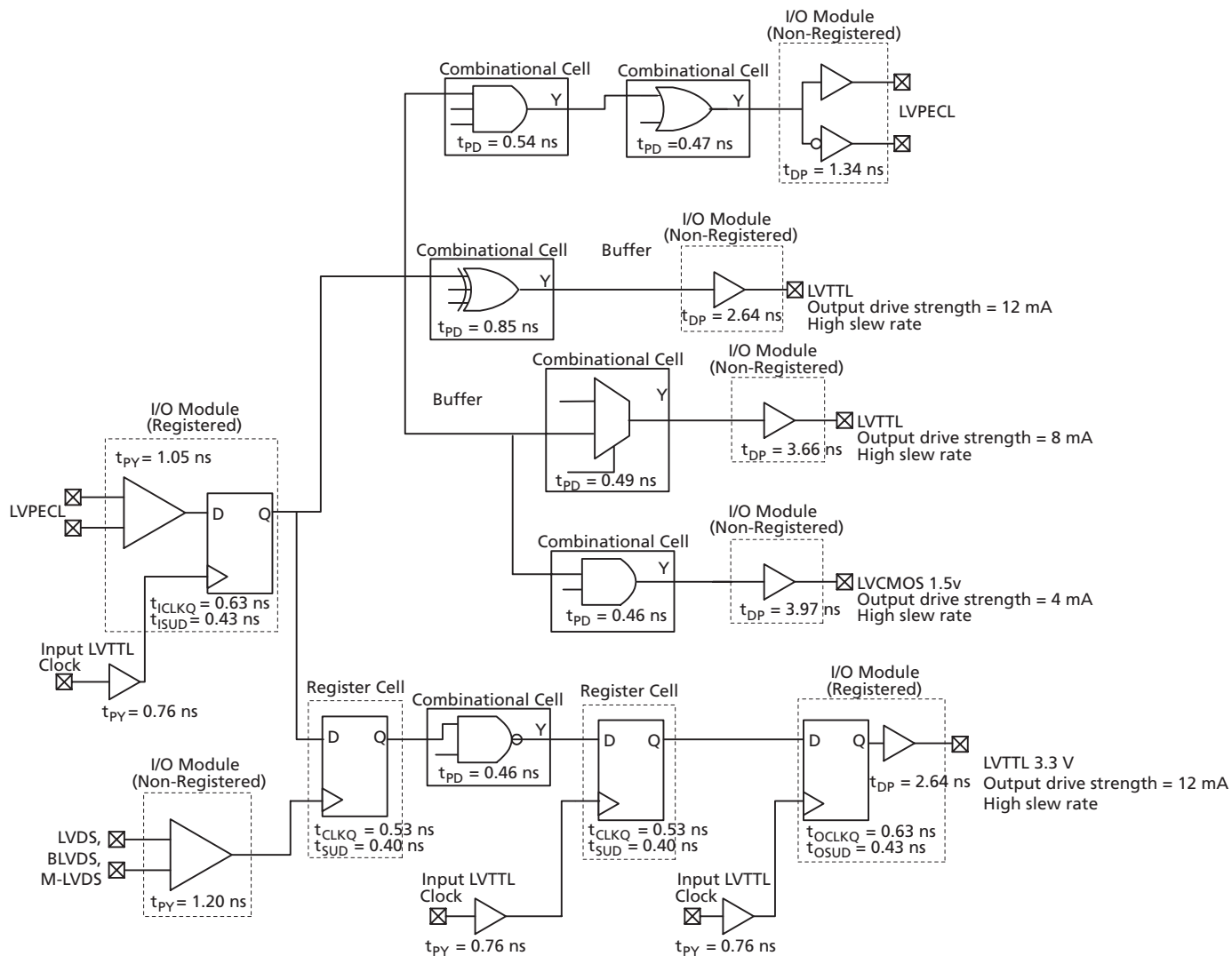


Figure 3-2 • Timing Model

Operating Conditions: -2 Speed, Commercial Temperature Range ($T_j = 70^\circ\text{C}$), Worst Case $V_{CC} = 1.425$ V

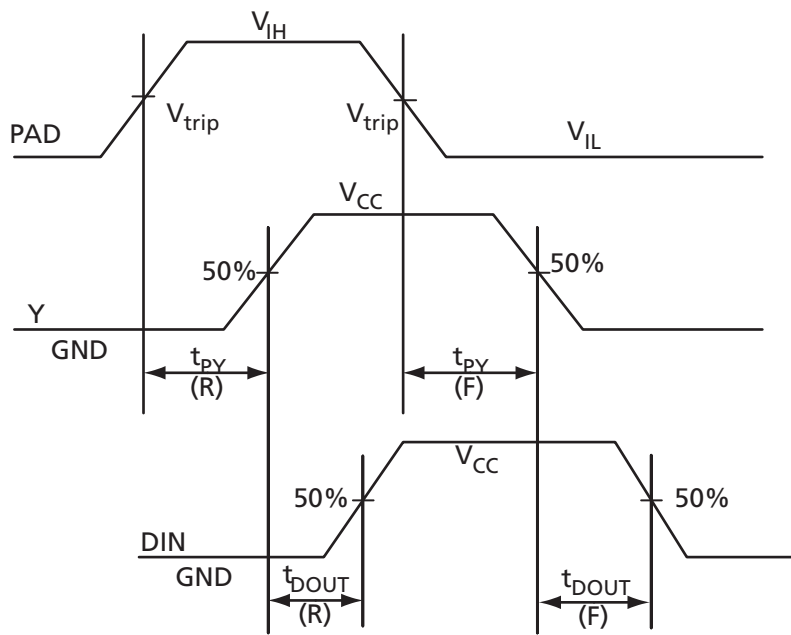
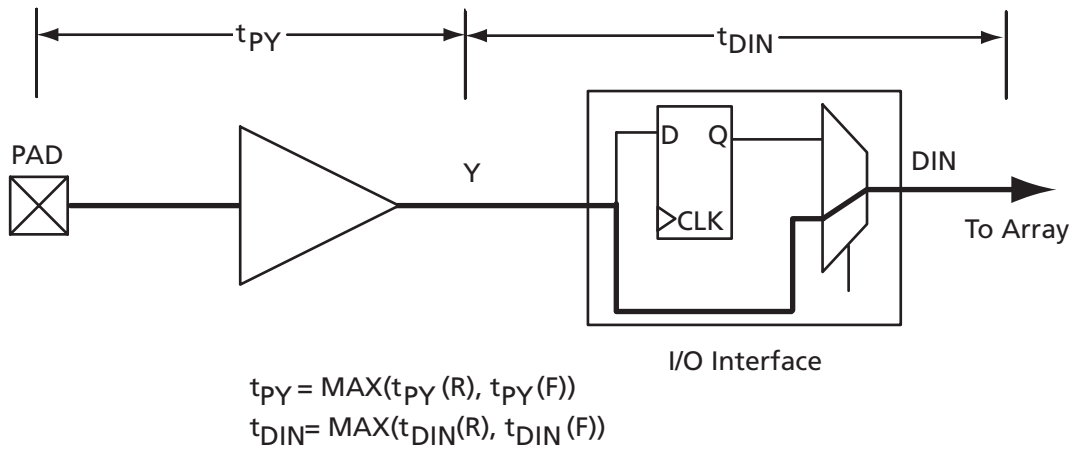


Figure 3-3 • Input Buffer Timing Model and Delays (example)

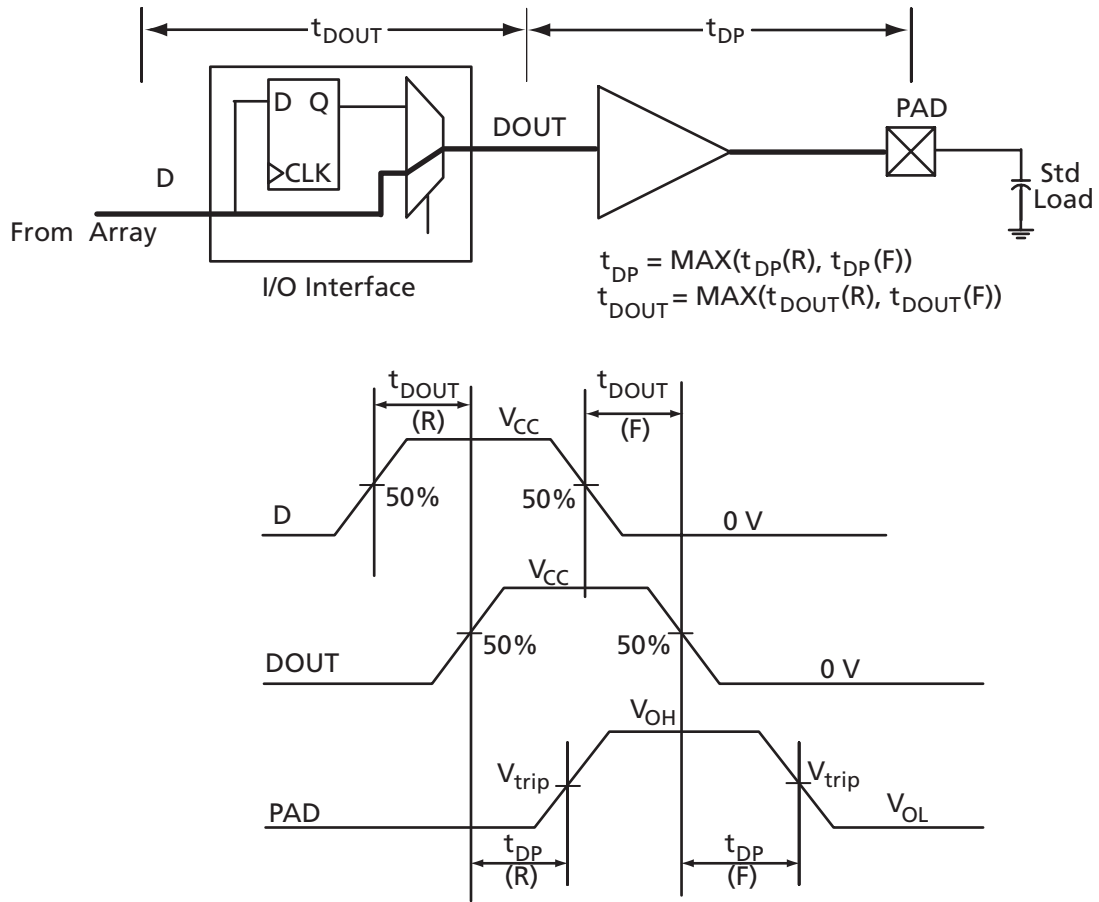


Figure 3-4 • Output Buffer Model and Delays (example)

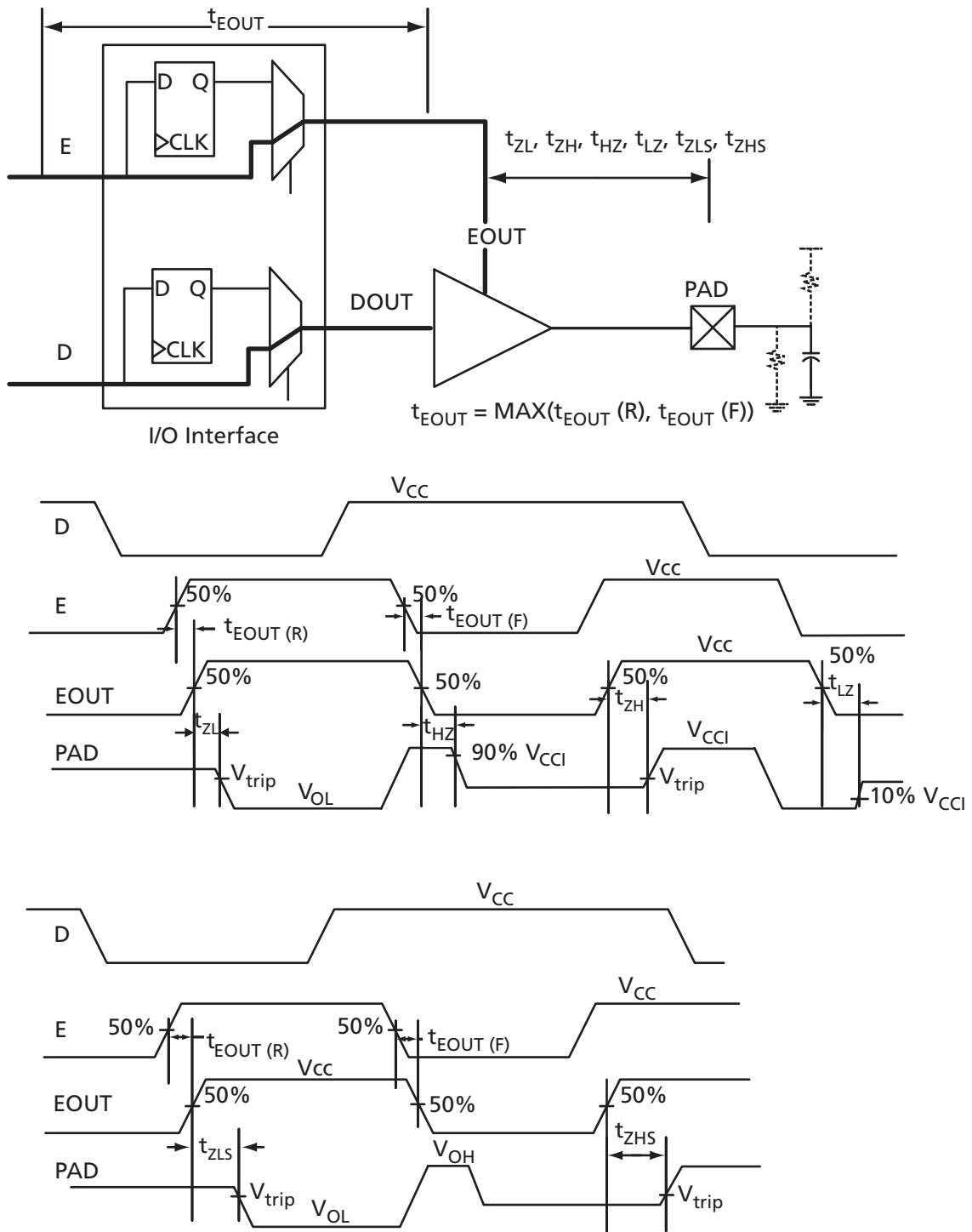


Figure 3-5 • Tristate Output Buffer Timing Model and Delays (example)

Overview of I/O Performance

Summary of I/O DC Input and Output Levels – Default I/O Software Settings

Table 3-14 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions
Applicable to Advanced I/O Banks

I/O Standard	Drive Strength	Slew Rate	V _{IL}		V _{IH}		V _{OL}	V _{OH}	I _{OL}	I _{OH}
			Min, V	Max, V	Min, V	Max, V	Max, V	Min, V	mA	mA
3.3 V LVTTTL / 3.3 V LVCMOS	12 mA	High	-0.3	0.8	2	3.6	0.4	2.4	12	12
2.5 V LVCMOS	12 mA	High	-0.3	0.7	1.7	3.6	0.7	1.7	12	12
1.8 V LVCMOS	12 mA	High	-0.3	0.35 * V _{CCI}	0.65 * V _{CCI}	3.6	0.45	V _{CCI} - 0.45	12	12
1.5 V LVCMOS	12 mA	High	-0.3	0.30 * V _{CCI}	0.7 * V _{CCI}	3.6	0.25 * V _{CCI}	0.75 * V _{CCI}	12	12
3.3 V PCI	Per PCI specifications									
3.3 V PCI-X	Per PCI-X specifications									

Notes:

1. Currents are measured at 85°C junction temperature.
2. V_{IH} is applied when hot-swap is applied.
3. A3P030 only supports hot-swap.

Table 3-15 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions
Applicable to Standard+ I/O Banks

I/O Standard	Drive Strength	Slew Rate	V _{IL}		V _{IH}		V _{OL}	V _{OH}	I _{OL}	I _{OH}
			Min, V	Max, V	Min, V	Max, V	Max, V	Min, V	mA	mA
3.3 V LVTTTL / 3.3 V LVCMOS	12 mA	High	-0.3	0.8	2	3.6	0.4	2.4	12	12
2.5 V LVCMOS	12 mA	High	-0.3	0.7	1.7	3.6	0.7	1.7	12	12
1.8 V LVCMOS	8 mA	High	-0.3	0.35 * V _{CCI}	0.65 * V _{CCI}	3.6	0.45	V _{CCI} - 0.45	8	8
1.5 V LVCMOS	4 mA	High	-0.3	0.30 * V _{CCI}	0.7 * V _{CCI}	3.6	0.25 * V _{CCI}	0.75 * V _{CCI}	4	4
3.3 V PCI	Per PCI specifications									
3.3 V PCI-X	Per PCI-X specifications									

Notes:

1. Currents are measured at 85°C junction temperature.
2. V_{IH} is applied when hot-swap is applied.
3. A3P030 only supports hot-swap.

Table 3-16 • Summary of Maximum and Minimum DC Input Levels Applicable to Commercial and Industrial Conditions

DC I/O Standards	Commercial ¹		Industrial ²	
	I _{IL}	I _{IH}	I _{IL}	I _{IH}
	μA	μA	μA	μA
3.3 V LVTTTL /3.3V LVCMOS	10	10	15	15
2.5 V LVCMOS	10	10	15	15
1.8 V LVCMOS	10	10	15	15
1.5 V LVCMOS	10	10	15	15
3.3 V PCI	10	10	15	15
3.3 V PCI-X	10	10	15	15

Notes:

1. Commercial range (0°C < T_J < 70°C)
2. Industrial range (-40°C < T_J < 85°C)

Summary of I/O Timing Characteristics – Default I/O Software Settings

Table 3-17 • Summary of AC Measuring Points

Standard	Measuring Trip Point (V _{trip})
3.3 V LVTTTL / 3.3 V LVCMOS	1.4 V
2.5 V LVCMOS	1.2 V
1.8 V LVCMOS	0.90 V
1.5 V LVCMOS	0.75 V
3.3 V PCI	0.285 * V _{CC1} (RR)
	0.615 * V _{CC1} (FF)
3.3 V PCI-X	0.285 * V _{CC1} (RR)
	0.615 * V _{CC1} (FF)

Table 3-18 • I/O AC Parameter Definitions

Parameter	Parameter Definition
t _{DP}	Data to Pad delay through the Output Buffer
t _{PY}	Pad to Data delay through the Input Buffer
t _{DOUT}	Data to Output Buffer delay through the I/O interface
t _{EOUT}	Enable to Output Buffer Tristate Control delay through the I/O interface
t _{DIN}	Input Buffer to Data delay through the I/O interface
t _{HZ}	Enable to Pad delay through the Output Buffer—high to Z
t _{ZH}	Enable to Pad delay through the Output Buffer—Z to high
t _{LZ}	Enable to Pad delay through the Output Buffer—low to Z
t _{ZL}	Enable to Pad delay through the Output Buffer—Z to low
t _{ZHS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to high
t _{ZLS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to low

Table 3-19 • Summary of I/O Timing Characteristics—Software Default Settings
 –2 Speed Grade, Commercial-Case Conditions: $T_j = 70^\circ\text{C}$, Worst Case $V_{CC} = 1.425\text{ V}$, Worst Case $V_{CCI} = 3.0\text{ V}$
 Advanced I/O Banks

I/O Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
3.3 V LVTTTL / 3.3 V LVCMOS	12 mA	High	35 pF	–	0.49	2.64	0.03	0.76	0.32	2.69	2.11	2.40	2.68	4.36	3.78	ns
2.5 V LVCMOS	12 mA	High	35pF	–	0.49	2.66	0.03	0.98	0.32	2.71	2.56	2.47	2.57	4.38	4.23	ns
1.8 V LVCMOS	12 mA	High	35pF	–	0.49	2.64	0.03	0.91	0.32	2.69	2.27	2.76	3.05	4.36	3.94	ns
1.5 V LVCMOS	12 mA	High	35pF	–	0.49	3.05	0.03	1.07	0.32	3.10	2.67	2.95	3.14	4.77	4.34	ns
3.3 V PCI	Per PCI specification	High	10pF	25^2	0.49	2.00	0.03	0.65	0.32	2.04	1.46	2.40	2.68	3.71	3.13	ns
3.3 V PCI-X	Per PCI-X specification	High	10pF	25^2	0.49	2.00	0.03	0.65	0.32	2.04	1.46	2.40	2.68	3.71	3.13	ns
LVDS	24 mA	High	–	–	0.49	1.37	0.03	1.20	–	–	–	–	–	–	–	ns
LVPECL	24 mA	High	–	–	0.49	1.34	0.03	1.05	–	–	–	–	–	–	–	ns

Notes:

1. For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.
2. Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 3-10 on page 3-42 for connectivity. This resistor is not required during normal operation.

Table 3-20 • Summary of I/O Timing Characteristics—Software Default Settings
 –2 Speed Grade, Commercial-Case Conditions: $T_j = 70^\circ\text{C}$, Worst Case $V_{CC} = 1.425\text{ V}$, Worst Case $V_{CCI} = 3.0\text{ V}$
 Standard+ I/O Banks

I/O Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
3.3 V LVTTTL / 3.3 V LVCMOS	12 mA	High	35 pF	–	0.49	2.36	0.03	0.75	0.32	2.40	1.93	2.08	2.41	4.07	3.60	ns
2.5 V LVCMOS	12 mA	High	35pF	–	0.49	2.39	0.03	0.97	0.32	2.44	2.35	2.11	2.32	4.11	4.02	ns
1.8 V LVCMOS	8 mA	High	35pF	–	0.49	3.03	0.03	0.90	0.32	2.87	3.03	2.19	2.32	4.54	4.70	ns
1.5 V LVCMOS	4 mA	High	35pF	–	0.49	3.61	0.03	1.06	0.32	3.35	3.61	2.26	2.34	5.02	5.28	ns
3.3 V PCI	Per PCI specification	High	10pF	25^2	0.49	1.72	0.03	0.64	0.32	1.76	1.27	2.08	2.41	3.42	2.94	ns
3.3 V PCI-X	Per PCI-X specification	High	10pF	25^2	0.49	1.72	0.03	0.64	0.32	1.76	1.27	2.08	2.41	3.42	2.94	ns

Notes:

1. For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.
2. Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 3-10 on page 3-42 for connectivity. This resistor is not required during normal operation.

Detailed I/O DC Characteristics

Table 3-21 • Input Capacitance

Symbol	Definition	Conditions	Min.	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0, f = 1.0 MHz		8	pF
C _{INCLK}	Input Capacitance on the clock pin	V _{IN} = 0, f = 1.0 MHz		8	pF

Table 3-22 • I/O Output Buffer Maximum Resistances¹
Applicable to Advanced I/O Banks

Standard	Drive Strength	R _{PULL-DOWN}	R _{PULL-UP}
		(Ω) ²	(Ω) ³
3.3 V LVTTTL/ 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
	12 mA	25	50
	16 mA	20	40
	24 mA	11	22
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
	12 mA	20	22
	16 mA	20	22
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
	6 mA	67	75
	8 mA	33	37
	12 mA	33	37
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75

Notes:

1. These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on V_{CC_I}, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Actel website at <http://www.actel.com/techdocs/models/ibis.html>.
2. $R_{(PULL-DOWN-MAX)} = (V_{OLspec}) / I_{OLspec}$
3. $R_{(PULL-UP-MAX)} = (V_{CCImax} - V_{OHspec}) / I_{OHspec}$

Table 3-23 • I/O Output Buffer Maximum Resistances¹
Applicable to Standard+ I/O Banks

Standard	Drive Strength	R _{PULL-DOWN}	R _{PULL-UP}
		(Ω) ²	(Ω) ³
3.3 V LVTTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	25	75
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
	12 mA	25	50
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75

Notes:

1. These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on V_{CCi} , drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Actel website at <http://www.actel.com/techdocs/models/ibis.html>.
2. $R_{(PULL-DOWN-MAX)} = (V_{OLspec}) / I_{OLspec}$
3. $R_{(PULL-UP-MAX)} = (V_{CCimax} - V_{OHspec}) / I_{OHspec}$

Table 3-24 • I/O Weak Pull-Up/Pull-Down Resistances
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values

V _{CCi}	R _(WEAK PULL-UP) ¹ (Ω)		R _(WEAK PULL-DOWN) ² (Ω)	
	Min.	Max.	Min.	Max.
3.3 V	10 k	45 k	10 k	45 k
2.5 V	11 k	55 k	12 k	74 k
1.8 V	18 k	70 k	17 k	110 k
1.5 V	19 k	90 k	19 k	140 k

Notes:

1. $R_{(WEAK PULL-UP-MAX)} = (V_{OLspec}) / I_{(WEAK PULL-UP-MIN)}$
2. $R_{(WEAK PULL-UP-MAX)} = (V_{CCimax} - V_{OHspec}) / I_{(WEAK PULL-UP-MIN)}$

Table 3-25 • I/O Short Currents I_{OSH}/I_{OSL}
Applicable to Advanced I/O Banks

	Drive Strength	I_{OSH} (mA)*	I_{OSL} (mA)*
3.3 V LVTTTL / 3.3 V LVCMOS	2 mA	27	25
	4 mA	27	25
	6 mA	54	51
	8 mA	54	51
	12 mA	109	103
	16 mA	127	132
	24 mA	181	268
3.3 V LVCMOS	2 mA	27	25
	4 mA	27	25
	6 mA	54	51
	8 mA	54	51
	12 mA	109	103
	16 mA	127	132
	24 mA	181	268
2.5 V LVCMOS	2 mA	18	16
	4 mA	18	16
	6 mA	37	32
	8 mA	37	32
	12 mA	74	65
	16 mA	87	83
	24 mA	124	169
1.8 V LVCMOS	2 mA	11	9
	4 mA	22	17
	6 mA	44	35
	8 mA	51	45
	12 mA	74	91
	16 mA	74	91
1.5 V LVCMOS	2 mA	16	13
	4 mA	33	25
	6 mA	39	32
	8 mA	55	66
	12 mA	55	66
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	109	103

Note: * $T_J = 100^\circ\text{C}$

Table 3-26 • I/O Short Currents I_{OSH}/I_{OSL}
Applicable to Standard+ I/O Banks

	Drive Strength	I_{OSH} (mA)*	I_{OSL} (mA)*
3.3 V LVTTTL / 3.3 V LVCMOS	2 mA	27	25
	4 mA	27	25
	6 mA	54	51
	8 mA	54	51
	12 mA	109	103
	16 mA	109	103
2.5 V LVCMOS	2 mA	18	16
	4 mA	18	16
	6 mA	37	32
	8 mA	37	32
	12 mA	74	65
1.8 V LVCMOS	2 mA	11	9
	4 mA	22	17
	6 mA	44	35
	8 mA	44	35
1.5 V LVCMOS	2 mA	16	13
	4 mA	33	25
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	109	103

Note: * $T_J = 100^\circ\text{C}$

The length of time an I/O can withstand I_{OSH}/I_{OSL} events depends on the junction temperature. The reliability data below is based on a 3.3 V, 12 mA I/O setting, which is the worst case for this type of analysis.

For example, at 110°C , the short current condition would have to be sustained for more than three months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

Table 3-27 • Short Current Event Duration before Failure

Temperature	Time Before Failure
-40°C	> 20 years
0°C	> 20 years
25°C	> 20 years
70°C	5 years
85°C	2 years
100°C	6 months
110°C	3 months

Table 3-28 • I/O Input Rise Time, Fall Time, and Related I/O Reliability

Input Buffer	Input Rise/Fall Time (Min.)	Input Rise/fall Time (Max.)	Reliability
LVTTTL/LVCMOS	No requirement	10 ns *	20 years (110°C)
LVDS/BLVDS.M-LVDS/LVPECL	No requirement	10 ns *	10 years (100°C)

Note: *The maximum input rise/fall time is related to the noise induced into the input buffer trace. If the noise is low, then the rise time and fall time of input buffers, when Schmitt trigger is disabled, can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Actel recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals.

Single-Ended I/O Characteristics

3.3 V LVTTTL / 3.3 V LVCMOS

Low-Voltage Transistor-Transistor Logic (LVTTTL) is a general purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTTL input buffer and push-pull output buffer.

Table 3-29 • Minimum and Maximum DC Input and Output Levels
Applicable to Advanced I/O Banks

3.3 V LVTTTL / 3.3 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
	Min, V	Max, V	Min, V	Max, V	Max, V	Min, V	mA	mA	Max, mA ¹	Max, mA ¹	μA^2	μA^2
2 mA	-0.3	0.8	2	3.6	0.4	2.4	2	2	27	25	10	10
4 mA	-0.3	0.8	2	3.6	0.4	2.4	4	4	27	25	10	10
6 mA	-0.3	0.8	2	3.6	0.4	2.4	6	6	54	51	10	10
8 mA	-0.3	0.8	2	3.6	0.4	2.4	8	8	54	51	10	10
12 mA	-0.3	0.8	2	3.6	0.4	2.4	12	12	109	103	10	10
16 mA	-0.3	0.8	2	3.6	0.4	2.4	16	16	127	132	10	10
24 mA	-0.3	0.8	2	3.6	0.4	2.4	24	24	181	268	10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.
3. Software default selection highlighted in gray.

Table 3-30 • Minimum and Maximum DC Input and Output Levels
Applicable to Standard+ I/O Banks

3.3 V LVTTTL / 3.3 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
	Min, V	Max, V	Min, V	Max, V	Max, V	Min, V	mA	mA	Max, mA ¹	Max, mA ¹	μA^2	μA^2
2 mA	-0.3	0.8	2	3.6	0.4	2.4	2	2	27	25	10	10
4 mA	-0.3	0.8	2	3.6	0.4	2.4	4	4	27	25	10	10
6 mA	-0.3	0.8	2	3.6	0.4	2.4	6	6	54	51	10	10
8 mA	-0.3	0.8	2	3.6	0.4	2.4	8	8	54	51	10	10
12 mA	-0.3	0.8	2	3.6	0.4	2.4	12	12	109	103	10	10
16 mA	-0.3	0.8	2	3.6	0.4	2.4	16	16	109	103	10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.
3. Software default selection highlighted in gray.

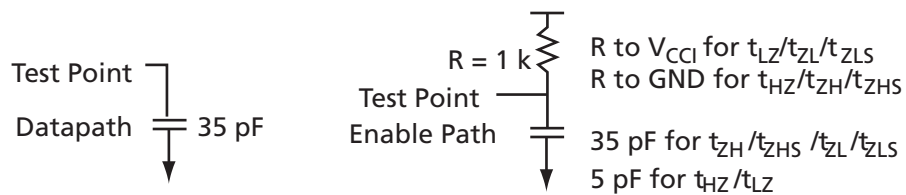


Figure 3-6 • AC Loading

Table 3-31 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C _{LOAD} (pF)
0	3.3	1.4	35

Note: *Measuring point = V_{trip}. See Table 3-17 on page 3-16 for a complete table of trip points.

Timing Characteristics

Table 3-32 • 3.3 V LVTTTL / 3.3 V LVCMOS Low Slew,
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst Case $V_{CC} = 1.425\text{ V}$, Worst Case $V_{CCI} = 3.0\text{ V}$
 Applicable to Advanced I/O Banks

Drive Strength (mA)	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	-F	0.79	12.32	0.05	1.22	0.51	12.55	10.69	3.18	2.95	15.23	13.37	ns
	Std.	0.66	10.26	0.04	1.02	0.43	10.45	8.90	2.64	2.46	12.68	11.13	ns
	-1	0.56	8.72	0.04	0.86	0.36	8.89	7.57	2.25	2.09	10.79	9.47	ns
	-2	0.49	7.66	0.03	0.76	0.32	7.80	6.64	1.98	1.83	9.47	8.31	ns
6 mA	-F	0.79	8.74	0.05	1.22	0.51	8.90	7.55	3.58	3.65	11.59	10.23	ns
	Std.	0.66	7.27	0.04	1.02	0.43	7.41	6.28	2.98	3.04	9.65	8.52	ns
	-1	0.56	6.19	0.04	0.86	0.36	6.30	5.35	2.54	2.59	8.20	7.25	ns
	-2	0.49	5.43	0.03	0.76	0.32	5.53	4.69	2.23	2.27	7.20	6.36	ns
8 mA	-F	0.79	8.74	0.05	1.22	0.51	8.90	7.55	3.58	3.65	11.59	10.23	ns
	Std.	0.66	7.27	0.04	1.02	0.43	7.41	6.28	2.98	3.04	9.65	8.52	ns
	-1	0.56	6.19	0.04	0.86	0.36	6.30	5.35	2.54	2.59	8.20	7.25	ns
	-2	0.49	5.43	0.03	0.76	0.32	5.53	4.69	2.23	2.27	7.20	6.36	ns
12 mA	-F	0.79	6.70	0.05	1.22	0.51	6.83	5.85	3.85	4.10	9.51	8.54	ns
	Std.	0.66	5.58	0.04	1.02	0.43	5.68	4.87	3.21	3.42	7.92	7.11	ns
	-1	0.56	4.75	0.04	0.86	0.36	4.84	4.14	2.73	2.91	6.74	6.05	ns
	-2	0.49	4.17	0.03	0.76	0.32	4.24	3.64	2.39	2.55	5.91	5.31	ns
16 mA	-F	0.79	6.25	0.05	1.22	0.51	6.37	5.48	3.91	4.22	9.06	8.17	ns
	Std.	0.66	5.21	0.04	1.02	0.43	5.30	4.56	3.26	3.51	7.54	6.80	ns
	-1	0.56	4.43	0.04	0.86	0.36	4.51	3.88	2.77	2.99	6.41	5.79	ns
	-2	0.49	3.89	0.03	0.76	0.32	3.96	3.41	2.43	2.62	5.63	5.08	ns
24 mA	-F	0.79	5.83	0.05	1.22	0.51	5.93	5.46	3.98	4.67	8.62	8.15	ns
	Std.	0.66	4.85	0.04	1.02	0.43	4.94	4.54	3.32	3.88	7.18	6.78	ns
	-1	0.56	4.13	0.04	0.86	0.36	4.20	3.87	2.82	3.30	6.10	5.77	ns
	-2	0.49	3.62	0.03	0.76	0.32	3.69	3.39	2.48	2.90	5.36	5.06	ns

Note: For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.

Table 3-33 • 3.3 V LVTTTL / 3.3 V LVCMOS High Slew,
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst Case $V_{CC} = 1.425\text{ V}$, Worst Case $V_{CCI} = 3.0\text{ V}$
 Applicable to Advanced I/O Banks

Drive Strength (mA)	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	-F	0.79	9.20	0.05	1.22	0.51	9.37	7.91	3.18	3.14	12.05	10.60	ns
	Std.	0.66	7.66	0.04	1.02	0.43	7.80	6.59	2.65	2.61	10.03	8.82	ns
	-1	0.56	6.51	0.04	0.86	0.36	6.63	5.60	2.25	2.22	8.54	7.51	ns
	-2	0.49	5.72	0.03	0.76	0.32	5.82	4.92	1.98	1.95	7.49	6.59	ns
6 mA	-F	0.79	5.89	0.05	1.22	0.51	6.00	4.89	3.59	3.85	8.69	7.57	ns
	Std.	0.66	4.91	0.04	1.02	0.43	5.00	4.07	2.99	3.20	7.23	6.31	ns
	-1	0.56	4.17	0.04	0.86	0.36	4.25	3.46	2.54	2.73	6.15	5.36	ns
	-2	0.49	3.66	0.03	0.76	0.32	3.73	3.04	2.23	2.39	5.40	4.71	ns
8 mA	-F	0.79	5.89	0.05	1.22	0.51	6.00	4.89	3.59	3.85	8.69	7.57	ns
	Std.	0.66	4.91	0.04	1.02	0.43	5.00	4.07	2.99	3.20	7.23	6.31	ns
	-1	0.56	4.17	0.04	0.86	0.36	4.25	3.46	2.54	2.73	6.15	5.36	ns
	-2	0.49	3.66	0.03	0.76	0.32	3.73	3.04	2.23	2.39	5.40	4.71	ns
12 mA	-F	0.79	4.24	0.05	1.22	0.51	4.32	3.39	3.86	4.30	7.01	6.08	ns
	Std.	0.66	3.53	0.04	1.02	0.43	3.60	2.82	3.21	3.58	5.83	5.06	ns
	-1	0.56	3.00	0.04	0.86	0.36	3.06	2.40	2.73	3.05	4.96	4.30	ns
	-2	0.49	2.64	0.03	0.76	0.32	2.69	2.11	2.40	2.68	4.36	3.78	ns
16 mA	-F	0.79	4.00	0.05	1.22	0.51	4.08	3.08	3.92	4.42	6.76	5.77	ns
	Std.	0.66	3.33	0.04	1.02	0.43	3.39	2.56	3.26	3.68	5.63	4.80	ns
	-1	0.56	2.83	0.04	0.86	0.36	2.89	2.18	2.77	3.13	4.79	4.08	ns
	-2	0.49	2.49	0.03	0.76	0.32	2.53	1.91	2.44	2.75	4.20	3.58	ns
24 mA	-F	0.79	3.69	0.05	1.22	0.51	3.76	2.54	3.99	4.88	6.45	5.23	ns
	Std.	0.66	3.08	0.04	1.02	0.43	3.13	2.12	3.32	4.06	5.37	4.35	ns
	-1	0.56	2.62	0.04	0.86	0.36	2.66	1.80	2.83	3.45	4.57	3.70	ns
	-2	0.49	2.30	0.03	0.76	0.32	2.34	1.58	2.48	3.03	4.01	3.25	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.

Table 3-34 • 3.3 V LVTTTL / 3.3 V LVCMOS Low Slew,
 Commercial-Case Conditions: $T_j = 70^\circ\text{C}$, Worst Case $V_{CC} = 1.425\text{ V}$, Worst Case $V_{CCI} = 3.0\text{ V}$
 Applicable to Standard+ I/O Banks

Drive Strength (mA)	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	-F	0.79	11.63	0.05	1.20	0.51	11.84	10.12	2.74	2.65	14.53	12.81	ns
	Std.	0.66	9.68	0.04	1.00	0.43	9.86	8.42	2.28	2.21	12.09	10.66	ns
	-1	0.56	8.23	0.04	0.85	0.36	8.39	7.17	1.94	1.88	10.29	9.07	ns
	-2	0.49	7.23	0.03	0.75	0.32	7.36	6.29	1.70	1.65	9.03	7.96	ns
6 mA	-F	0.79	8.05	0.05	1.20	0.51	8.20	7.07	3.10	3.29	10.88	9.76	ns
	Std.	0.66	6.70	0.04	1.00	0.43	6.82	5.89	2.58	2.74	9.06	8.12	ns
	-1	0.56	5.70	0.04	0.85	0.36	5.80	5.01	2.20	2.33	7.71	6.91	ns
	-2	0.49	5.00	0.03	0.75	0.32	5.10	4.40	1.93	2.05	6.76	6.06	ns
8 mA	-F	0.79	8.05	0.05	1.20	0.51	8.20	7.07	3.10	3.29	10.88	9.76	ns
	Std.	0.66	6.70	0.04	1.00	0.43	6.82	5.89	2.58	2.74	9.06	8.12	ns
	-1	0.56	5.70	0.04	0.85	0.36	5.80	5.01	2.20	2.33	7.71	6.91	ns
	-2	0.49	5.00	0.03	0.75	0.32	5.10	4.40	1.93	2.05	6.76	6.06	ns
12 mA	-F	0.79	6.06	0.05	1.20	0.51	6.18	5.42	3.35	3.70	8.86	8.10	ns
	Std.	0.66	5.05	0.04	1.00	0.43	5.14	4.51	2.79	3.08	7.38	6.75	ns
	-1	0.56	4.29	0.04	0.85	0.36	4.37	3.84	2.38	2.62	6.28	5.74	ns
	-2	0.49	3.77	0.03	0.75	0.32	3.84	3.37	2.09	2.30	5.51	5.04	ns
16 mA	-F	0.79	6.06	0.05	1.20	0.51	6.18	5.42	3.35	3.70	8.86	8.10	ns
	Std.	0.66	5.05	0.04	1.00	0.43	5.14	4.51	2.79	3.08	7.38	6.75	ns
	-1	0.56	4.29	0.04	0.85	0.36	4.37	3.84	2.38	2.62	6.28	5.74	ns
	-2	0.49	3.77	0.03	0.75	0.32	3.84	3.37	2.09	2.30	5.51	5.04	ns

Note: For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.

Table 3-35 • 3.3 V LVTTTL / 3.3 V LVCMOS High Slew,
Commercial-Case Conditions: $T_j = 70^\circ\text{C}$, Worst Case $V_{CC} = 1.425\text{ V}$, Worst Case $V_{CCI} = 3.0\text{ V}$
Applicable to Standard+ I/O Banks

Drive Strength (mA)	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	-F	0.79	8.65	0.05	1.20	0.51	8.81	7.55	2.73	2.81	11.50	10.24	ns
	Std.	0.66	7.20	0.04	1.00	0.43	7.34	6.29	2.27	2.34	9.57	8.52	ns
	-1	0.56	6.13	0.04	0.85	0.36	6.24	5.35	1.93	1.99	8.14	7.25	ns
	-2	0.49	5.38	0.03	0.75	0.32	5.48	4.69	1.70	1.75	7.15	6.36	ns
6 mA	-F	0.79	5.41	0.05	1.20	0.51	5.51	4.58	3.10	3.45	8.19	7.27	ns
	Std.	0.66	4.50	0.04	1.00	0.43	4.58	3.82	2.58	2.88	6.82	6.05	ns
	-1	0.56	3.83	0.04	0.85	0.36	3.90	3.25	2.19	2.45	5.80	5.15	ns
	-2	0.49	3.36	0.03	0.75	0.32	3.42	2.85	1.92	2.15	5.09	4.52	ns
8 mA	-F	0.79	5.41	0.05	1.20	0.51	5.51	4.58	3.10	3.45	8.19	7.27	ns
	Std.	0.66	4.50	0.04	1.00	0.43	4.58	3.82	2.58	2.88	6.82	6.05	ns
	-1	0.56	3.83	0.04	0.85	0.36	3.90	3.25	2.19	2.45	5.80	5.15	ns
	-2	0.49	3.36	0.03	0.75	0.32	3.42	2.85	1.92	2.15	5.09	4.52	ns
12 mA	-F	0.79	3.80	0.05	1.20	0.51	3.87	3.10	3.35	3.87	6.55	5.79	ns
	Std.	0.66	3.16	0.04	1.00	0.43	3.22	2.58	2.79	3.22	5.45	4.82	ns
	-1	0.56	2.69	0.04	0.85	0.36	2.74	2.20	2.37	2.74	4.64	4.10	ns
	-2	0.49	2.36	0.03	0.75	0.32	2.40	1.93	2.08	2.41	4.07	3.60	ns
16 mA	-F	0.79	3.80	0.05	1.20	0.51	3.87	3.10	3.35	3.87	6.55	5.79	ns
	Std.	0.66	3.16	0.04	1.00	0.43	3.22	2.58	2.79	3.22	5.45	4.82	ns
	-1	0.56	2.69	0.04	0.85	0.36	2.74	2.20	2.37	2.74	4.64	4.10	ns
	-2	0.49	2.36	0.03	0.75	0.32	2.40	1.93	2.08	2.41	4.07	3.60	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general purpose 2.5 V applications. It uses a 5-V-tolerant input buffer and push-pull output buffer.

Table 3-36 • Minimum and Maximum DC Input and Output Levels
Applicable to Advanced I/O Banks

2.5 V LVCMOS Drive Strength	V _{IL}		V _{IH}		V _{OL}	V _{OH}	I _{OL}	I _{OH}	I _{OSL}	I _{OSH}	I _{IL}	I _{IH}
	Min, V	Max, V	Min, V	Max, V	Max, V	Min, V	mA	mA	Max, mA ¹	Max, mA ¹	μA ²	μA ²
2 mA	-0.3	0.7	1.7	3.6	0.7	1.7	2	2	18	16	10	10
4 mA	-0.3	0.7	1.7	3.6	0.7	1.7	4	4	18	16	10	10
6 mA	-0.3	0.7	1.7	3.6	0.7	1.7	6	6	37	32	10	10
8 mA	-0.3	0.7	1.7	3.6	0.7	1.7	8	8	37	32	10	10
12 mA	-0.3	0.7	1.7	3.6	0.7	1.7	12	12	74	65	10	10
16 mA	-0.3	0.7	1.7	3.6	0.7	1.7	16	16	87	83	10	10
24 mA	-0.3	0.7	1.7	3.6	0.7	1.7	24	24	124	169	10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.
3. Software default selection highlighted in gray.

Table 3-37 • Minimum and Maximum DC Input and Output Levels
Applicable to Standard+ I/O Banks

2.5 V LVCMOS Drive Strength	V _{IL}		V _{IH}		V _{OL}	V _{OH}	I _{OL}	I _{OH}	I _{OSL}	I _{OSH}	I _{IL}	I _{IH}
	Min, V	Max, V	Min, V	Max, V	Max, V	Min, V	mA	mA	Max, mA ¹	Max, mA ¹	μA ²	μA ²
2 mA	-0.3	0.7	1.7	3.6	0.7	1.7	2	2	18	16	10	10
4 mA	-0.3	0.7	1.7	3.6	0.7	1.7	4	4	18	16	10	10
6 mA	-0.3	0.7	1.7	3.6	0.7	1.7	6	6	37	32	10	10
8 mA	-0.3	0.7	1.7	3.6	0.7	1.7	8	8	37	32	10	10
12 mA	-0.3	0.7	1.7	3.6	0.7	1.7	12	12	74	65	10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.
3. Software default selection highlighted in gray.

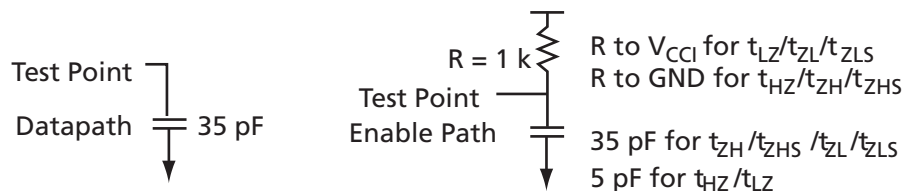


Figure 3-7 • AC Loading

Table 3-38 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C _{LOAD} (pF)
0	2.5	1.2	35

Note: *Measuring point = V_{trip} . See Table 3-17 on page 3-16 for a complete table of trip points.

Timing Characteristics

Table 3-39 • 2.5 V LVCMOS Low Slew,
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst Case $V_{CC} = 1.425\text{ V}$, Worst Case $V_{CCI} = 2.3\text{ V}$
 Applicable to Advanced I/O Banks

Drive Strength (mA)	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	–F	0.79	13.69	0.05	1.57	0.51	13.48	13.69	3.22	2.65	16.16	16.38	ns
	Std.	0.66	11.40	0.04	1.31	0.43	11.22	11.40	2.68	2.20	13.45	13.63	ns
	–1	0.56	9.69	0.04	1.11	0.36	9.54	9.69	2.28	1.88	11.44	11.60	ns
	–2	0.49	8.51	0.03	0.98	0.32	8.38	8.51	2.00	1.65	10.05	10.18	ns
6 mA	–F	0.79	9.56	0.05	1.57	0.51	9.74	9.39	3.66	3.47	12.43	12.07	ns
	Std.	0.66	7.96	0.04	1.31	0.43	8.11	7.81	3.05	2.89	10.34	10.05	ns
	–1	0.56	6.77	0.04	1.11	0.36	6.90	6.65	2.59	2.46	8.80	8.55	ns
	–2	0.49	5.94	0.03	0.98	0.32	6.05	5.84	2.28	2.16	7.72	7.50	ns
8 mA	–F	0.79	9.56	0.05	1.57	0.51	9.74	9.39	3.66	3.47	12.43	12.07	ns
	Std.	0.66	7.96	0.04	1.31	0.43	8.11	7.81	3.05	2.89	10.34	10.05	ns
	–1	0.56	6.77	0.04	1.11	0.36	6.90	6.65	2.59	2.46	8.80	8.55	ns
	–2	0.49	5.94	0.03	0.98	0.32	6.05	5.84	2.28	2.16	7.72	7.50	ns
12 mA	–F	0.79	7.42	0.05	1.57	0.51	7.56	7.11	3.97	3.99	10.25	9.80	ns
	Std.	0.66	6.18	0.04	1.31	0.43	6.29	5.92	3.30	3.32	8.53	8.15	ns
	–1	0.56	5.26	0.04	1.11	0.36	5.35	5.03	2.81	2.83	7.26	6.94	ns
	–2	0.49	4.61	0.03	0.98	0.32	4.70	4.42	2.47	2.48	6.37	6.09	ns
16 mA	–F	0.79	6.92	0.05	1.57	0.51	7.05	6.64	4.04	4.13	9.74	9.32	ns
	Std.	0.66	5.76	0.04	1.31	0.43	5.87	5.53	3.36	3.44	8.11	7.76	ns
	–1	0.56	4.90	0.04	1.11	0.36	4.99	4.70	2.86	2.92	6.90	6.60	ns
	–2	0.49	4.30	0.03	0.98	0.32	4.38	4.13	2.51	2.57	6.05	5.80	ns
24 mA	–F	0.79	6.61	0.05	1.57	0.51	6.61	6.61	4.13	4.65	9.30	9.30	ns
	Std.	0.66	5.51	0.04	1.31	0.43	5.50	5.51	3.43	3.87	7.74	7.74	ns
	–1	0.56	4.68	0.04	1.11	0.36	4.68	4.68	2.92	3.29	6.58	6.59	ns
	–2	0.49	4.11	0.03	0.98	0.32	4.11	4.11	2.56	2.89	5.78	5.78	ns

Note: For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.

Table 3-40 • 2.5 V LVCMOS High Slew,
Commercial-Case Conditions: $T_j = 70^\circ\text{C}$, Worst Case $V_{CC} = 1.425\text{ V}$, Worst Case $V_{CCI} = 2.3\text{ V}$
Applicable to Advanced I/O Banks

Drive Strength (mA)	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	-F	0.79	10.41	0.05	1.57	0.51	9.41	10.41	3.22	2.77	12.09	13.09	ns
	Std.	0.66	8.66	0.04	1.31	0.43	7.83	8.66	2.68	2.30	10.07	10.90	ns
	-1	0.56	7.37	0.04	1.11	0.36	6.66	7.37	2.28	1.96	8.56	9.27	ns
	-2	0.49	6.47	0.03	0.98	0.32	5.85	6.47	2.00	1.72	7.52	8.14	ns
6 mA	-F	0.79	6.21	0.05	1.57	0.51	6.05	6.21	3.66	3.60	8.74	8.89	ns
	Std.	0.66	5.17	0.04	1.31	0.43	5.04	5.17	3.05	3.00	7.27	7.40	ns
	-1	0.56	4.39	0.04	1.11	0.36	4.28	4.39	2.59	2.55	6.19	6.30	ns
	-2	0.49	3.86	0.03	0.98	0.32	3.76	3.86	2.28	2.24	5.43	5.53	ns
8 mA	-F	0.79	6.21	0.05	1.57	0.51	6.05	6.21	3.66	3.60	8.74	8.89	ns
	Std.	0.66	5.17	0.04	1.31	0.43	5.04	5.17	3.05	3.00	7.27	7.40	ns
	-1	0.56	4.39	0.04	1.11	0.36	4.28	4.39	2.59	2.55	6.19	6.30	ns
	-2	0.49	3.86	0.03	0.98	0.32	3.76	3.86	2.28	2.24	5.43	5.53	ns
12 mA	-F	0.79	4.28	0.05	1.57	0.51	4.36	4.12	3.97	4.13	7.04	6.81	ns
	Std.	0.66	3.56	0.04	1.31	0.43	3.63	3.43	3.30	3.44	5.86	5.67	ns
	-1	0.56	3.03	0.04	1.11	0.36	3.08	2.92	2.81	2.92	4.99	4.82	ns
	-2	0.49	2.66	0.03	0.98	0.32	2.71	2.56	2.47	2.57	4.38	4.23	ns
16 mA	-F	0.79	4.03	0.05	1.57	0.51	4.10	3.68	4.04	4.26	6.79	6.36	ns
	Std.	0.66	3.35	0.04	1.31	0.43	3.41	3.06	3.36	3.55	5.65	5.30	ns
	-1	0.56	2.85	0.04	1.11	0.36	2.90	2.60	2.86	3.02	4.81	4.51	ns
	-2	0.49	2.50	0.03	0.98	0.32	2.55	2.29	2.51	2.65	4.22	3.96	ns
24 mA	-F	0.79	3.71	0.05	1.57	0.51	3.78	2.93	4.13	4.80	6.47	5.62	ns
	Std.	0.66	3.09	0.04	1.31	0.43	3.15	2.44	3.44	4.00	5.38	4.68	ns
	-1	0.56	2.63	0.04	1.11	0.36	2.68	2.08	2.92	3.40	4.58	3.98	ns
	-2	0.49	2.31	0.03	0.98	0.32	2.35	1.82	2.57	2.98	4.02	3.49	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage-supply levels, refer to [Table 3-6 on page 3-4](#) for derating values.

Table 3-41 • 2.5 V LVCMOS Low Slew,
 Commercial-Case Conditions: $T_j = 70^\circ\text{C}$, Worst Case $V_{CC} = 1.425\text{ V}$, Worst Case $V_{CCI} = 2.3\text{ V}$
 Applicable to Standard+ I/O Banks

Drive Strength (mA)	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	-F	0.79	13.02	0.05	1.56	0.51	12.78	13.02	2.71	2.39	15.46	15.71	ns
	Std.	0.66	10.84	0.04	1.30	0.43	10.66	10.84	2.26	1.99	12.87	13.08	ns
	-1	0.56	9.22	0.04	1.10	0.36	9.05	9.22	1.92	1.69	10.95	11.12	ns
	-2	0.49	8.10	0.03	0.97	0.32	7.94	8.10	1.68	1.49	9.61	9.77	ns
6 mA	-F	0.79	8.85	0.05	1.56	0.51	9.01	8.84	3.11	3.14	11.70	11.53	ns
	Std.	0.66	7.37	0.04	1.30	0.43	7.50	7.36	2.59	2.61	9.74	9.60	ns
	-1	0.56	6.27	0.04	1.10	0.36	6.38	6.26	2.20	2.22	8.29	8.16	ns
	-2	0.49	5.50	0.03	0.97	0.32	5.60	5.50	1.93	1.95	7.27	7.17	ns
8 mA	-F	0.79	8.85	0.05	1.56	0.51	9.01	8.84	3.11	3.14	11.70	11.53	ns
	Std.	0.66	7.37	0.04	1.30	0.43	7.50	7.36	2.59	2.61	9.74	9.60	ns
	-1	0.56	6.27	0.04	1.10	0.36	6.38	6.26	2.20	2.22	8.29	8.16	ns
	-2	0.49	5.50	0.03	0.97	0.32	5.60	5.50	1.93	1.95	7.27	7.17	ns
12 mA	-F	0.79	6.76	0.05	1.56	0.51	6.89	6.61	3.40	3.62	9.57	9.30	ns
	Std.	0.66	5.63	0.04	1.30	0.43	5.73	5.51	2.83	3.01	7.97	7.74	ns
	-1	0.56	4.79	0.04	1.10	0.36	4.88	4.68	2.41	2.56	6.78	6.59	ns
	-2	0.49	4.20	0.03	0.97	0.32	4.28	4.11	2.11	2.25	5.95	5.78	ns

Note: For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.

Table 3-42 • 2.5 V LVCMOS High Slew,
 Commercial-Case Conditions: $T_j = 70^\circ\text{C}$, Worst Case $V_{CC} = 1.425\text{ V}$, Worst Case $V_{CCI} = 2.3\text{ V}$
 Applicable to Standard+ I/O Banks

Drive Strength (mA)	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	-F	0.79	9.94	0.05	1.56	0.51	8.90	9.94	2.70	2.49	11.58	12.63	ns
	Std.	0.66	8.28	0.04	1.30	0.43	7.41	8.28	2.25	2.07	9.64	10.51	ns
	-1	0.56	7.04	0.04	1.10	0.36	6.30	7.04	1.92	1.76	8.20	8.94	ns
	-2	0.49	6.18	0.03	0.97	0.32	5.53	6.18	1.68	1.55	7.20	7.85	ns
6 mA	-F	0.79	5.83	0.05	1.56	0.51	5.58	5.83	3.11	3.26	8.27	8.52	ns
	Std.	0.66	4.85	0.04	1.30	0.43	4.65	4.85	2.59	2.71	6.88	7.09	ns
	-1	0.56	4.13	0.04	1.10	0.36	3.95	4.13	2.20	2.31	5.85	6.03	ns
	-2	0.49	3.62	0.03	0.97	0.32	3.47	3.62	1.93	2.02	5.14	5.29	ns
8 mA	-F	0.79	5.83	0.05	1.56	0.51	5.58	5.83	3.11	3.26	8.27	8.52	ns
	Std.	0.66	4.85	0.04	1.30	0.43	4.65	4.85	2.59	2.71	6.88	7.09	ns
	-1	0.56	4.13	0.04	1.10	0.36	3.95	4.13	2.20	2.31	5.85	6.03	ns
	-2	0.49	3.62	0.03	0.97	0.32	3.47	3.62	1.93	2.02	5.14	5.29	ns
12 mA	-F	0.79	3.85	0.05	1.56	0.51	3.92	3.77	3.39	3.74	6.61	6.46	ns
	Std.	0.66	3.21	0.04	1.30	0.43	3.27	3.14	2.82	3.11	5.50	5.38	ns
	-1	0.56	2.73	0.04	1.10	0.36	2.78	2.67	2.40	2.65	4.68	4.57	ns
	-2	0.49	2.39	0.03	0.97	0.32	2.44	2.35	2.11	2.32	4.11	4.02	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.

1.8 V LVCMOS

Low-voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general purpose 1.8 V applications. It uses 1.8 V input buffer and push-pull output buffer.

Table 3-43 • Minimum and Maximum DC Input and Output Levels
Applicable to Advanced I/O Banks

1.8 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
	Min, V	Max, V	Min, V	Max, V	Max, V	Min, V	mA	mA	Max, mA ¹	Max, mA ¹	μA^2	μA^2
2 mA	-0.3	$0.35 * V_{CCI}$	$0.65 * V_{CCI}$	3.6	0.45	$V_{CCI} - 0.45$	2	2	11	9	10	10
4 mA	-0.3	$0.35 * V_{CCI}$	$0.65 * V_{CCI}$	3.6	0.45	$V_{CCI} - 0.45$	4	4	22	17	10	10
6 mA	-0.3	$0.35 * V_{CCI}$	$0.65 * V_{CCI}$	3.6	0.45	$V_{CCI} - 0.45$	6	6	44	35	10	10
8 mA	-0.3	$0.35 * V_{CCI}$	$0.65 * V_{CCI}$	3.6	0.45	$V_{CCI} - 0.45$	8	8	51	45	10	10
12 mA	-0.3	$0.35 * V_{CCI}$	$0.65 * V_{CCI}$	3.6	0.45	$V_{CCI} - 0.45$	12	12	74	91	10	10
16 mA	-0.3	$0.35 * V_{CCI}$	$0.65 * V_{CCI}$	3.6	0.45	$V_{CCI} - 0.45$	16	16	74	91	10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.
3. Software default selection highlighted in gray.

Table 3-44 • Minimum and Maximum DC Input and Output Levels
Applicable to Standard+ I/O Banks

1.8 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
	Min, V	Max, V	Min, V	Max, V	Max, V	Min, V	mA	mA	Max, mA ¹	Max, mA ¹	μA^2	μA^2
2 mA	-0.3	$0.35 * V_{CCI}$	$0.65 * V_{CCI}$	3.6	0.45	$V_{CCI} - 0.45$	2	2	11	9	10	10
4 mA	-0.3	$0.35 * V_{CCI}$	$0.65 * V_{CCI}$	3.6	0.45	$V_{CCI} - 0.45$	4	4	22	17	10	10
6 mA	-0.3	$0.35 * V_{CCI}$	$0.65 * V_{CCI}$	3.6	0.45	$V_{CCI} - 0.45$	6	6	44	35	10	10
8 mA	-0.3	$0.35 * V_{CCI}$	$0.65 * V_{CCI}$	3.6	0.45	$V_{CCI} - 0.45$	8	8	44	35	10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.
3. Software default selection highlighted in gray.

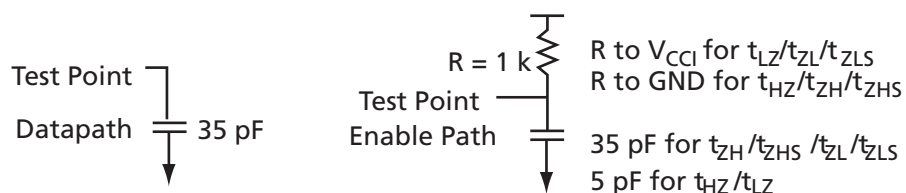


Figure 3-8 • AC Loading

Table 3-45 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C _{LOAD} (pF)
0	1.8	0.9	35

Note: *Measuring point = V_{trip} . See Table 3-17 on page 3-16 for a complete table of trip points.

Timing Characteristics

Table 3-46 • 1.8 V LVCMOS Low Slew,
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst Case $V_{CC} = 1.425\text{ V}$, Worst Case $V_{CCI} = 1.7\text{ V}$
Applicable to Advanced I/O Banks

Drive Strength (mA)	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PV}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
2 mA	–F	0.79	18.66	0.05	1.46	0.51	16.95	18.66	3.34	1.92	19.64	21.34	ns
	Std.	0.66	15.53	0.04	1.22	0.43	14.11	15.53	2.78	1.60	16.35	17.77	ns
	–1	0.56	13.21	0.04	1.04	0.36	12.01	13.21	2.36	1.36	13.91	15.11	ns
	–2	0.49	11.60	0.03	0.91	0.32	10.54	11.60	2.07	1.19	12.21	13.27	ns
4 mA	–F	0.79	12.58	0.05	1.46	0.51	12.51	12.58	3.88	3.28	15.19	15.27	ns
	Std.	0.66	10.48	0.04	1.22	0.43	10.41	10.48	3.23	2.73	12.65	12.71	ns
	–1	0.56	8.91	0.04	1.04	0.36	8.86	8.91	2.75	2.33	10.76	10.81	ns
	–2	0.49	7.82	0.03	0.91	0.32	7.77	7.82	2.41	2.04	9.44	9.49	ns
6 mA	–F	0.79	9.67	0.05	1.46	0.51	9.85	9.42	4.25	3.93	12.53	12.11	ns
	Std.	0.66	8.05	0.04	1.22	0.43	8.20	7.84	3.54	3.27	10.43	10.08	ns
	–1	0.56	6.85	0.04	1.04	0.36	6.97	6.67	3.01	2.78	8.88	8.57	ns
	–2	0.49	6.01	0.03	0.91	0.32	6.12	5.86	2.64	2.44	7.79	7.53	ns
8 mA	–F	0.79	9.01	0.05	1.46	0.51	9.18	8.77	4.33	4.10	11.87	11.45	ns
	Std.	0.66	7.50	0.04	1.22	0.43	7.64	7.30	3.61	3.41	9.88	9.53	ns
	–1	0.56	6.38	0.04	1.04	0.36	6.50	6.21	3.07	2.90	8.40	8.11	ns
	–2	0.49	5.60	0.03	0.91	0.32	5.71	5.45	2.69	2.55	7.38	7.12	ns
12 mA	–F	0.79	8.76	0.05	1.46	0.51	8.69	8.76	4.45	4.74	11.38	11.45	ns
	Std.	0.66	7.29	0.04	1.22	0.43	7.23	7.29	3.71	3.95	9.47	9.53	ns
	–1	0.56	6.20	0.04	1.04	0.36	6.15	6.20	3.15	3.36	8.06	8.11	ns
	–2	0.49	5.45	0.03	0.91	0.32	5.40	5.45	2.77	2.95	7.07	7.12	ns
16 mA	–F	0.79	8.76	0.05	1.46	0.51	8.69	8.76	4.45	4.74	11.38	11.45	ns
	Std.	0.66	7.29	0.04	1.22	0.43	7.23	7.29	3.71	3.95	9.47	9.53	ns
	–1	0.56	6.20	0.04	1.04	0.36	6.15	6.20	3.15	3.36	8.06	8.11	ns
	–2	0.49	5.45	0.03	0.91	0.32	5.40	5.45	2.77	2.95	7.07	7.12	ns

Note: For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.

Table 3-47 • 1.8 V LVCMOS High Slew,
 Commercial-Case Conditions: $T_j = 70^\circ\text{C}$, Worst Case $V_{CC} = 1.425\text{ V}$, Worst Case $V_{CCI} = 1.7\text{ V}$
 Applicable to Advanced I/O Banks

Drive Strength (mA)	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	-F	0.79	14.25	0.05	1.46	0.51	10.97	14.25	3.33	1.99	13.66	16.94	ns
	Std.	0.66	11.86	0.04	1.22	0.43	9.14	11.86	2.77	1.66	11.37	14.10	ns
	-1	0.56	10.09	0.04	1.04	0.36	7.77	10.09	2.36	1.41	9.67	11.99	ns
	-2	0.49	8.86	0.03	0.91	0.32	6.82	8.86	2.07	1.24	8.49	10.53	ns
4 mA	-F	0.79	8.31	0.05	1.46	0.51	7.04	8.31	3.87	3.41	9.73	10.99	ns
	Std.	0.66	6.91	0.04	1.22	0.43	5.86	6.91	3.22	2.84	8.10	9.15	ns
	-1	0.56	5.88	0.04	1.04	0.36	4.99	5.88	2.74	2.41	6.89	7.78	ns
	-2	0.49	5.16	0.03	0.91	0.32	4.38	5.16	2.41	2.12	6.05	6.83	ns
6 mA	-F	0.79	5.34	0.05	1.46	0.51	5.02	5.34	4.24	4.06	7.71	8.03	ns
	Std.	0.66	4.45	0.04	1.22	0.43	4.18	4.45	3.53	3.38	6.42	6.68	ns
	-1	0.56	3.78	0.04	1.04	0.36	3.56	3.78	3.00	2.88	5.46	5.69	ns
	-2	0.49	3.32	0.03	0.91	0.32	3.12	3.32	2.64	2.53	4.79	4.99	ns
8 mA	-F	0.79	4.71	0.05	1.46	0.51	4.72	4.71	4.32	4.23	7.40	7.40	ns
	Std.	0.66	3.92	0.04	1.22	0.43	3.93	3.92	3.60	3.52	6.16	6.16	ns
	-1	0.56	3.34	0.04	1.04	0.36	3.34	3.34	3.06	3.00	5.24	5.24	ns
	-2	0.49	2.93	0.03	0.91	0.32	2.93	2.93	2.69	2.63	4.60	4.60	ns
12 mA	-F	0.79	4.24	0.05	1.46	0.51	4.32	3.65	4.45	4.90	7.01	6.34	ns
	Std.	0.66	3.53	0.04	1.22	0.43	3.60	3.04	3.70	4.08	5.84	5.28	ns
	-1	0.56	3.01	0.04	1.04	0.36	3.06	2.59	3.15	3.47	4.96	4.49	ns
	-2	0.49	2.64	0.03	0.91	0.32	2.69	2.27	2.76	3.05	4.36	3.94	ns
16 mA	-F	0.79	4.24	0.05	1.46	0.51	4.32	3.65	4.45	4.90	7.01	6.34	ns
	Std.	0.66	3.53	0.04	1.22	0.43	3.60	3.04	3.70	4.08	5.84	5.28	ns
	-1	0.56	3.01	0.04	1.04	0.36	3.06	2.59	3.15	3.47	4.96	4.49	ns
	-2	0.49	2.64	0.03	0.91	0.32	2.69	2.27	2.76	3.05	4.36	3.94	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.

Table 3-48 • 1.8 V LVCMOS Low Slew,
 Commercial-Case Conditions: $T_j = 70^\circ\text{C}$, Worst Case $V_{CC} = 1.425\text{ V}$, Worst Case $V_{CCI} = 1.7\text{ V}$
 Applicable to Standard+ I/O Banks

Drive Strength (mA)	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	-F	0.79	17.78	0.05	1.44	0.51	16.21	17.78	2.70	1.76	18.90	20.47	ns
	Std.	0.66	14.80	0.04	1.20	0.43	13.49	14.80	2.25	1.46	15.73	17.04	ns
	-1	0.56	12.59	0.04	1.02	0.36	11.48	12.59	1.91	1.25	13.38	14.49	ns
	-2	0.49	11.05	0.03	0.90	0.32	10.08	11.05	1.68	1.09	11.75	12.72	ns
4 mA	-F	0.79	11.89	0.05	1.44	0.51	11.69	11.89	3.19	3.00	14.38	14.58	ns
	Std.	0.66	9.90	0.04	1.20	0.43	9.73	9.90	2.65	2.50	11.97	12.13	ns
	-1	0.56	8.42	0.04	1.02	0.36	8.28	8.42	2.26	2.12	10.18	10.32	ns
	-2	0.49	7.39	0.03	0.90	0.32	7.27	7.39	1.98	1.86	8.94	9.06	ns
6 mA	-F	0.79	8.93	0.05	1.44	0.51	9.10	8.79	3.53	3.59	11.79	11.48	ns
	Std.	0.66	7.44	0.04	1.20	0.43	7.58	7.32	2.94	2.99	9.81	9.56	ns
	-1	0.56	6.33	0.04	1.02	0.36	6.44	6.23	2.50	2.54	8.35	8.13	ns
	-2	0.49	5.55	0.03	0.90	0.32	5.66	5.47	2.19	2.23	7.33	7.14	ns
8 mA	-F	0.79	8.93	0.05	1.44	0.51	9.10	8.79	3.53	3.59	11.79	11.48	ns
	Std.	0.66	7.44	0.04	1.20	0.43	7.58	7.32	2.94	2.99	9.81	9.56	ns
	-1	0.56	6.33	0.04	1.02	0.36	6.44	6.23	2.50	2.54	8.35	8.13	ns
	-2	0.49	5.55	0.03	0.90	0.32	5.66	5.47	2.19	2.23	7.33	7.14	ns

Note: For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.

Table 3-49 • 1.8 V LVCMOS High Slew,
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst Case $V_{CC} = 1.425\text{ V}$, Worst Case $V_{CCI} = 1.7\text{ V}$
Applicable to Standard+ I/O Banks

Drive Strength (mA)	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	-F	0.79	13.61	0.05	1.44	0.51	10.48	13.61	2.70	1.83	13.17	16.30	ns
	Std.	0.66	11.33	0.04	1.20	0.43	8.72	11.33	2.24	1.52	10.96	13.57	ns
	-1	0.56	9.64	0.04	1.02	0.36	7.42	9.64	1.91	1.29	9.32	11.54	ns
	-2	0.49	8.46	0.03	0.90	0.32	6.51	8.46	1.68	1.14	8.18	10.13	ns
4 mA	-F	0.79	7.79	0.05	1.44	0.51	6.58	7.79	3.18	3.13	9.27	10.47	ns
	Std.	0.66	6.48	0.04	1.20	0.43	5.48	6.48	2.65	2.60	7.72	8.72	ns
	-1	0.56	5.51	0.04	1.02	0.36	4.66	5.51	2.25	2.21	6.56	7.42	ns
	-2	0.49	4.84	0.03	0.90	0.32	4.09	4.84	1.98	1.94	5.76	6.51	ns
6 mA	-F	0.79	4.88	0.05	1.44	0.51	4.61	4.88	3.52	3.73	7.30	7.56	ns
	Std.	0.66	4.06	0.04	1.20	0.43	3.84	4.06	2.93	3.10	6.07	6.30	ns
	-1	0.56	3.45	0.04	1.02	0.36	3.27	3.45	2.49	2.64	5.17	5.36	ns
	-2	0.49	3.03	0.03	0.90	0.32	2.87	3.03	2.19	2.32	4.54	4.70	ns
8 mA	-F	0.79	4.88	0.05	1.44	0.51	4.61	4.88	3.52	3.73	7.30	7.56	ns
	Std.	0.66	4.06	0.04	1.20	0.43	3.84	4.06	2.93	3.10	6.07	6.30	ns
	-1	0.56	3.45	0.04	1.02	0.36	3.27	3.45	2.49	2.64	5.17	5.36	ns
	-2	0.49	3.03	0.03	0.90	0.32	2.87	3.03	2.19	2.32	4.54	4.70	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.

1.5 V LVCMOS (JESD8-11)

Low-voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general purpose 1.5 V applications. It uses 1.5 V input buffer and push-pull output buffer.

Table 3-50 • Minimum and Maximum DC Input and Output Levels
Applicable to Advanced I/O Banks

1.5 V LVCMOS	V _{IL}		V _{IH}		V _{OL}	V _{OH}	I _{OL}	I _{OH}	I _{OSL}	I _{OSH}	I _{IL}	I _{IH}
	Min, V	Max, V	Min, V	Max, V	Max, V	Min, V	mA	mA	Max, mA ¹	Max, mA ¹	μA ²	μA ²
2 mA	-0.3	0.30 * V _{CCI}	0.7 * V _{CCI}	3.6	0.25 * V _{CCI}	0.75 * V _{CCI}	2	2	16	13	10	10
4 mA	-0.3	0.30 * V _{CCI}	0.7 * V _{CCI}	3.6	0.25 * V _{CCI}	0.75 * V _{CCI}	4	4	33	25	10	10
6 mA	-0.3	0.30 * V _{CCI}	0.7 * V _{CCI}	3.6	0.25 * V _{CCI}	0.75 * V _{CCI}	6	6	39	32	10	10
8 mA	-0.3	0.30 * V _{CCI}	0.7 * V _{CCI}	3.6	0.25 * V _{CCI}	0.75 * V _{CCI}	8	8	55	66	10	10
12 mA	-0.3	0.30 * V _{CCI}	0.7 * V _{CCI}	3.6	0.25 * V _{CCI}	0.75 * V _{CCI}	12	12	55	66	10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.
3. Software default selection highlighted in gray.

Table 3-51 • Minimum and Maximum DC Input and Output Levels
Applicable to Standard+ I/O Banks

1.5 V LVCMOS	V _{IL}		V _{IH}		V _{OL}	V _{OH}	I _{OL}	I _{OH}	I _{OSL}	I _{OSH}	I _{IL}	I _{IH}
	Min, V	Max, V	Min, V	Max, V	Max, V	Min, V	mA	mA	Max, mA ¹	Max, mA ¹	μA ²	μA ²
2 mA	-0.3	0.30 * V _{CCI}	0.7 * V _{CCI}	3.6	0.25 * V _{CCI}	0.75 * V _{CCI}	2	2	0	0	10	10
4 mA	-0.3	0.30 * V _{CCI}	0.7 * V _{CCI}	3.6	0.25 * V _{CCI}	0.75 * V _{CCI}	4	4	0	0	10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.
3. Software default selection highlighted in gray.

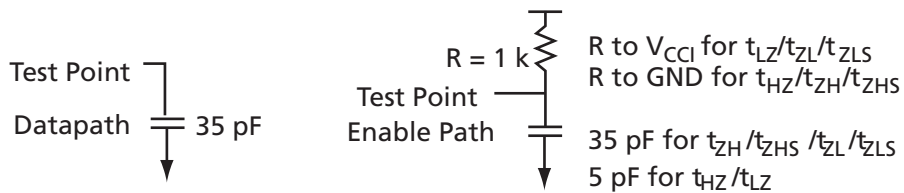


Figure 3-9 • AC Loading

Table 3-52 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C _{LOAD} (pF)
0	1.5	0.75	35

Note: *Measuring point = V_{trip}. See Table 3-17 on page 3-16 for a complete table of trip points.

Timing Characteristics

Table 3-53 • 1.5 V LVCMOS Low Slew,
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst Case $V_{CC} = 1.425\text{ V}$, Worst Case $V_{CCI} = 1.4\text{ V}$
Applicable to Advanced I/O Banks

Drive Strength (mA)	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PV}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	–F	0.79	15.36	0.05	1.73	0.51	15.39	15.36	4.08	3.18	18.07	18.04	ns
	Std.	0.66	12.78	0.04	1.44	0.43	12.81	12.78	3.40	2.64	15.05	15.02	ns
	–1	0.56	10.87	0.04	1.22	0.36	10.90	10.87	2.89	2.25	12.80	12.78	ns
	–2	0.49	9.55	0.03	1.07	0.32	9.57	9.55	2.54	1.97	11.24	11.22	ns
4 mA	–F	0.79	12.02	0.05	1.73	0.51	12.25	11.47	4.50	3.93	14.93	14.15	ns
	Std.	0.66	10.01	0.04	1.44	0.43	10.19	9.55	3.75	3.27	12.43	11.78	ns
	–1	0.56	8.51	0.04	1.22	0.36	8.67	8.12	3.19	2.78	10.57	10.02	ns
	–2	0.49	7.47	0.03	1.07	0.32	7.61	7.13	2.80	2.44	9.28	8.80	ns
6 mA	–F	0.79	11.21	0.05	1.73	0.51	11.42	10.68	4.60	4.12	14.11	13.37	ns
	Std.	0.66	9.33	0.04	1.44	0.43	9.51	8.89	3.83	3.43	11.74	11.13	ns
	–1	0.56	7.94	0.04	1.22	0.36	8.09	7.56	3.26	2.92	9.99	9.47	ns
	–2	0.49	6.97	0.03	1.07	0.32	7.10	6.64	2.86	2.56	8.77	8.31	ns
8 mA	–F	0.79	10.70	0.05	1.73	0.51	10.90	10.68	4.75	4.86	13.59	13.37	ns
	Std.	0.66	8.91	0.04	1.44	0.43	9.07	8.89	3.95	4.05	11.31	11.13	ns
	–1	0.56	7.58	0.04	1.22	0.36	7.72	7.57	3.36	3.44	9.62	9.47	ns
	–2	0.49	6.65	0.03	1.07	0.32	6.78	6.64	2.95	3.02	8.45	8.31	ns
12 mA	–F	0.79	10.70	0.05	1.73	0.51	10.90	10.68	4.75	4.86	13.59	13.37	ns
	Std.	0.66	8.91	0.04	1.44	0.43	9.07	8.89	3.95	4.05	11.31	11.13	ns
	–1	0.56	7.58	0.04	1.22	0.36	7.72	7.57	3.36	3.44	9.62	9.47	ns
	–2	0.49	6.65	0.03	1.07	0.32	6.78	6.64	2.95	3.02	8.45	8.31	ns

Note: For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.

Table 3-54 • 1.5 V LVCMOS High Slew,
 Commercial-Case Conditions: $T_j = 70^\circ\text{C}$, Worst Case $V_{CC} = 1.425\text{ V}$, Worst Case $V_{CCI} = 1.4\text{ V}$
 Applicable to Advanced I/O Banks

Drive Strength (mA)	Speed Grade	tDOU T	tDP	tDIN	tPY	tEOU T	tZL	tZH	tLZ	tHZ	tZLS	tZHS	Units
2 mA	-F	0.79	10.05	0.05	1.73	0.51	8.20	10.05	4.07	3.32	10.88	12.73	ns
	Std.	0.66	8.36	0.04	1.44	0.43	6.82	8.36	3.39	2.77	9.06	10.60	ns
	-1	0.56	7.11	0.04	1.22	0.36	5.80	7.11	2.88	2.35	7.71	9.02	ns
	-2	0.49	6.24	0.03	1.07	0.32	5.10	6.24	2.53	2.06	6.76	7.91	ns
4 mA	-F	0.79	6.38	0.05	1.73	0.51	5.83	6.38	4.49	4.09	8.51	9.07	ns
	Std.	0.66	5.31	0.04	1.44	0.43	4.85	5.31	3.74	3.40	7.09	7.55	ns
	-1	0.56	4.52	0.04	1.22	0.36	4.13	4.52	3.18	2.89	6.03	6.42	ns
	-2	0.49	3.97	0.03	1.07	0.32	3.62	3.97	2.79	2.54	5.29	5.64	ns
6 mA	-F	0.79	5.61	0.05	1.73	0.51	5.46	5.61	4.59	4.28	8.15	8.29	ns
	Std.	0.66	4.67	0.04	1.44	0.43	4.55	4.67	3.82	3.56	6.78	6.90	ns
	-1	0.56	3.97	0.04	1.22	0.36	3.87	3.97	3.25	3.03	5.77	5.87	ns
	-2	0.49	3.49	0.03	1.07	0.32	3.40	3.49	2.85	2.66	5.07	5.16	ns
8 mA	-F	0.79	4.90	0.05	1.73	0.51	4.99	4.30	4.74	5.05	7.68	6.98	ns
	Std.	0.66	4.08	0.04	1.44	0.43	4.15	3.58	3.94	4.20	6.39	5.81	ns
	-1	0.56	3.47	0.04	1.22	0.36	3.53	3.04	3.36	3.58	5.44	4.95	ns
	-2	0.49	3.05	0.03	1.07	0.32	3.10	2.67	2.95	3.14	4.77	4.34	ns
12 mA	-F	0.79	4.90	0.05	1.73	0.51	4.99	4.30	4.74	5.05	7.68	6.98	ns
	Std.	0.66	4.08	0.04	1.44	0.43	4.15	3.58	3.94	4.20	6.39	5.81	ns
	-1	0.56	3.47	0.04	1.22	0.36	3.53	3.04	3.36	3.58	5.44	4.95	ns
	-2	0.49	3.05	0.03	1.07	0.32	3.10	2.67	2.95	3.14	4.77	4.34	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.

Table 3-55 • 1.5 V LVCMOS Low Slew,
Commercial-Case Conditions: $T_j = 70^\circ\text{C}$, Worst Case $V_{CC} = 1.425\text{ V}$, Worst Case $V_{CCI} = 1.4\text{ V}$
Applicable to Standard+ I/O Banks

Drive Strength (mA)	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	–F	0.79	14.51	0.05	1.71	0.51	14.42	14.51	3.26	2.91	17.11	17.20	ns
	Std.	0.66	12.08	0.04	1.42	0.43	12.01	12.08	2.72	2.43	14.24	14.31	ns
	–1	0.56	10.27	0.04	1.21	0.36	10.21	10.27	2.31	2.06	12.12	12.18	ns
	–2	0.49	9.02	0.03	1.06	0.32	8.97	9.02	2.03	1.81	10.64	10.69	ns
4 mA	–F	0.79	11.15	0.05	1.71	0.51	11.35	10.71	3.65	3.60	14.04	13.40	ns
	Std.	0.66	9.28	0.04	1.42	0.43	9.45	8.91	3.04	3.00	11.69	11.15	ns
	–1	0.56	7.89	0.04	1.21	0.36	8.04	7.58	2.58	2.55	9.94	9.49	ns
	–2	0.49	6.93	0.03	1.06	0.32	7.06	6.66	2.27	2.24	8.73	8.33	ns

Note: For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.

Table 3-56 • 1.5 V LVCMOS High Slew,
Commercial-Case Conditions: $T_j = 70^\circ\text{C}$, Worst Case $V_{CC} = 1.425\text{ V}$, Worst Case $V_{CCI} = 1.4\text{ V}$
Applicable to Standard+ I/O Banks

Drive Strength (mA)	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	–F	0.79	9.41	0.05	1.71	0.51	7.71	9.41	3.25	3.06	10.40	12.09	ns
	Std.	0.66	7.83	0.04	1.42	0.43	6.42	7.83	2.71	2.55	8.65	10.07	ns
	–1	0.56	6.66	0.04	1.21	0.36	5.46	6.66	2.31	2.17	7.36	8.56	ns
	–2	0.49	5.85	0.03	1.06	0.32	4.79	5.85	2.02	1.90	6.46	7.52	ns
4 mA	–F	0.79	5.81	0.05	1.71	0.51	5.39	5.81	3.64	3.76	8.08	8.50	ns
	Std.	0.66	4.84	0.04	1.42	0.43	4.49	4.84	3.03	3.13	6.72	7.08	ns
	–1	0.56	4.12	0.04	1.21	0.36	3.82	4.12	2.58	2.66	5.72	6.02	ns
	–2	0.49	3.61	0.03	1.06	0.32	3.35	3.61	2.26	2.34	5.02	5.28	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.

3.3 V PCI, 3.3 V PCI-X

Peripheral Component Interface for 3.3 V standard specifies support for 33 MHz and 66 MHz PCI Bus applications.

Table 3-57 • Minimum and Maximum DC Input and Output Levels

3.3 V PCI/PCI-X Drive Strength	V _{IL}		V _{IH}		V _{OL}	V _{OH}	I _{OL}	I _{OH}	I _{osL}	I _{osH}	I _{IL}	I _{IH}
	Min, V	Max, V	Min, V	Max, V	Max, V	Min, V	mA	mA	Max, mA ¹	Max, mA ¹	μA ²	μA ²
Per PCI specification	Per PCI curves										10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.

AC loadings are defined per the PCI/PCI-X specifications for the datapath; Actel loadings for enable path characterization are described in Figure 3-10.

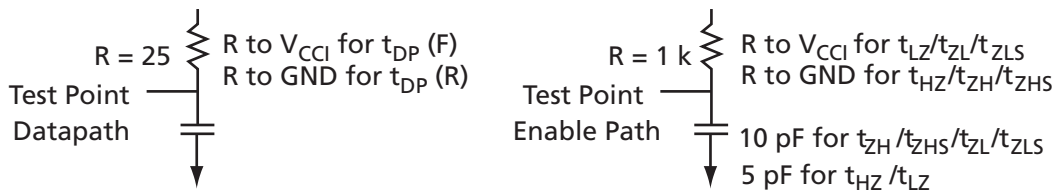


Figure 3-10 • AC Loading

AC loading are defined per PCI/PCI-X specifications for the datapath; Actel loading for tristate is described in Table 3-58.

Table 3-58 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C _{LOAD} (pF)
0	3.3	0.285 * V _{CC1} for t _{DP(R)} 0.615 * V _{CC1} for t _{DP(F)}	10

Note: *Measuring point = V_{trip}. See Table 3-17 on page 3-16 for a complete table of trip points.

Timing Characteristics

Table 3-59 • 3.3 V PCI/PCI-X, Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CC1} = 3.0 V
Applicable to Advanced I/O Banks

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
-F	0.79	3.22	0.05	1.04	0.51	3.28	2.34	3.86	4.30	5.97	5.03	ns
Std.	0.66	2.68	0.04	0.86	0.43	2.73	1.95	3.21	3.58	4.97	4.19	ns
-1	0.56	2.28	0.04	0.73	0.36	2.32	1.66	2.73	3.05	4.22	3.56	ns
-2	0.49	2.00	0.03	0.65	0.32	2.04	1.46	2.40	2.68	3.71	3.13	ns

Note: For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.

Table 3-60 • 3.3 V PCI/PCI-X,
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CC1} = 3.0 V
Applicable to Standard+ I/O Banks

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
-F	0.79	2.77	0.05	1.02	0.51	2.82	2.05	3.35	3.87	5.51	4.73	ns
Std.	0.66	2.31	0.04	0.85	0.43	2.35	1.70	2.79	3.22	4.59	3.94	ns
-1	0.56	1.96	0.04	0.72	0.36	2.00	1.45	2.37	2.74	3.90	3.35	ns
-2	0.49	1.72	0.03	0.64	0.32	1.76	1.27	2.08	2.41	3.42	2.94	ns

Note: For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.

Differential I/O Characteristics

Physical Implementation

Configuration of the I/O modules as a differential pair is handled by Actel Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and Double Data Rate (DDR). However, there is no support for bidirectional I/Os or tristates with the LVPECL standards.

LVDS

Low-Voltage Differential Signal (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard. It requires that one

data bit is carried through two signal lines, so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in [Figure 3-11](#). The building blocks of the LVDS transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation, because the output standard specifications are different.

Along with the LVDS IO, ProASIC3 also will support BusLVDS structure and Multi-Drop LVDS (M-LVDS) configuration (up to 40 nodes).

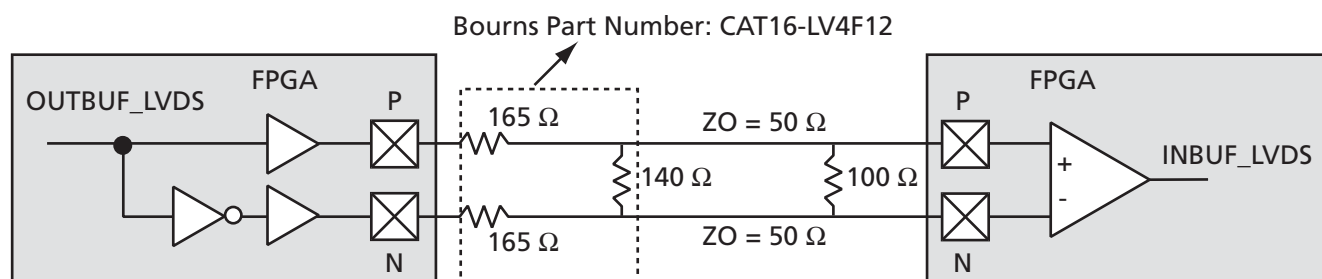


Figure 3-11 • LVDS Circuit Diagram and Board-Level Implementation

Table 3-61 • Minimum and Maximum DC Input and Output Levels

DC Parameter	Description	Min.	Typ.	Max.	Units
V_{CCI}	Supply Voltage	2.375	2.5	2.625	V
V_{OL}	Output Low Voltage	0.9	1.075	1.25	V
V_{OH}	Output High Voltage	1.25	1.425	1.6	V
V_I	Input Voltage	0	–	2.925	V
V_{ODIFF}	Differential Output Voltage	250	350	450	mV
V_{OCM}	Output Common Mode Voltage	1.125	1.25	1.375	V
V_{ICM}	Input Common Mode Voltage	0.05	1.25	2.35	V
V_{IDIFF}	Input Differential Voltage	100	350	–	mV

Notes:

1. $\pm 5\%$
2. Differential input voltage = ± 350 mV.

Table 3-62 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)
1.075	1.325	Cross point

Note: *Measuring point = V_{trip} . See [Table 3-6](#) on [page 3-4](#) for a complete table of trip points.

Timing Characteristics

Table 3-63 • LVDS

Commercial-Case Conditions: $T_j = 70^\circ\text{C}$, Worst Case $V_{CC} = 1.425\text{ V}$, Worst Case $V_{CCI} = 2.3\text{ V}$

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
-F	0.79	2.20	0.05	1.92	ns
Std.	0.66	1.83	0.04	1.60	ns
-1	0.56	1.56	0.04	1.36	ns
-2	0.49	1.37	0.03	1.20	ns

Note: For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.

BLVDS/M-LVDS

Bus LVDS (BLVDS) and Multipoint LVDS (M-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers and transceivers. Actel LVDS drivers provide the higher drive current required by BLVDS and M-LVDS to accommodate the loading. The driver requires series terminations for better signal quality and to control voltage swing. Termination is also required at both ends of the bus since the driver can be located anywhere on the bus. These configurations can be implemented using TRIBUF_LVDS and BIBUF_LVDS macros

along with appropriate terminations. Multipoint designs using Actel LVDS macros can achieve upto 200 MHz with a maximum of 20 loads. A sample application is given in Figure 3-12. The input and output buffer delays are available in the LVDS section in Table 3-63.

Example: For a bus consisting of 20 equidistant loads, the following terminations provide the required differential voltage, in worst case Industrial operating conditions, at the farthest receiver: $R_S = 60\ \Omega$ and $R_T = 70\ \Omega$, given $Z_0 = 50\ \Omega$ (2") and a $Z_{stub} = 50\ \Omega$ (~1.5").

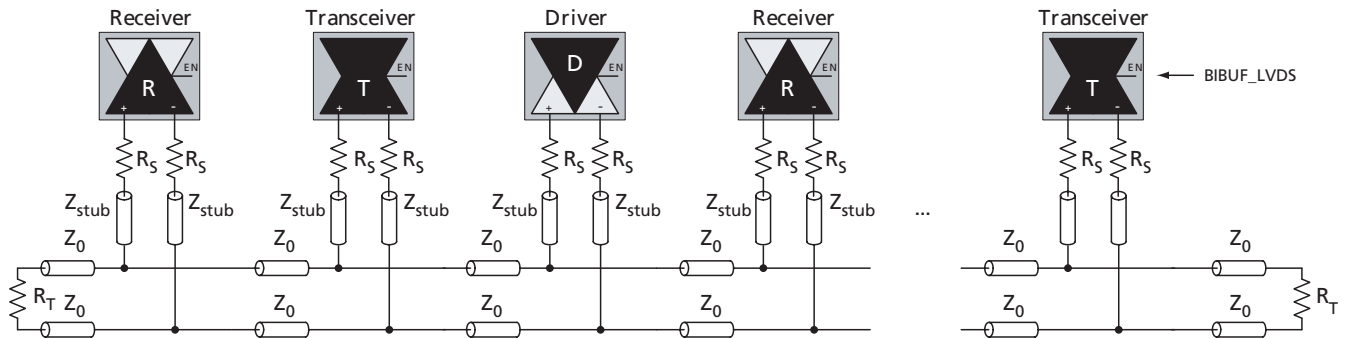


Figure 3-12 • BLVDS/M-LVDS Multipoint Application Using LVDS I/O Buffers

LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit is carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in [Figure 3-13](#). The building blocks of the LVPECL transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVDS implementation, because the output standard specifications are different.

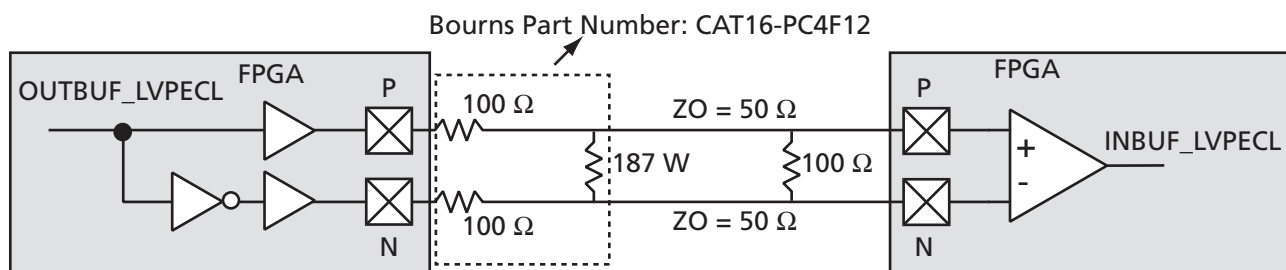


Figure 3-13 • LVPECL Circuit Diagram and Board-Level Implementation

Table 3-64 • Minimum and Maximum DC Input and Output Levels

DC Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
V_{CCI}	Supply Voltage	3.0		3.3		3.6		V
V_{OL}	Output Low Voltage	0.96	1.27	1.06	1.43	1.30	1.57	V
V_{OH}	Output High Voltage	1.8	2.11	1.92	2.28	2.13	2.41	V
V_{IL}, V_{IH}	Input Low, Input High voltages	0	3.3	0	3.6	0	3.9	V
V_{ODIFF}	Differential Output Voltage	0.625	0.97	0.625	0.97	0.625	0.97	V
V_{OCM}	Output Common Mode Voltage	1.762	1.98	1.762	1.98	1.762	1.98	V
V_{ICM}	Input Common Mode Voltage	1.01	2.57	1.01	2.57	1.01	2.57	V
V_{IDIFF}	Input Differential Voltage	300		300		300		mV

Table 3-65 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)
1.64	1.94	Cross point

Note: *Measuring point = V_{trip} . See [Table 3-17](#) on [page 3-16](#) for a complete table of trip points.

Timing Characteristics

Table 3-66 • LVPECL

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst Case $V_{CC} = 1.425\text{ V}$, Worst Case $V_{CCI} = 3.0\text{ V}$

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
-F	0.79	2.16	0.05	1.69	ns
Std.	0.66	1.80	0.04	1.40	ns
-1	0.56	1.53	0.04	1.19	ns
-2	0.49	1.34	0.03	1.05	ns

Note: For specific junction temperature and voltage-supply levels, refer to [Table 3-6](#) on [page 3-4](#) for derating values.

I/O Register Specifications

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

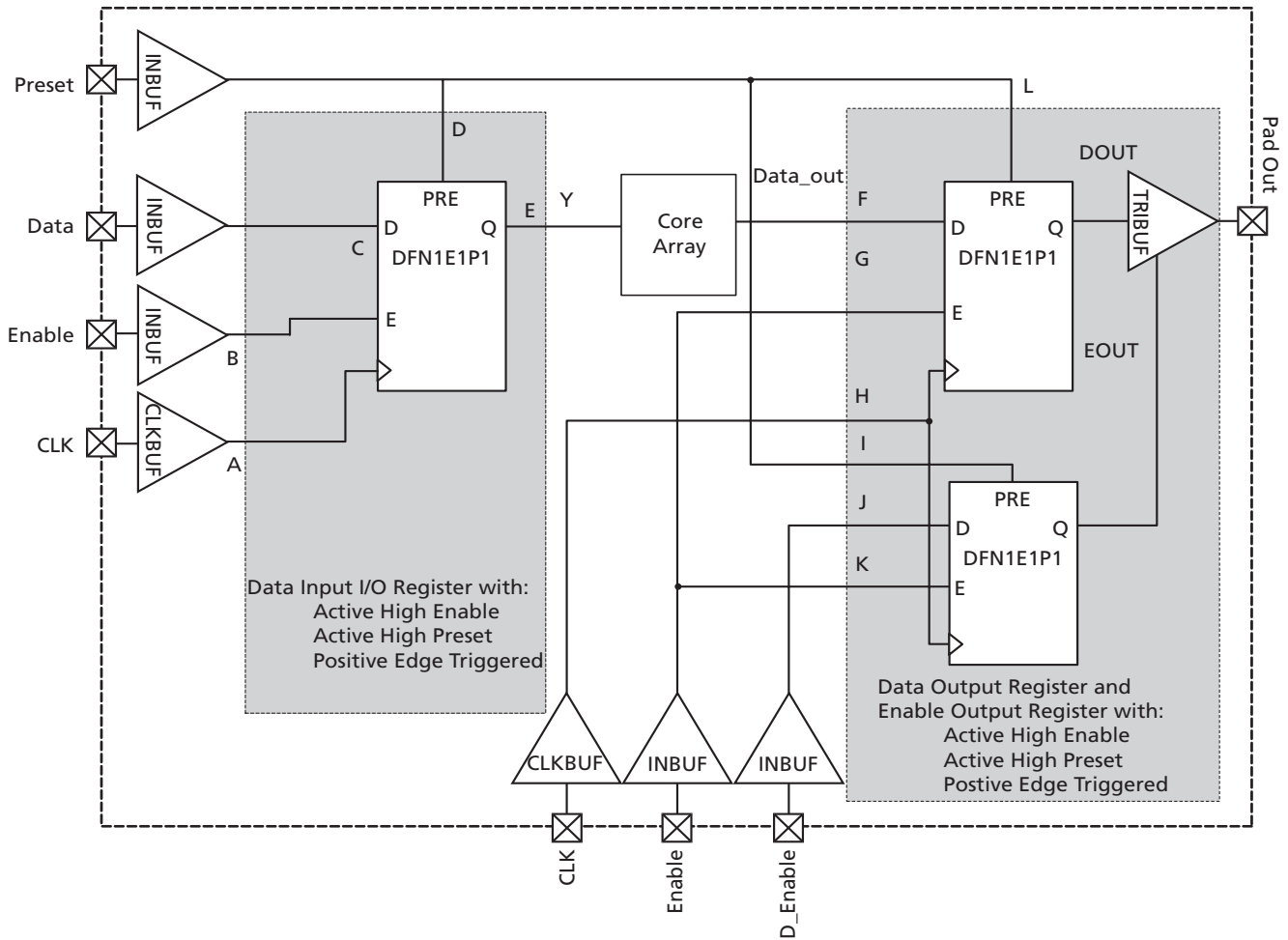


Figure 3-14 • Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

Table 3-67 • Parameter Definition and Measuring Nodes

Parameter Name	Parameter Definition	Measuring Nodes (From, To)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	H, DOUT
t_{OSUD}	Data Setup time for the Output Data Register	F, H
t_{OHD}	Data Hold time for the Output Data Register	F, H
t_{OSUE}	Enable Setup time for the Output Data Register	G, H
t_{OHE}	Enable Hold time for the Output Data Register	G, H
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L, DOUT
$t_{OREMPRE}$	Asynchronous Preset removal time for the Output Data Register	L, H
$t_{ORECPRE}$	Asynchronous Preset Recovery time for the Output Data Register	L, H
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
t_{OESUD}	Data Setup time for the Output Enable Register	J, H
t_{OEHd}	Data Hold time for the Output Enable Register	J, H
t_{OESUE}	Enable Setup time for the Output Enable Register	K, H
t_{OEHE}	Enable Hold time for the Output Enable Register	K, H
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
$t_{OEREMPRE}$	Asynchronous Preset Removal time for the Output Enable Register	I, H
$t_{OERECPRE}$	Asynchronous Preset Recovery time for the Output Enable Register	I, H
t_{ICLKQ}	Clock-to-Q of the Input Data Register	A, E
t_{ISUD}	Data Setup time for the Input Data Register	C, A
t_{IHd}	Data Hold time for the Input Data Register	C, A
t_{ISUE}	Enable Setup time for the Input Data Register	B, A
t_{IHE}	Enable Hold time for the Input Data Register	B, A
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
$t_{IREMPRE}$	Asynchronous Preset Removal time for the Input Data Register	D, A
$t_{IRECPRE}$	Asynchronous Preset Recovery time for the Input Data Register	D, A

Note: *See Figure 3-14 on page 3-46 for more information.

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

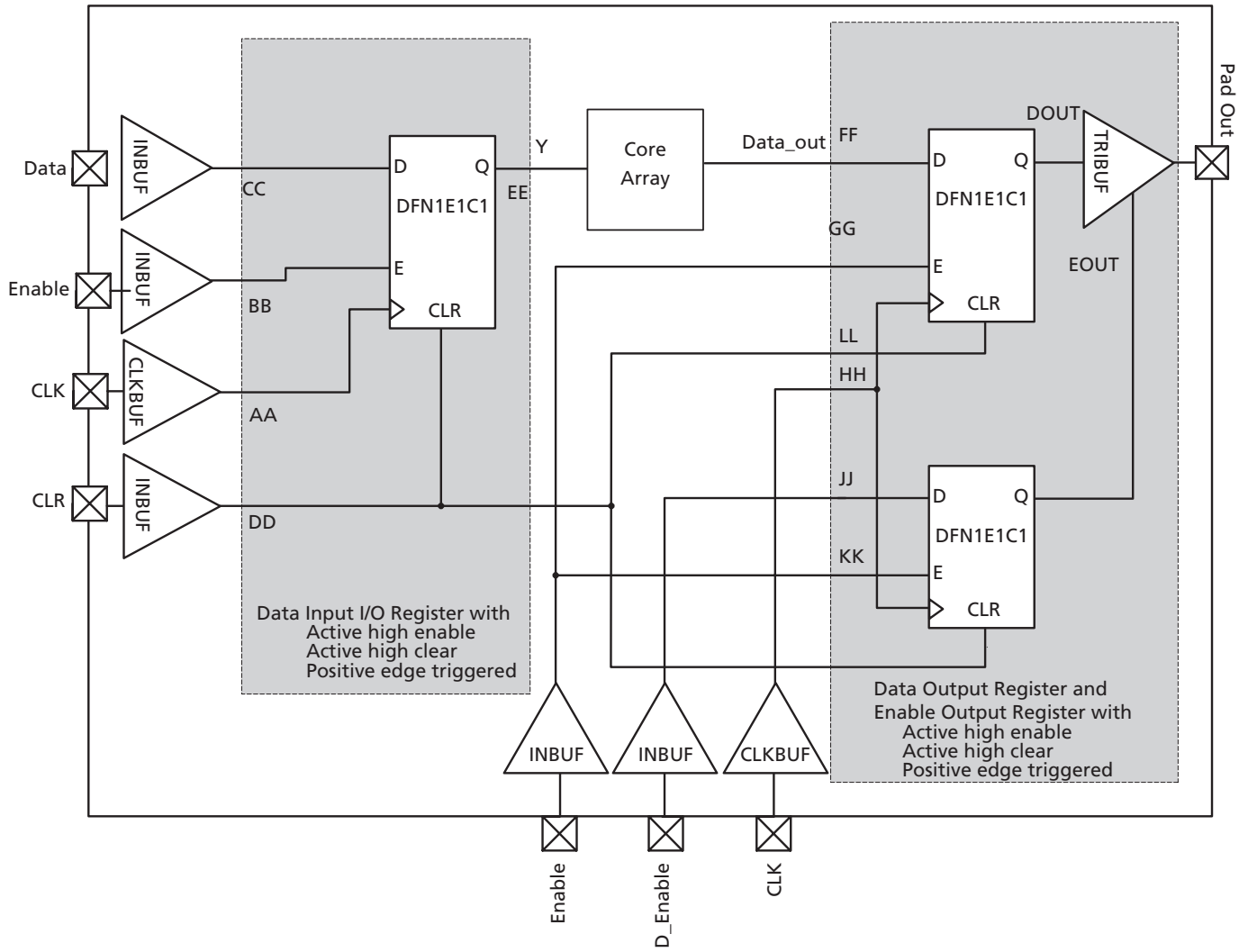


Figure 3-15 • Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

Table 3-68 • Parameter Definition and Measuring Nodes

Parameter Name	Parameter Definition	Measuring Nodes (From, To)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	HH, DOUT
t_{OSUD}	Data Setup time for the Output Data Register	FF, HH
t_{OHD}	Data Hold time for the Output Data Register	FF, HH
t_{OSUE}	Enable Setup time for the Output Data Register	GG, HH
t_{OHE}	Enable Hold time for the Output Data Register	GG, HH
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	LL, DOUT
$t_{OREMCLR}$	Asynchronous Clear Removal time for the Output Data Register	LL, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery time for the Output Data Register	LL, HH
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	HH, EOUT
t_{OESUD}	Data Setup time for the Output Enable Register	JJ, HH
t_{OEHD}	Data Hold time for the Output Enable Register	JJ, HH
t_{OESUE}	Enable Setup time for the Output Enable Register	KK, HH
t_{OEHE}	Enable Hold time for the Output Enable Register	KK, HH
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	II, EOUT
$t_{OEREMCLR}$	Asynchronous Clear Removal time for the Output Enable Register	II, HH
$t_{OERECCLR}$	Asynchronous Clear Recovery time for the Output Enable Register	II, HH
t_{ICLKQ}	Clock-to-Q of the Input Data Register	AA, EE
t_{ISUD}	Data Setup time for the Input Data Register	CC, AA
t_{IHD}	Data Hold time for the Input Data Register	CC, AA
t_{ISUE}	Enable Setup time for the Input Data Register	BB, AA
t_{IHE}	Enable Hold time for the Input Data Register	BB, AA
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	DD, EE
$t_{IREMCLR}$	Asynchronous Clear Removal time for the Input Data Register	DD, AA
$t_{IRECCLR}$	Asynchronous Clear Recovery time for the Input Data Register	DD, AA

Note: *See Figure 3-15 on page 3-48 for more information.

Input Register

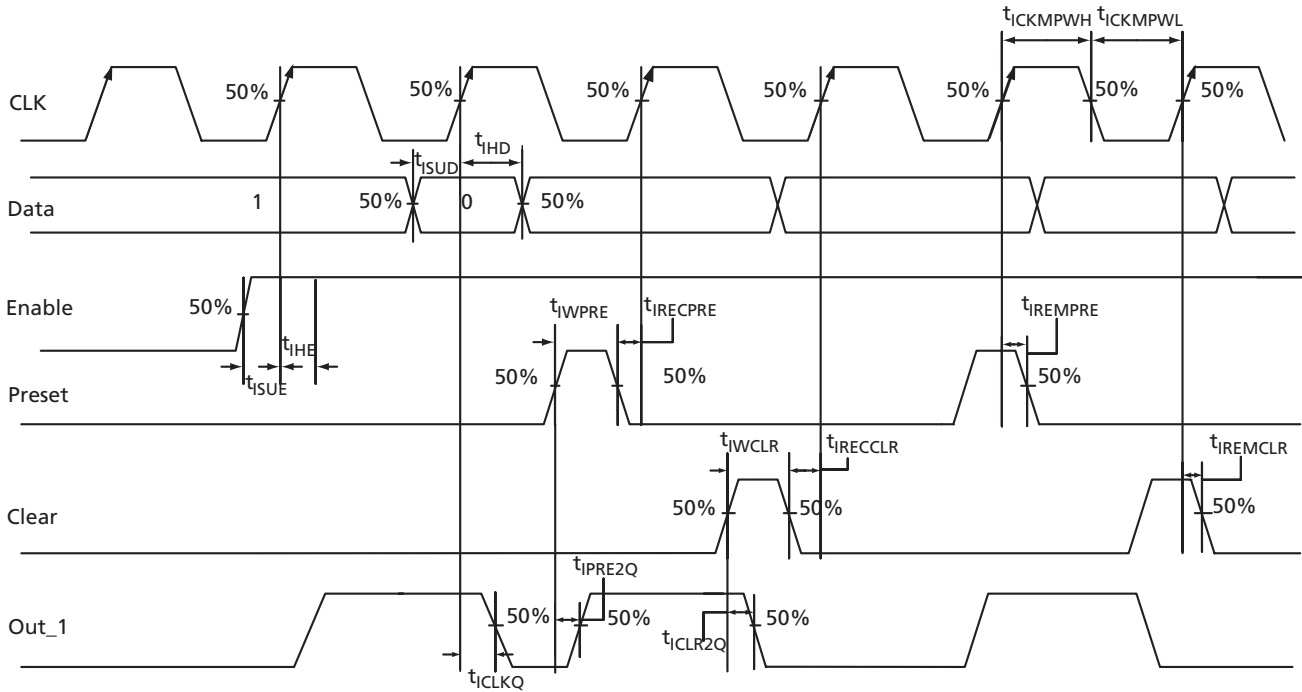


Figure 3-16 • Input Register Timing Diagram

Timing Characteristics

Table 3-69 • Input Data Register Propagation Delays
Commercial-Case Conditions: $T_j = 70^\circ\text{C}$, Worst Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	-2	-1	Std.	-F	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.63	0.71	0.84	1.01	ns
t_{ISUD}	Data Setup time for the Input Data Register	0.43	0.49	0.57	0.69	ns
t_{IHD}	Data Hold time for the Input Data Register	0.00	0.00	0.00	0.00	ns
t_{ISUE}	Enable Setup time for the Input Data Register	0.43	0.49	0.57	0.69	ns
t_{IHE}	Enable Hold time for the Input Data Register	0.00	0.00	0.00	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.63	0.71	0.84	1.01	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.45	0.51	0.60	0.72	ns
t_{IEMCLR}	Asynchronous Clear Removal time for the Input Data Register	0.00	0.00	0.00	0.00	ns
t_{IRECLR}	Asynchronous Clear Recovery time for the Input Data Register	0.22	0.25	0.30	0.36	ns
$t_{IREMPRE}$	Asynchronous Preset Removal time for the Input Data Register	0.00	0.00	0.00	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery time for the Input Data Register	0.22	0.25	0.30	0.36	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.25	0.28	0.33	0.40	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.25	0.28	0.33	0.40	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width High for the Input Data Register	0.36	0.41	0.48	0.58	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width Low for the Input Data Register	0.41	0.46	0.54	0.65	ns

Note: For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.

Output Register

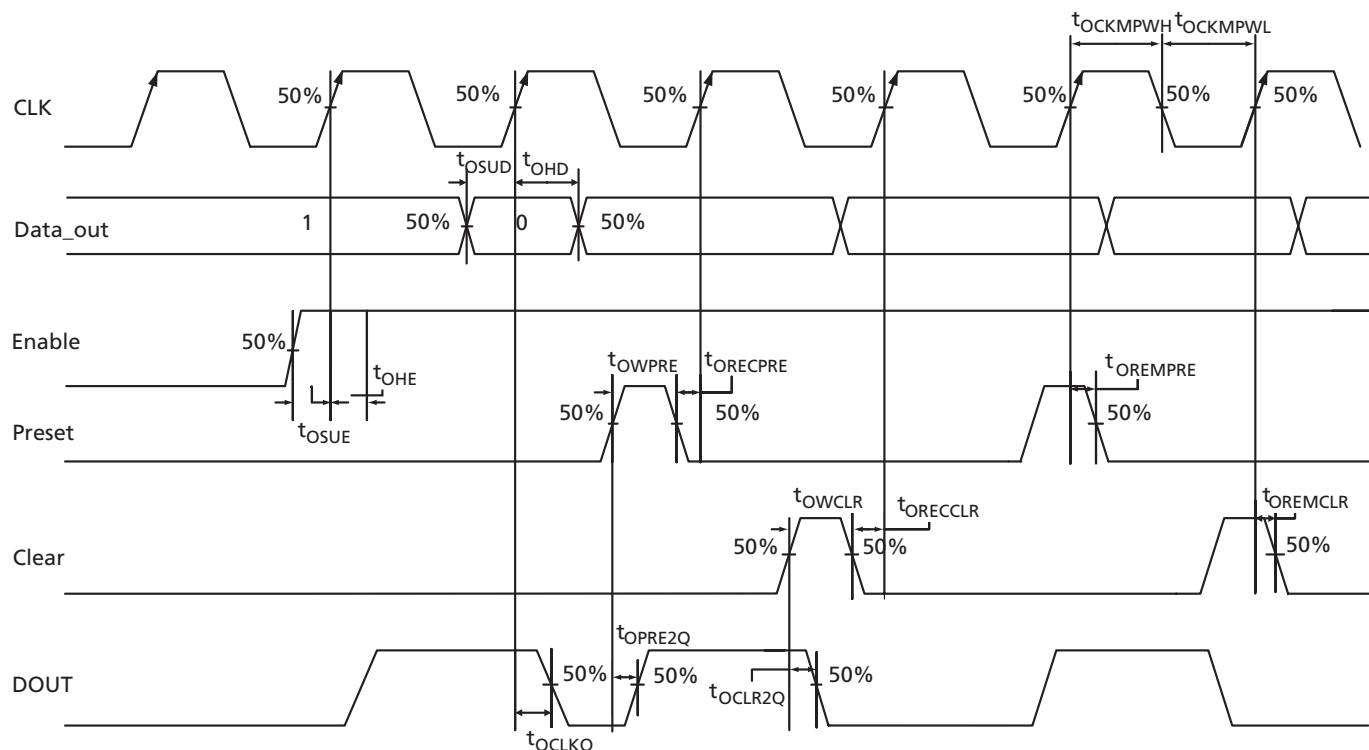


Figure 3-17 • Output Register Timing Diagram

Timing Characteristics

Table 3-70 • Output Data Register Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V

Parameter	Description	-2	-1	Std.	-F	Units
t _{OCLKQ}	Clock-to-Q of the Output Data Register	0.63	0.71	0.84	1.01	ns
t _{OSUD}	Data Setup time for the Output Data Register	0.43	0.49	0.57	0.69	ns
t _{OHD}	Data Hold time for the Output Data Register	0.00	0.00	0.00	0.00	ns
t _{OSUE}	Enable Setup time for the Output Data Register	0.43	0.49	0.57	0.69	ns
t _{OHE}	Enable Hold time for the Output Data Register	0.00	0.00	0.00	0.00	ns
t _{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	0.63	0.71	0.84	1.01	ns
t _{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	0.45	0.51	0.60	0.72	ns
t _{OREMCLR}	Asynchronous Clear Removal time for the Output Data Register	0.00	0.00	0.00	0.00	ns
t _{ORECCLR}	Asynchronous Clear Recovery time for the Output Data Register	0.22	0.25	0.30	0.36	ns
t _{OREMPRE}	Asynchronous Preset Removal time for the Output Data Register	0.00	0.00	0.00	0.00	ns
t _{ORECPRE}	Asynchronous Preset Recovery time for the Output Data Register	0.22	0.25	0.30	0.36	ns
t _{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.25	0.28	0.33	0.40	ns
t _{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.25	0.28	0.33	0.40	ns
t _{OCKMPWH}	Clock Minimum Pulse Width High for the Output Data Register	0.36	0.41	0.48	0.58	ns
t _{OCKMPWL}	Clock Minimum Pulse Width Low for the Output Data Register	0.41	0.46	0.54	0.65	ns

Note: For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.

Output Enable Register

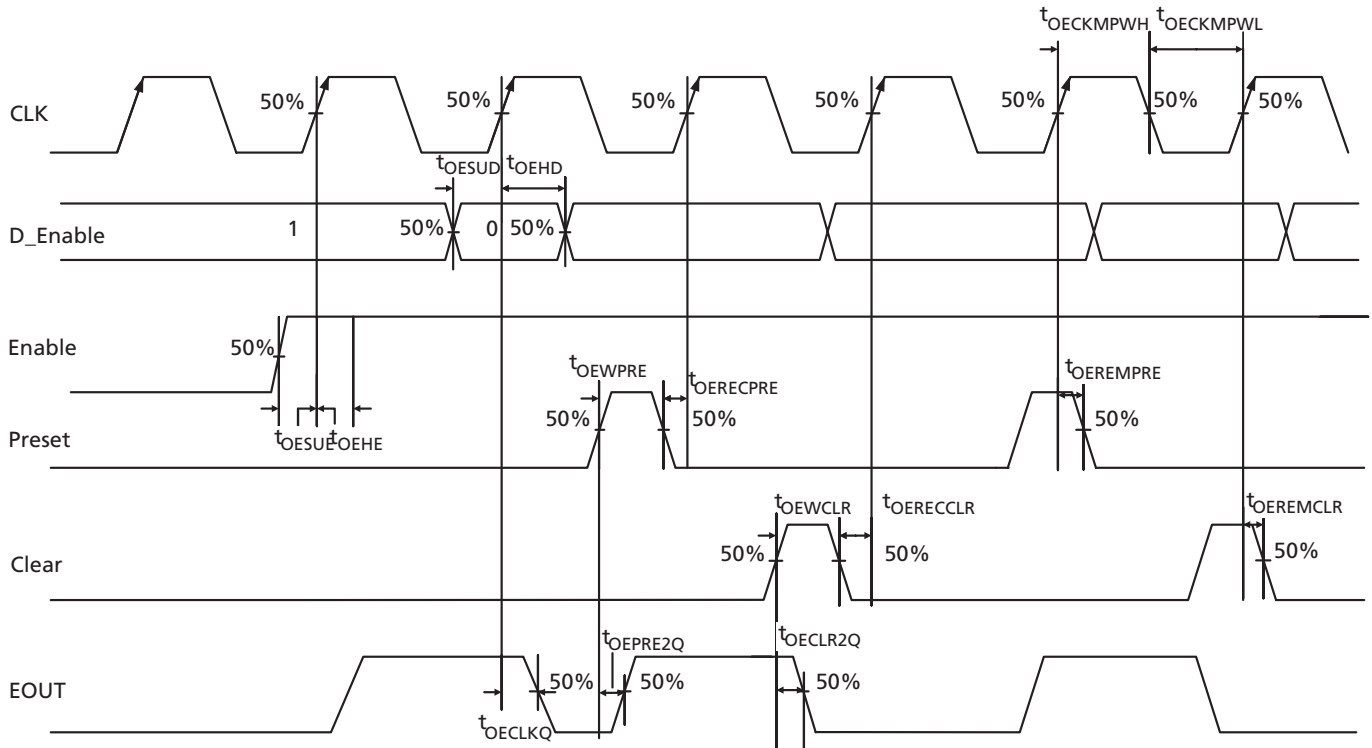


Figure 3-18 • Output Enable Register Timing Diagram

Timing Characteristics

Table 3-71 • Output Enable Register Propagation Delays
Commercial-Case Conditions: $T_j = 70^\circ\text{C}$, Worst Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	-2	-1	Std.	-F	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	0.63	0.71	0.84	1.01	ns
t_{OESUD}	Data Setup time for the Output Enable Register	0.43	0.49	0.57	0.69	ns
t_{OEHD}	Data Hold time for the Output Enable Register	0.00	0.00	0.00	0.00	ns
t_{OESUE}	Enable Setup time for the Output Enable Register	0.43	0.49	0.57	0.69	ns
t_{OEHE}	Enable Hold time for the Output Enable Register	0.00	0.00	0.00	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	0.63	0.71	0.84	1.01	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	0.45	0.51	0.60	0.72	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal time for the Output Enable Register	0.00	0.00	0.00	0.00	ns
$t_{OERECCLR}$	Asynchronous Clear Recovery time for the Output Enable Register	0.22	0.25	0.30	0.36	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal time for the Output Enable Register	0.00	0.00	0.00	0.00	ns
$t_{OERECPRE}$	Asynchronous Preset Recovery time for the Output Enable Register	0.22	0.25	0.30	0.36	ns
$t_{OEWCCLR}$	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.25	0.28	0.33	0.40	ns
t_{OEWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.25	0.28	0.33	0.40	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width High for the Output Enable Register	0.36	0.41	0.48	0.58	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width Low for the Output Enable Register	0.41	0.46	0.54	0.65	ns

Note: For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.

DDR Module Specifications

Input DDR Module

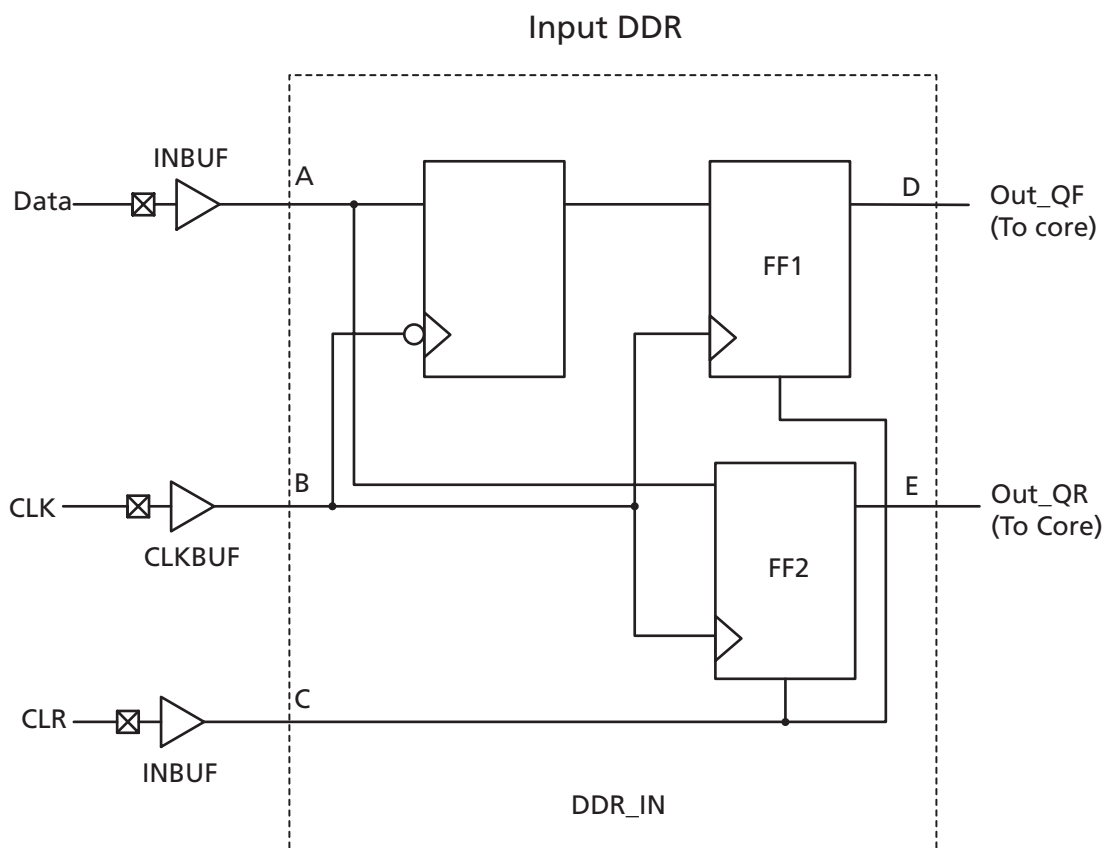


Figure 3-19 • Input DDR Timing Model

Table 3-72 • Parameter Definitions

Parameter Name	Parameter Definition	Measuring Nodes (From, To)
t_{DDRICKQ1}	Clock-to-Out Out_QR	B, D
t_{DDRICKQ2}	Clock-to-Out Out_QF	B, E
t_{DDRISUD}	Data Setup time of DDR input	A, B
t_{DDRIHD}	Data Hold time of DDR input	A, B
$t_{\text{DDRICLR2Q1}}$	Clear-to-Out Out_QR	C, D
$t_{\text{DDRICLR2Q2}}$	Clear-to-Out Out_QF	C, E
$t_{\text{DDRIREMCLR}}$	Clear Removal	C, B
$t_{\text{DDRIRECCLR}}$	Clear Recovery	C, B

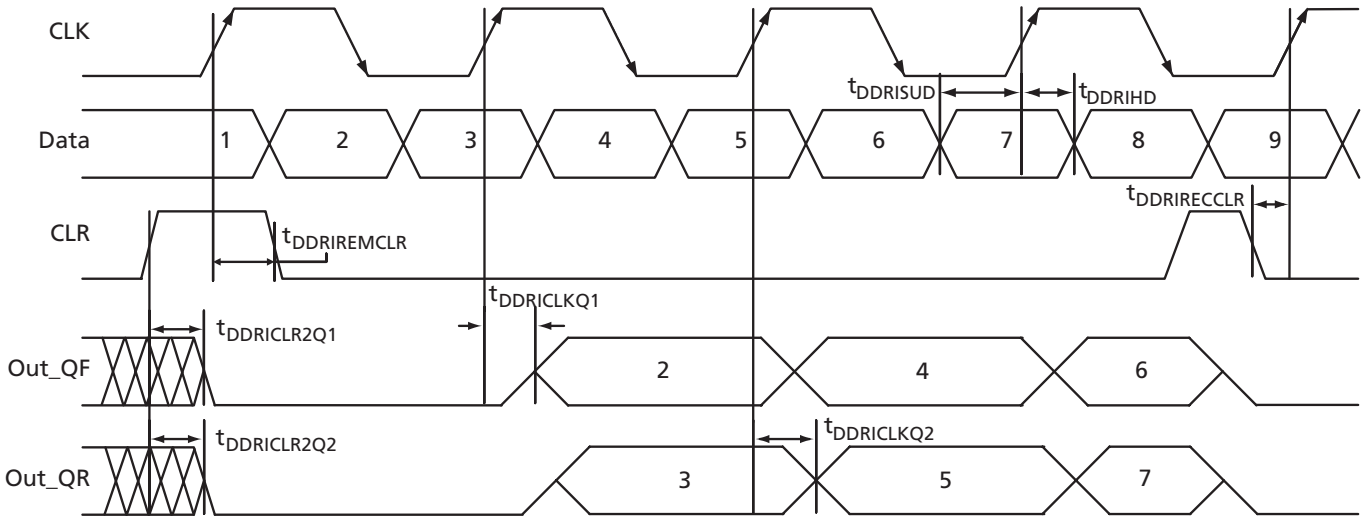


Figure 3-20 • Input DDR Timing Diagram

Timing Characteristics

Table 3-73 • Input DDR Propagation Delays
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	-2	-1	Std.	-F	Units
$t_{DDRICKQ1}$	Clock-to-Out Out_QR for Input DDR	0.63	0.71	0.84	1.01	ns
$t_{DDRICKQ2}$	Clock-to-Out Out_QF for Input DDR	0.63	0.71	0.84	1.01	ns
$t_{DDRISUD}$	Data Setup for Input DDR	0.53	0.61	0.71	0.86	ns
t_{DDRIHD}	Data Hold for Input DDR	0.00	0.00	0.00	0.00	ns
$t_{DDRICLR2Q1}$	Asynchronous Clear-to-Out Out_QR for Input DDR	0.57	0.65	0.76	0.91	ns
$t_{DDRICLR2Q2}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.57	0.65	0.76	0.91	ns
$t_{DDRIREMCLR}$	Asynchronous Clear Removal time for Input DDR	0.00	0.00	0.00	0.00	ns
$t_{DDRIRECCLR}$	Asynchronous Clear Recovery time for Input DDR	0.22	0.25	0.30	0.36	ns
$t_{DDRIWCLR}$	Asynchronous Clear Minimum Pulse Width for Input DDR					ns
$t_{DDRICKMPWH}$	Clock Minimum Pulse Width High for Input DDR					ns
$t_{DDRICKMPWL}$	Clock Minimum Pulse Width Low for Input DDR					ns
$F_{DDRIMAX}$	Maximum Frequency for Input DDR					MHz

Note: For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.

Output DDR Module

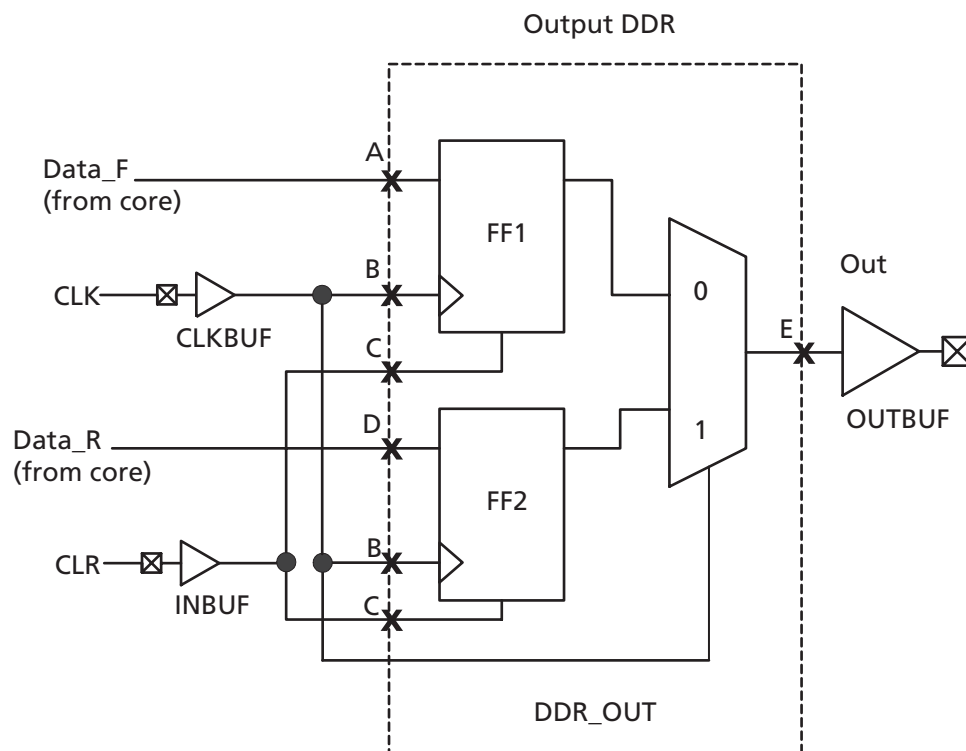


Figure 3-21 • Output DDR Timing Model

Table 3-74 • Parameter Definitions

Parameter Name	Parameter Definition	Measuring Nodes (From, To)
$t_{DDROCLKQ}$	Clock-to-Out	B, E
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out	C, E
$t_{DDROREMCLR}$	Clear Removal	C, B
$t_{DDRORECCLR}$	Clear Recovery	C, B
$t_{DDROSUD1}$	Data Setup Data_F	A, B
$t_{DDROSUD2}$	Data Setup Data_R	D, B
$t_{DDROHD1}$	Data Hold Data_F	A, B
$t_{DDROHD2}$	Data Hold Data_R	D, B

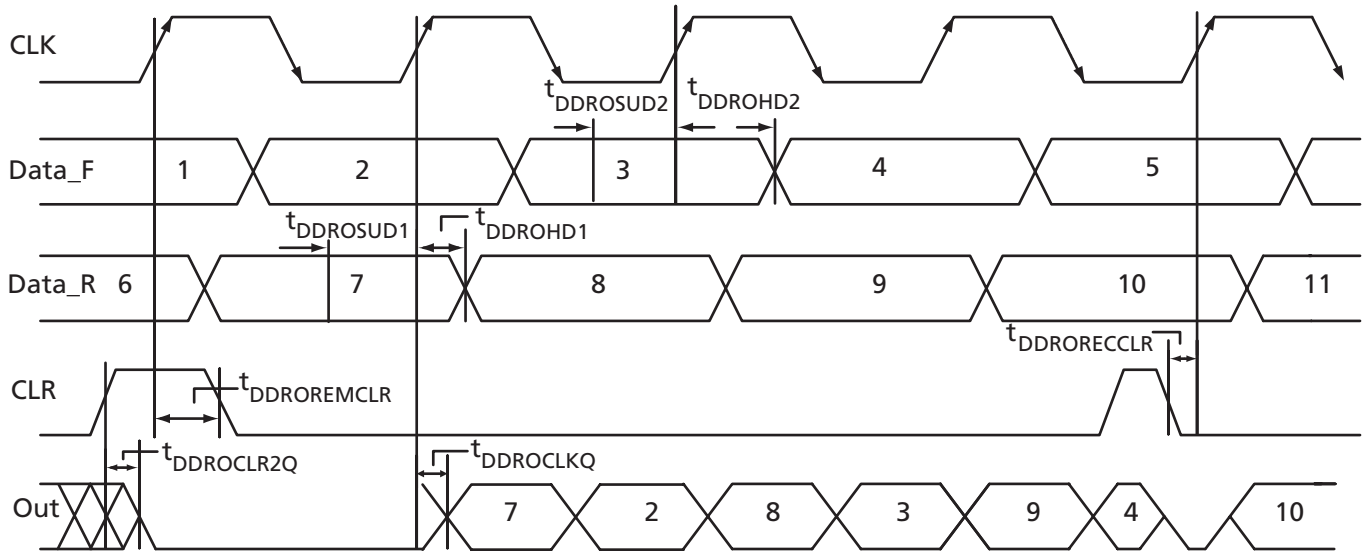


Figure 3-22 • Output DDR Timing Diagram

Timing Characteristics

Table 3-75 • Output DDR Propagation Delays
Commercial-Case Conditions: $T_j = 70^\circ\text{C}$, Worst Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	-2	-1	Std.	-F	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	0.63	0.71	0.84	1.01	ns
$t_{DDROSUD1}$	Data_F Data Setup for Output DDR	0.43	0.49	0.57	0.69	ns
$t_{DDROSUD2}$	Data_R Data Setup for Output DDR	0.43	0.49	0.57	0.69	ns
$t_{DDROHD1}$	Data_F Data Hold for Output DDR	0.00	0.00	0.00	0.00	ns
$t_{DDROHD2}$	Data_R Data Hold for Output DDR	0.00	0.00	0.00	0.00	ns
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out for Output DDR	0.57	0.65	0.76	0.91	ns
$t_{DDROEMCLR}$	Asynchronous Clear Removal time for Output DDR	0.00	0.00	0.00	0.00	ns
$t_{DDROECCLR}$	Asynchronous Clear Recovery time for Output DDR	0.22	0.25	0.30	0.36	ns
$t_{DDROWCLR1}$	Asynchronous Clear Minimum Pulse Width for Output DDR					ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width High for the Output DDR					ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width Low for the Output DDR					ns
F_{DDOMAX}	Maximum Frequency for the Output DDR					MHz

Note: For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.

VersaTile Characteristics

VersaTile Specifications as a Combinatorial Module

The ProASIC3 library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *ProASIC3/E Macro Library Guide*.

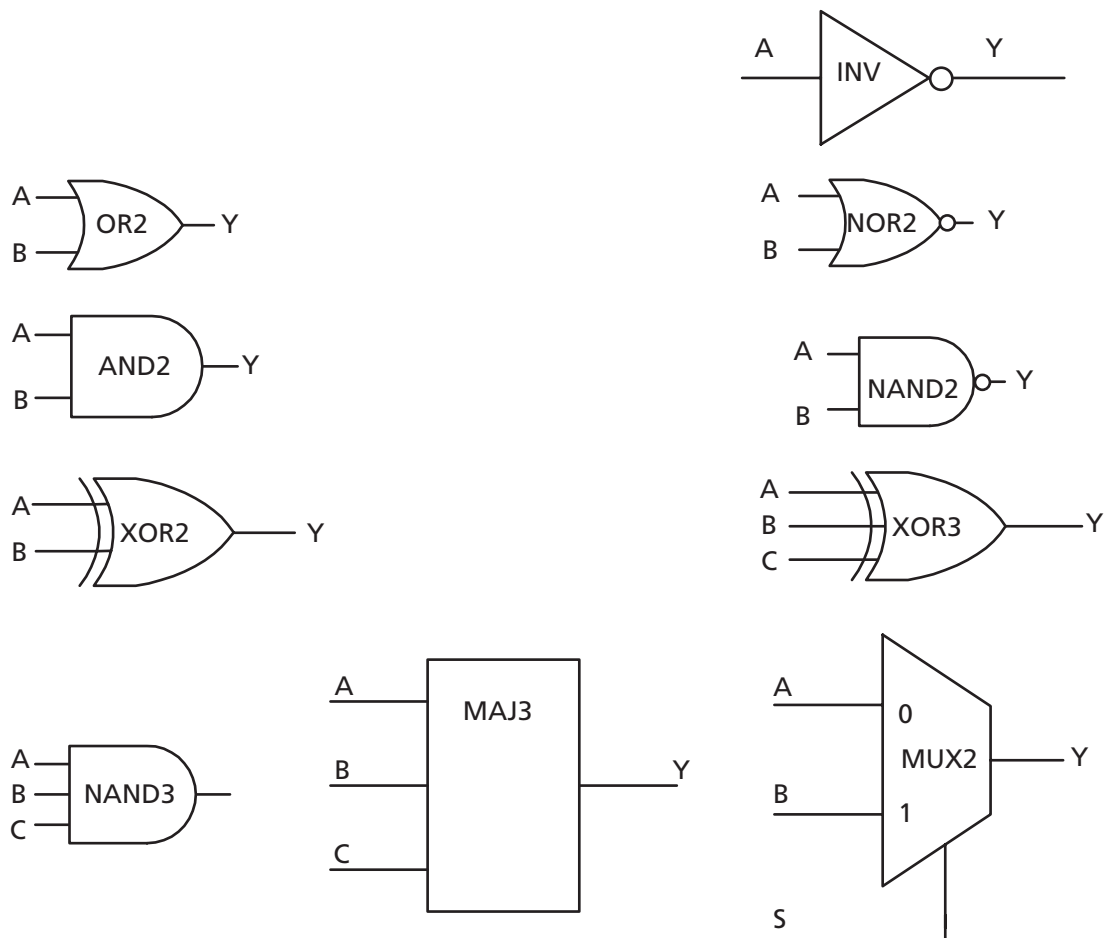


Figure 3-23 • Sample of Combinatorial Cells

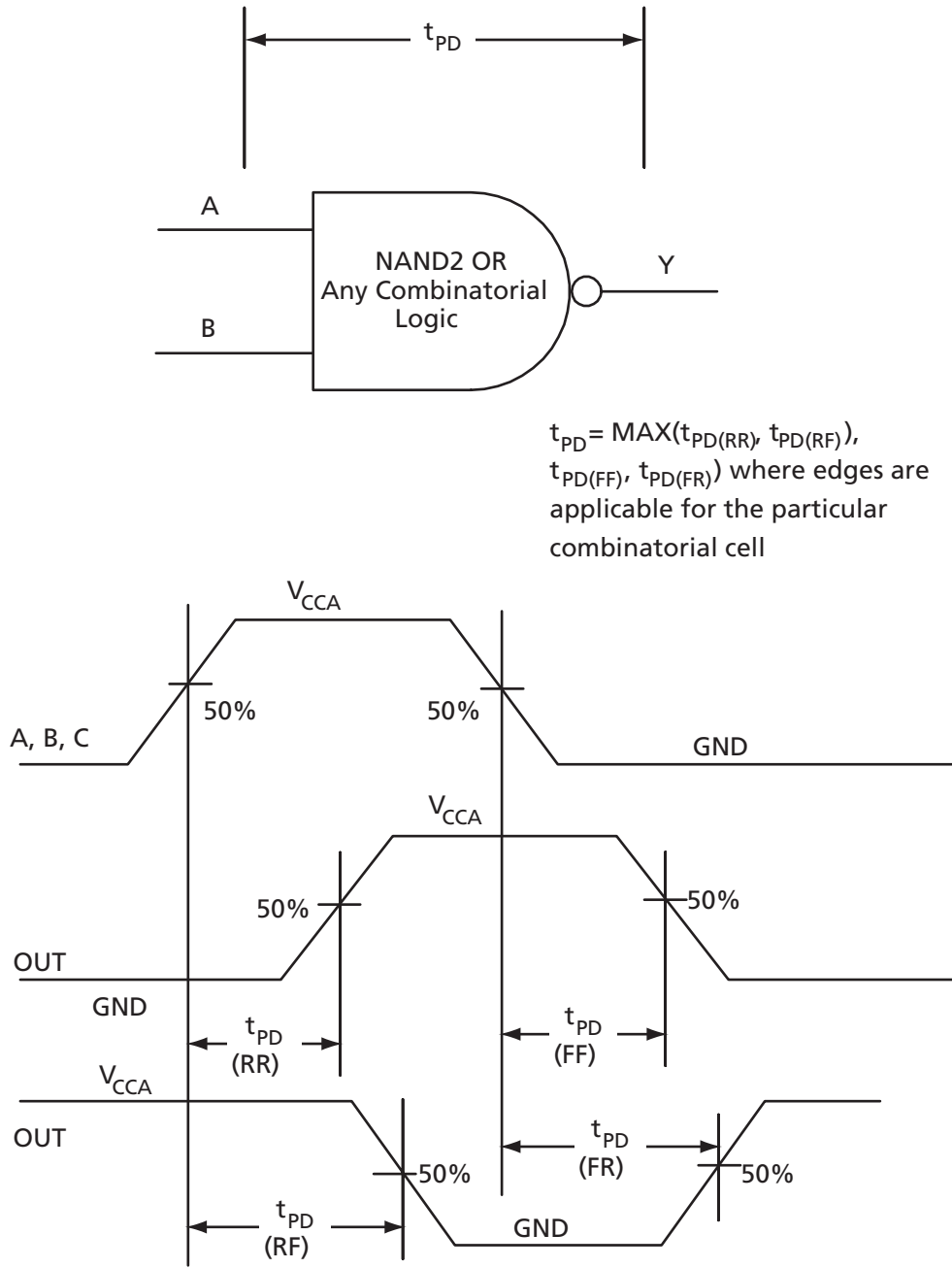


Figure 3-24 • Timing Model and Waveforms

Timing Characteristics

Table 3-76 • Combinatorial Cell Propagation Delays
Commercial-Case Conditions: $T_j = 70^\circ\text{C}$, Worst Case $V_{CC} = 1.425\text{ V}$

Combinatorial Cell	Equation	Parameter	-2	-1	Std.	-F	Units
INV	$Y = !A$	t_{PD}	0.40	0.46	0.54	0.65	ns
AND2	$Y = A \cdot B$	t_{PD}	0.47	0.54	0.63	0.76	ns
NAND2	$Y = !(A \cdot B)$	t_{PD}	0.47	0.54	0.63	0.76	ns
OR2	$Y = A + B$	t_{PD}	0.49	0.55	0.65	0.78	ns
NOR2	$Y = !(A + B)$	t_{PD}	0.49	0.55	0.65	0.78	ns
XOR2	$Y = A \oplus B$	t_{PD}	0.74	0.84	0.99	1.19	ns
MAJ3	$Y = \text{MAJ}(A, B, C)$	t_{PD}	0.70	0.79	0.93	1.12	ns
XOR3	$Y = A \oplus B \oplus C$	t_{PD}	0.87	1.00	1.17	1.41	ns
MUX2	$Y = A \text{ !S} + B \text{ S}$	t_{PD}	0.51	0.58	0.68	0.81	ns
AND3	$Y = A \cdot B \cdot C$	t_{PD}	0.56	0.64	0.75	0.90	ns

Note: For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.

VersaTile Specifications as a Sequential Module

The ProASIC3 library offers a wide variety of sequential cells including flip-flops and latches. Each have a data input and optional Enable, Clear, or Preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *ProASIC3/E Macro Library Guide*.

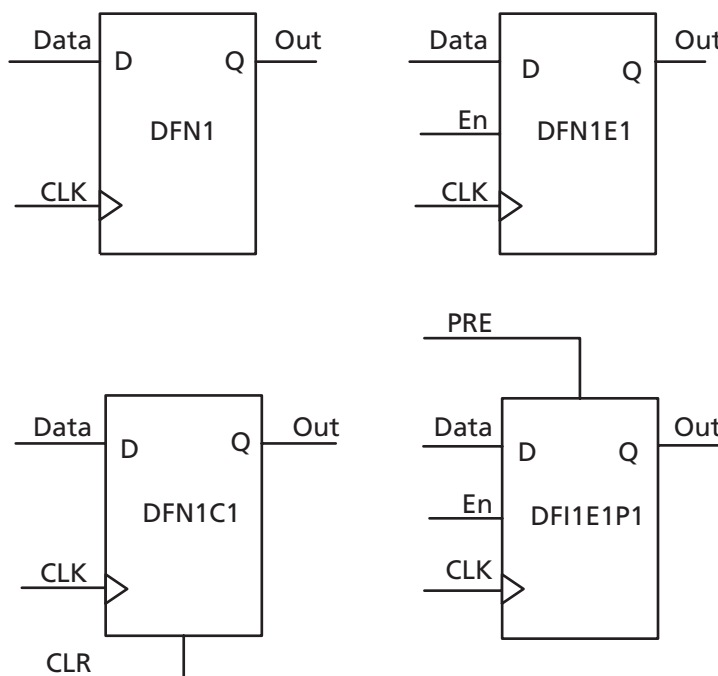


Figure 3-25 • Sample of Sequential Cells

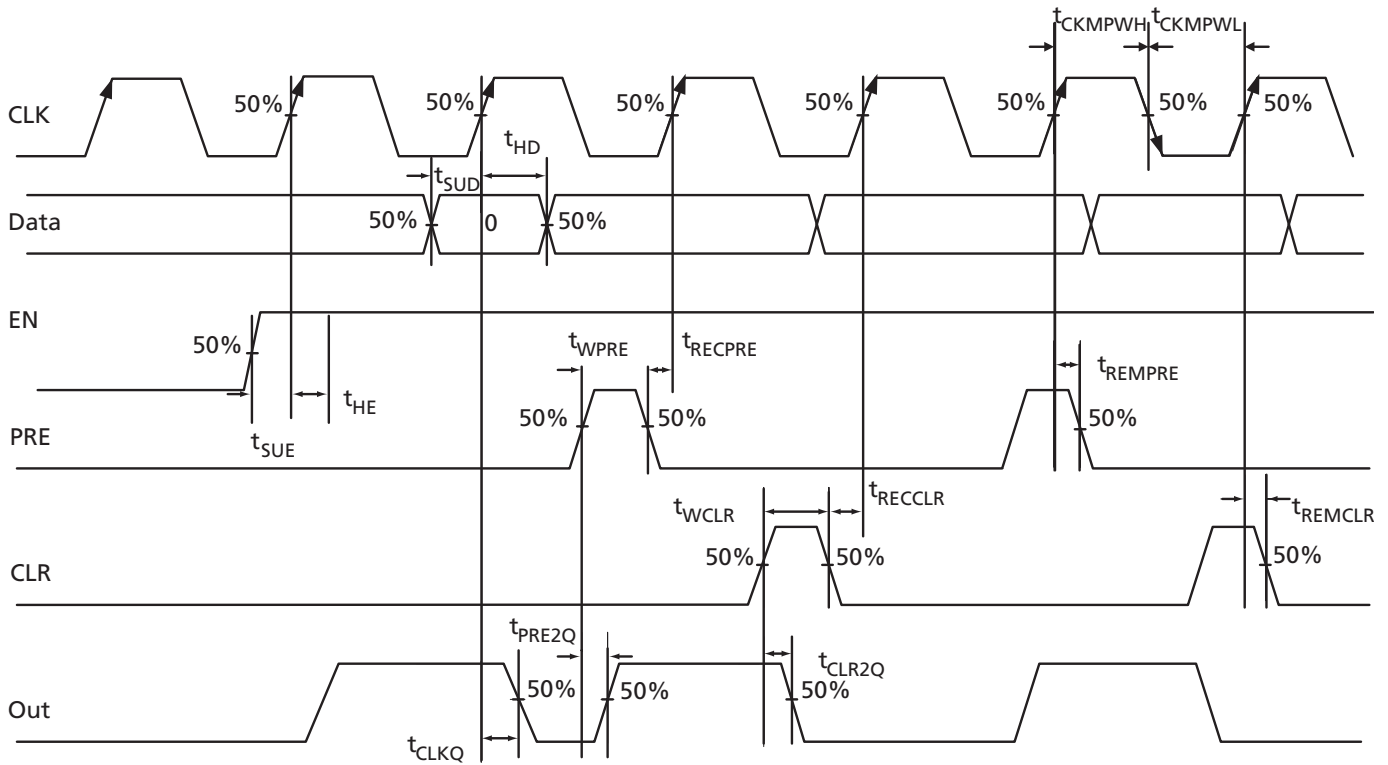


Figure 3-26 • Timing Model and Waveforms

Timing Characteristics

Table 3-77 • Register Delays
Commercial-Case Conditions: $T_j = 70^\circ\text{C}$, Worst Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	-2	-1	Std.	-F	Units
t_{CLKQ}	Clock-to-Q of the Core Register	0.55	0.63	0.74	0.89	ns
t_{SUD}	Data Setup time for the Core Register	0.43	0.49	0.57	0.69	ns
t_{HD}	Data Hold time for the Core Register	0.00	0.00	0.00	0.00	ns
t_{SUE}	Enable Setup time for the Core Register	0.45	0.52	0.61	0.73	ns
t_{HE}	Enable Hold time for the Core Register	0.00	0.00	0.00	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.40	0.45	0.53	0.64	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.40	0.45	0.53	0.64	ns
t_{REMCLR}	Asynchronous Clear Removal time for the Core Register	0.00	0.00	0.00	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery time for the Core Register	0.22	0.25	0.30	0.36	ns
t_{REMPRE}	Asynchronous Preset Removal time for the Core Register	0.00	0.00	0.00	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery time for the Core Register	0.22	0.25	0.30	0.36	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.25	0.28	0.33	0.40	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.25	0.28	0.33	0.40	ns
t_{CKMPWH}	Clock Minimum Pulse Width High for the Core Register	0.36	0.41	0.48	0.58	ns
t_{CKMPWL}	Clock Minimum Pulse Width Low for the Core Register	0.41	0.46	0.54	0.65	ns

Note: For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.

Global Resource Characteristics

A3P250 Clock Tree Topology

Clock delays are device-specific. Figure 3-27 is an example of a global tree used for clock routing. The global tree presented in Figure 3-27 is driven by a CCC located on the west side of the A3P250 device. It is used to drive all D-flip-flops in the device.

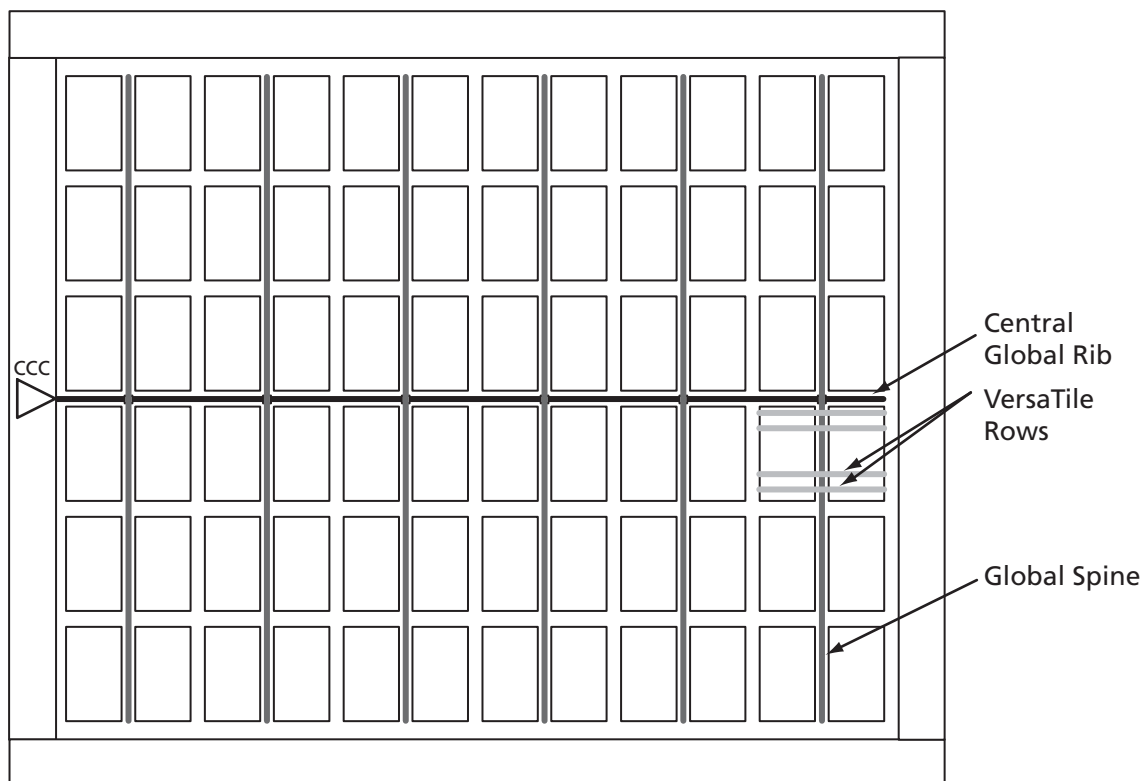


Figure 3-27 • Example of Global Tree Use in an A3P250 Device for Clock Routing

Global Tree Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard dependent and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the "Clock Conditioning Circuits" section on page 2-13. Table 3-78 to Table 3-83 on page 3-64 present minimum and maximum global clock delays within each device. Minimum and maximum delays are measured with minimum and maximum loading.

Timing Characteristics

Table 3-78 • A3P060 Global Resource
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	-2		-1		Std.		-F		Units
		Min. ¹	Max. ²	Min. ¹	Max. ²	Min. ¹	Max. ²	Min. ¹	Max. ²	
t _{RCKL}	Input Low Delay for Global Clock	0.71	0.93	0.81	1.05	0.95	1.24	1.14	1.49	ns
t _{RCKH}	Input High Delay for Global Clock	0.70	0.96	0.80	1.09	0.94	1.28	1.13	1.54	ns
t _{RCKMPWH}	Minimum Pulse Width High for Global Clock									ns
t _{RCKMPWL}	Minimum Pulse Width Low for Global Clock									ns
t _{RCKSW}	Maximum Skew for Global Clock		0.26		0.29		0.34		0.41	ns
F _{RMAX}	Maximum Frequency for Global Clock									MHz

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.

Table 3-79 • A3P125 Global Resource
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	-2		-1		Std.		-F		Units
		Min. ¹	Max. ²	Min. ¹	Max. ²	Min. ¹	Max. ²	Min. ¹	Max. ²	
t _{RCKL}	Input Low Delay for Global Clock	0.77	0.99	0.87	1.12	1.03	1.32	1.24	1.58	ns
t _{RCKH}	Input High Delay for Global Clock	0.76	1.02	0.87	1.16	1.02	1.37	1.23	1.64	ns
t _{RCKMPWH}	Minimum Pulse Width High for Global Clock									ns
t _{RCKMPWL}	Minimum Pulse Width Low for Global Clock									ns
t _{RCKSW}	Maximum Skew for Global Clock		0.26		0.29		0.34		0.41	ns
F _{RMAX}	Maximum Frequency for Global Clock									MHz

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.

Table 3-80 • **A3P250 Global Resource**
 Commercial-Case Conditions: $T_j = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	-2		-1		Std.		-F		Units
		Min. ¹	Max. ²	Min. ¹	Max. ²	Min. ¹	Max. ²	Min. ¹	Max. ²	
t _{RCKL}	Input Low Delay for Global Clock	0.80	1.01	0.91	1.15	1.07	1.36	1.28	1.63	ns
t _{RCKH}	Input High Delay for Global Clock	0.78	1.04	0.89	1.18	1.04	1.39	1.25	1.66	ns
t _{RCKMPWH}	Minimum Pulse Width High for Global Clock									ns
t _{RCKMPWL}	Minimum Pulse Width Low for Global Clock									ns
t _{RCKSW}	Maximum Skew for Global Clock		0.26		0.29		0.34		0.41	ns
F _{RMAX}	Maximum Frequency for Global Clock									MHz

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage-supply levels, refer to [Table 3-6 on page 3-4](#) for derating values.

Table 3-81 • **A3P400 Global Resource**
 Commercial-Case Conditions: $T_j = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	-2		-1		Std.		-F		Units
		Min. ¹	Max. ²	Min. ¹	Max. ²	Min. ¹	Max. ²	Min. ¹	Max. ²	
t _{RCKL}	Input Low Delay for Global Clock	0.87	1.09	0.99	1.24	1.17	1.46	1.40	1.75	ns
t _{RCKH}	Input High Delay for Global Clock	0.86	1.11	0.98	1.27	1.15	1.49	1.38	1.79	ns
t _{RCKMPWH}	Minimum Pulse Width High for Global Clock									ns
t _{RCKMPWL}	Minimum Pulse Width Low for Global Clock									ns
t _{RCKSW}	Maximum Skew for Global Clock		0.26		0.29		0.34		0.41	ns
F _{RMAX}	Maximum Frequency for Global Clock									Mhz

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage-supply levels, refer to [Table 3-6 on page 3-4](#) for derating values.

Table 3-82 • A3P600 Global Resource
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	-2		-1		Std.		-F		Units
		Min. ¹	Max. ²	Min. ¹	Max. ²	Min. ¹	Max. ²	Min. ¹	Max. ²	
t _{RCKL}	Input Low Delay for Global Clock	0.87	1.09	0.99	1.24	1.17	1.46	1.40	1.75	ns
t _{RCKH}	Input High Delay for Global Clock	0.86	1.11	0.98	1.27	1.15	1.49	1.38	1.79	ns
t _{RCKMPWH}	Minimum Pulse Width High for Global Clock									ns
t _{RCKMPWL}	Minimum Pulse Width Low for Global Clock									ns
t _{RCKSW}	Maximum Skew for Global Clock		0.26		0.29		0.34		0.41	ns
F _{RMAX}	Maximum Frequency for Global Clock									MHz

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.

Table 3-83 • A3P1000 Global Resource
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	-2		-1		Std.		-F		Units
		Min. ¹	Max. ²	Min. ¹	Max. ²	Min. ¹	Max. ²	Min. ¹	Max. ²	
t _{RCKL}	Input Low Delay for Global Clock	0.94	1.16	1.07	1.32	1.26	1.55	1.51	1.86	ns
t _{RCKH}	Input High Delay for Global Clock	0.93	1.19	1.06	1.35	1.24	1.59	1.49	1.91	ns
t _{RCKMPWH}	Minimum Pulse Width High for Global Clock									ns
t _{RCKMPWL}	Minimum Pulse Width Low for Global Clock									ns
t _{RCKSW}	Maximum Skew for Global Clock		0.26		0.29		0.35		0.41	ns
F _{RMAX}	Maximum Frequency for Global Clock									MHz

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.

Embedded SRAM and FIFO Characteristics

SRAM

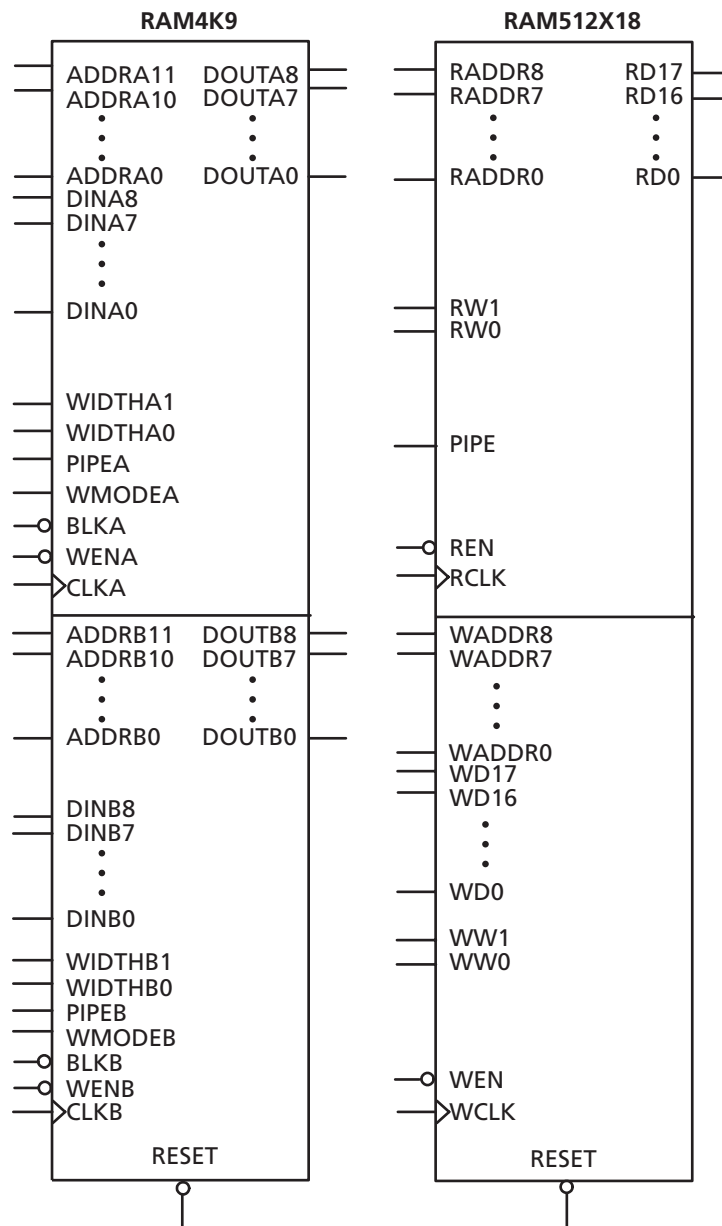


Figure 3-28 • RAM Models

Timing Waveforms

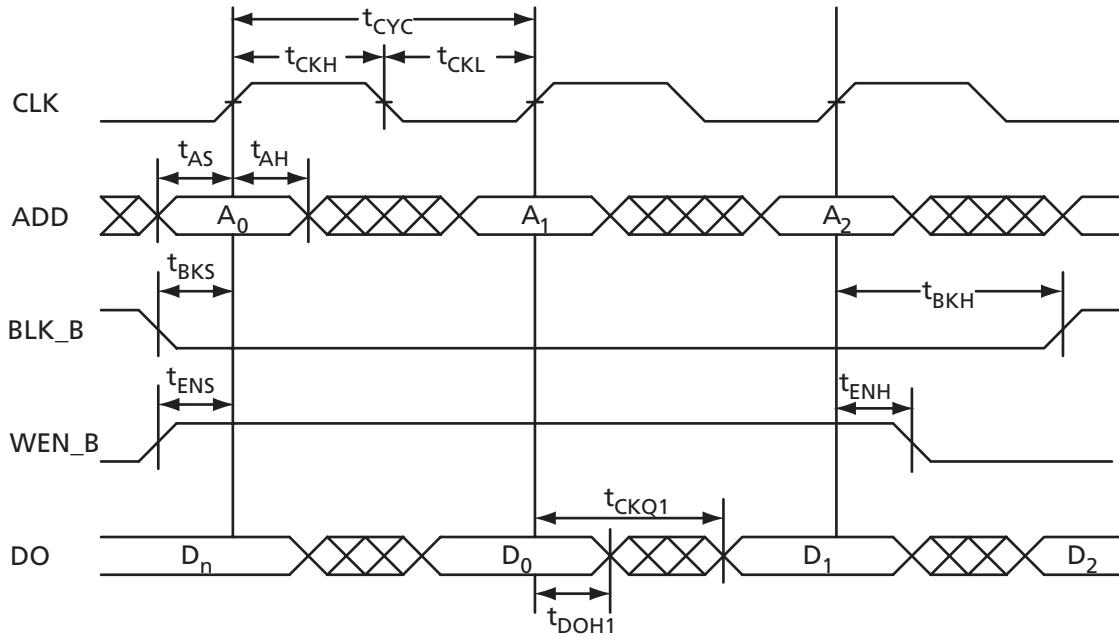


Figure 3-29 • RAM Read for Pass-Through Output

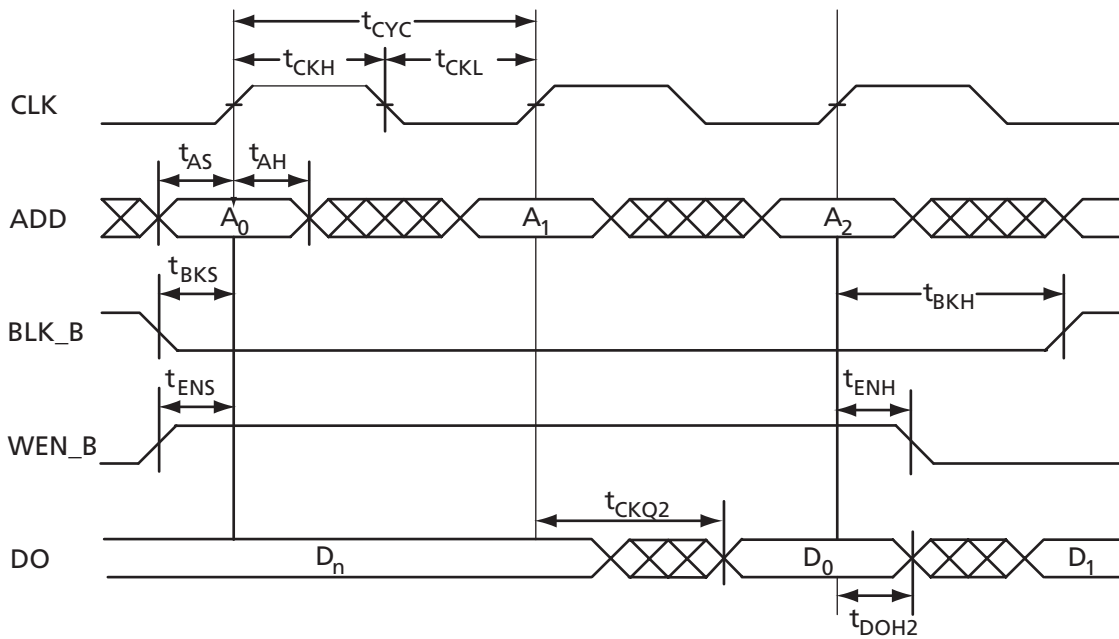


Figure 3-30 • RAM Read for Pipelined Output

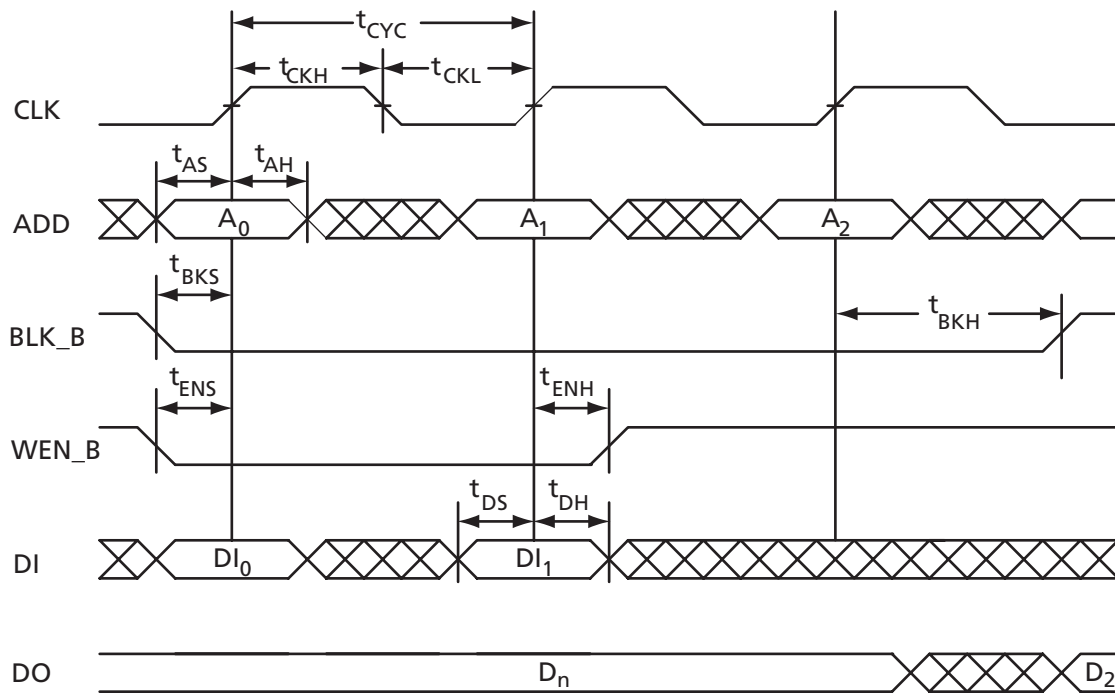


Figure 3-31 • RAM Write, Output Retained (WMODE = 0)

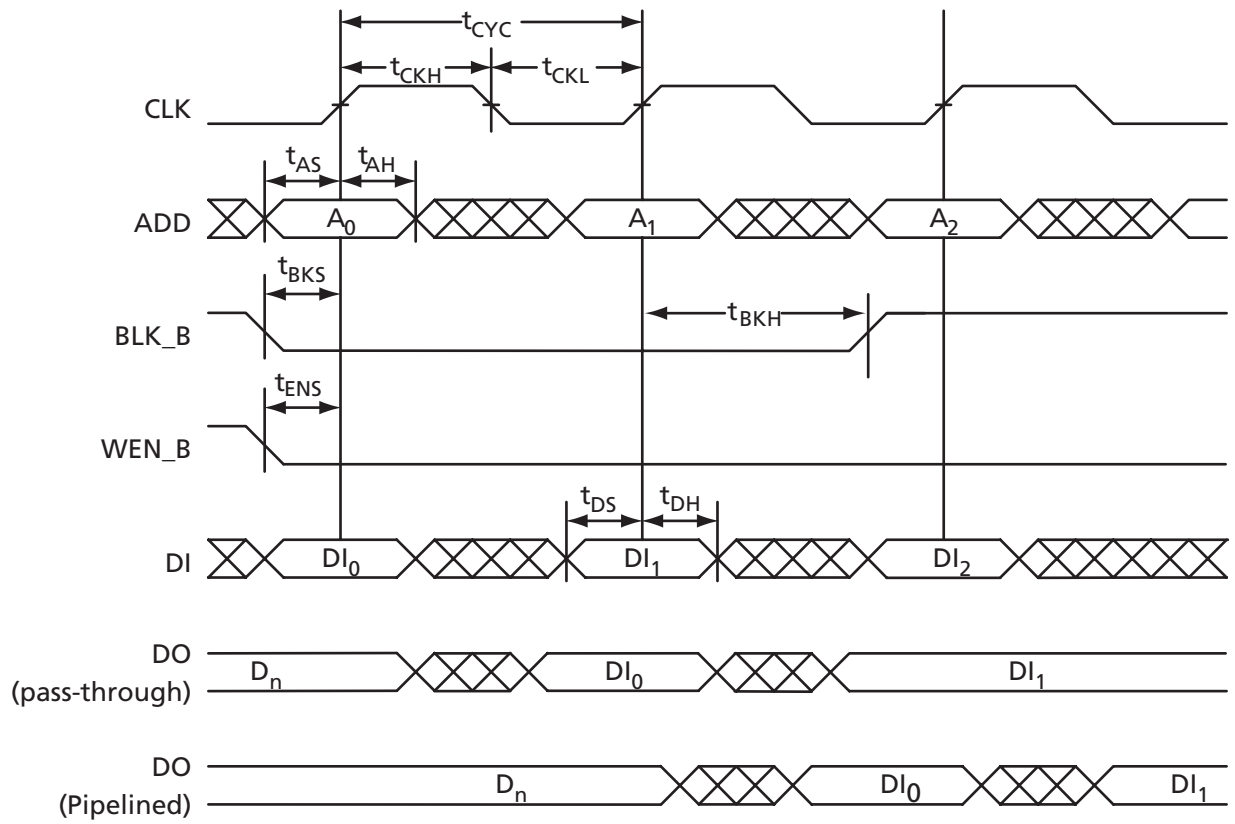


Figure 3-32 • RAM Write, Output as Write Data (WMODE = 1)

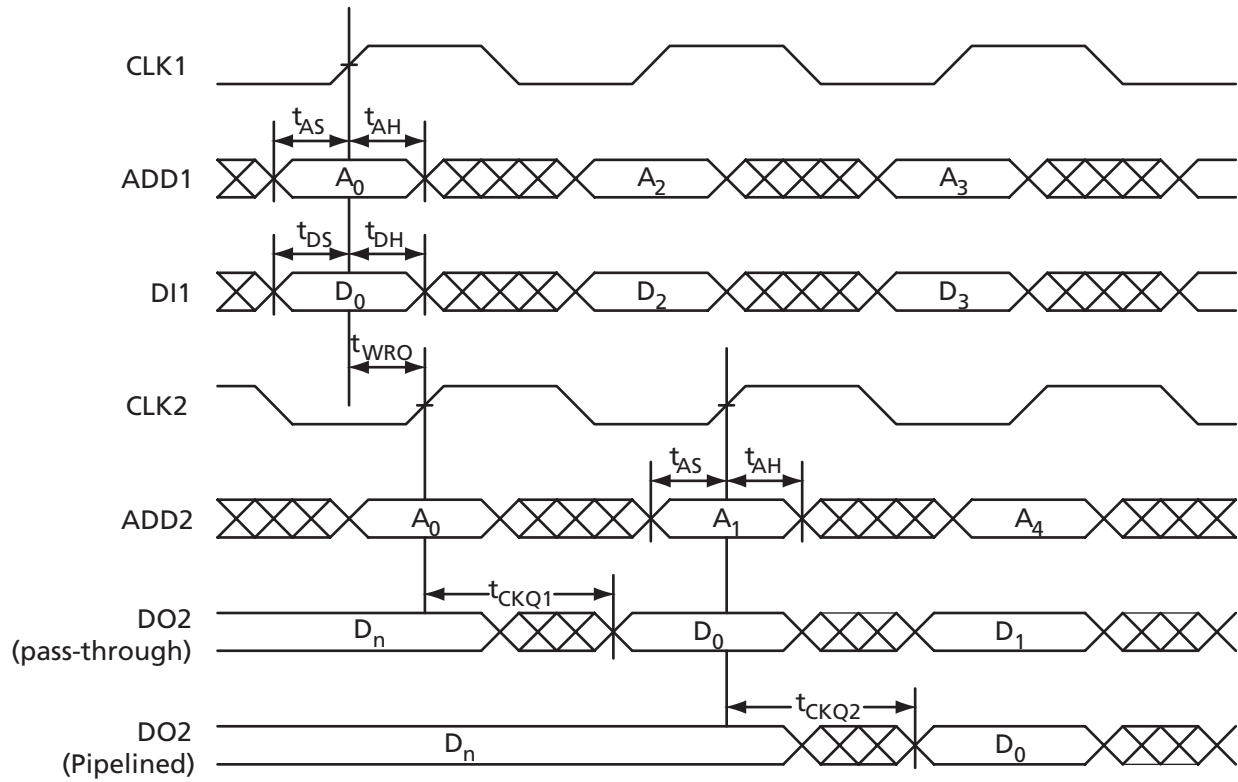


Figure 3-33 • One Port Write/Other Port Read Same

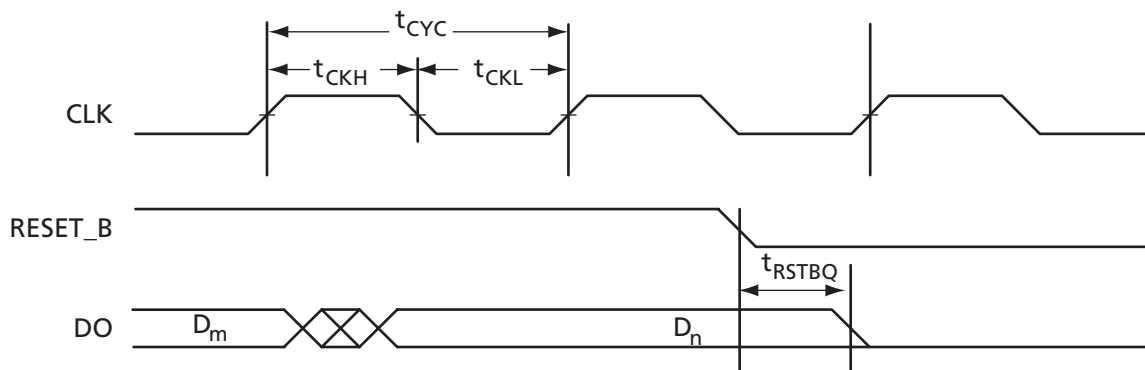


Figure 3-34 • RAM Reset

Timing Characteristics

Table 3-84 • RAM4K9

Commercial-Case Conditions: $T_j = 70^\circ\text{C}$, Worst Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	-2	-1	Std.	-F	Units
t_{AS}	Address Setup time	0.25	0.28	0.33	0.40	ns
t_{AH}	Address Hold time	0.00	0.00	0.00	0.00	ns
t_{ENS}	REN_B, WEN_B Setup time	0.14	0.16	0.19	0.23	ns
t_{ENH}	REN_B, WEN_B Hold time	0.10	0.11	0.13	0.16	ns
t_{BKS}	BLK_B Setup time	0.23	0.27	0.31	0.37	ns
t_{BKH}	BLK_B Hold time	0.02	0.02	0.02	0.03	ns
t_{DS}	Input data (DI) Setup time	0.18	0.21	0.25	0.29	ns
t_{DH}	Input data (DI) Hold time	0.00	0.00	0.00	0.00	ns
t_{CKQ1}	Clock High to New Data Valid on DO (output retained, WMODE = 0)	1.79	2.03	2.39	2.87	ns
	Clock High to New Data Valid on DO (pass-through, WMODE = 1)	2.36	2.68	3.15	3.79	ns
t_{CKQ2}	Clock HIGH to New Data Valid on DO (pipelined)	0.89	1.02	1.20	1.44	ns
t_{RSTBQ}	RESET_B Low to Data Out Low on DO (pass-through)	0.92	1.05	1.23	1.48	ns
	RESET_B Low to Data Out Low on DO (pipelined)	0.92	1.05	1.23	1.48	ns
$t_{REMRSTB}$	RESET_B Removal	0.25	0.28	0.33	0.40	ns
$t_{RECRSTB}$	RESET_B Recovery	1.49	1.68	1.98	2.38	ns
$t_{MPWRSTB}$	RESET_B Minimum Pulse Width	0.22	0.25	0.29	0.35	ns
t_{CYC}	Clock Cycle time	1.99	2.26	2.66	3.19	ns

Note: For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.

Table 3-85 • RAM512X18

Commercial-Case Conditions: $T_j = 70^\circ\text{C}$, Worst Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	-2	-1	Std.	-F	Units
t_{AS}	Address Setup time	0.25	0.28	0.33	0.40	ns
t_{AH}	Address Hold time	0.00	0.00	0.00	0.00	ns
t_{ENS}	REN_B, WEN_B Setup time	0.18	0.20	0.24	0.28	ns
t_{ENH}	REN_B, WEN_B Hold time	0.06	0.07	0.08	0.09	ns
t_{DS}	Input data (DI) Setup time	0.18	0.21	0.25	0.29	ns
t_{DH}	Input data (DI) Hold time	0.00	0.00	0.00	0.00	ns
t_{CKQ1}	Clock High to New Data Valid on DO (output retained, WMODE = 0)	2.16	2.46	2.89	3.47	ns
t_{CKQ2}	Clock High to New Data Valid on DO (pipelined)	0.90	1.02	1.20	1.44	ns
t_{RSTBQ}	RESET_B Low to Data Out Low on DO (pass-through)	0.92	1.05	1.23	1.48	ns
	RESET_B Low to Data Out Low on DO (pipelined)	0.92	1.05	1.23	1.48	ns
$t_{REMRSTB}$	RESET_B Removal	0.25	0.28	0.33	0.40	ns
$t_{RECRSTB}$	RESET_B Recovery	1.49	1.68	1.98	2.38	ns
$t_{MPWRSTB}$	RESET_B Minimum Pulse Width	0.22	0.25	0.29	0.35	ns
t_{CYC}	Clock Cycle time	1.99	2.26	2.66	3.19	ns

Note: For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.

FIFO

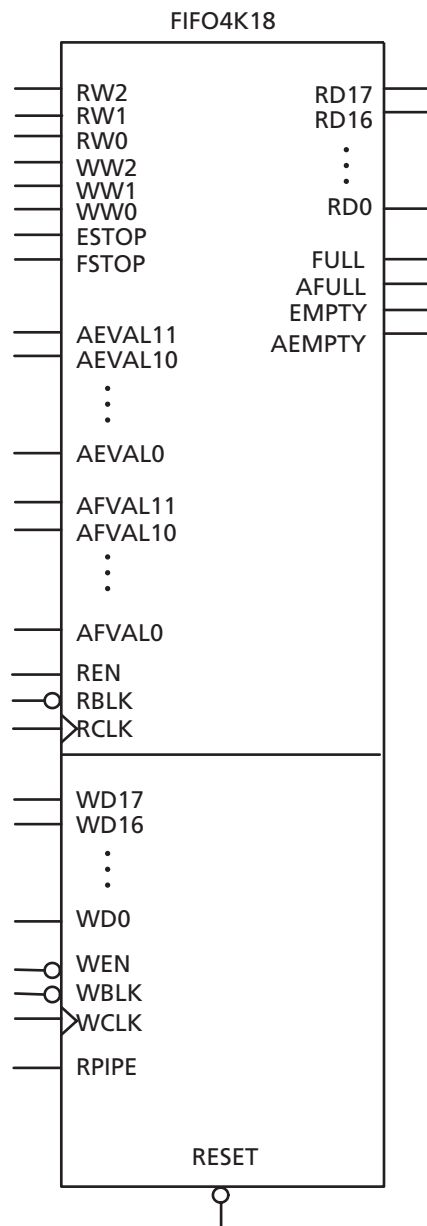


Figure 3-35 • FIFO Model

Timing Waveforms

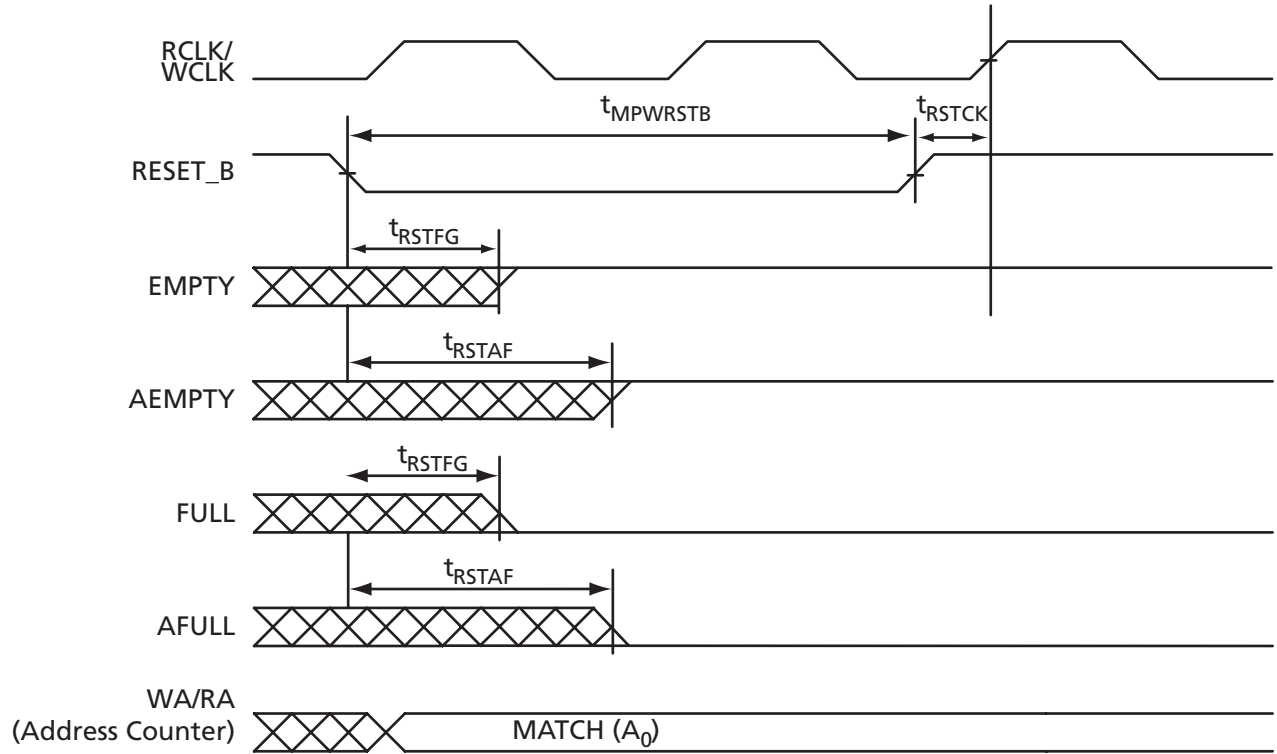


Figure 3-36 • FIFO Reset

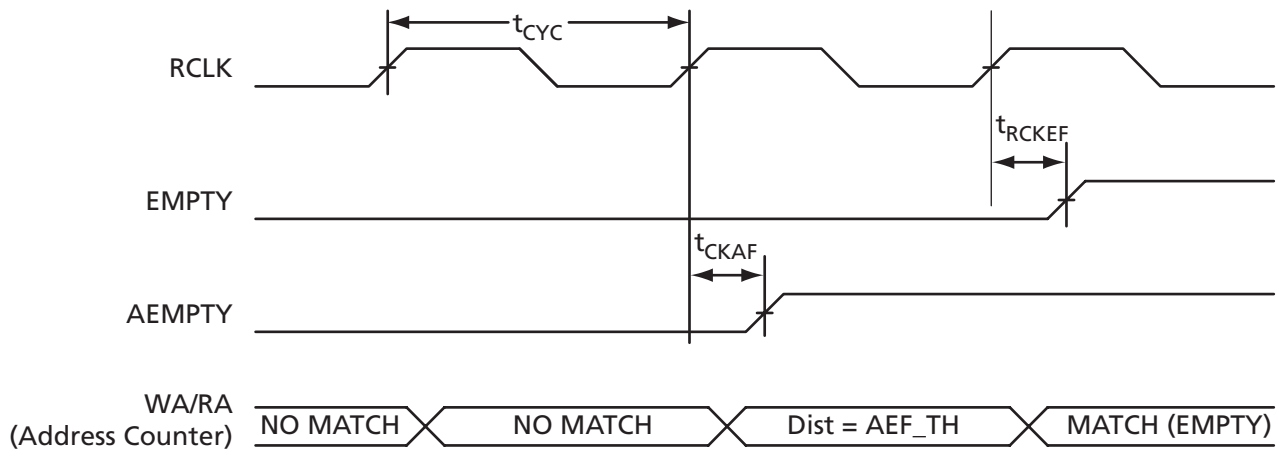


Figure 3-37 • FIFO EMPTY Flag and AEMPTY Flag Assertion

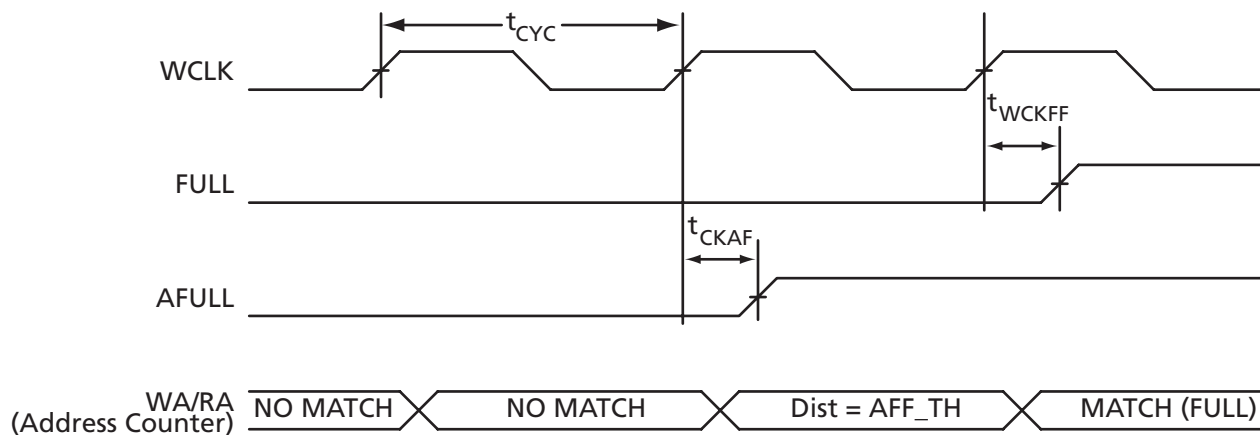


Figure 3-38 • FIFO FULL Flag and AFULL Flag Assertion

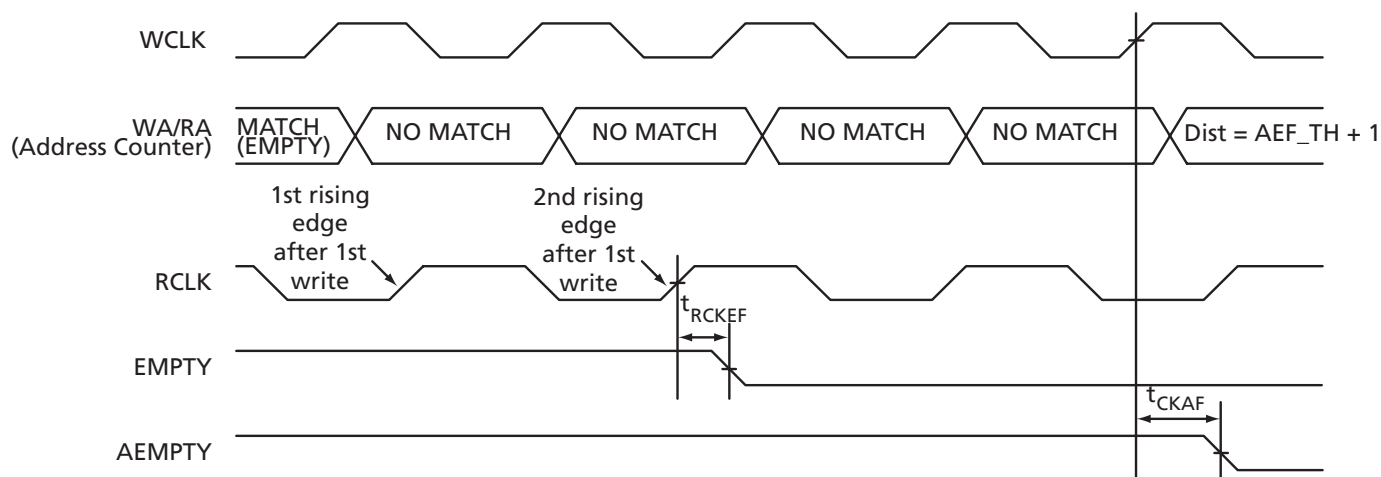


Figure 3-39 • FIFO EMPTY Flag and AEMPTY Flag Deassertion

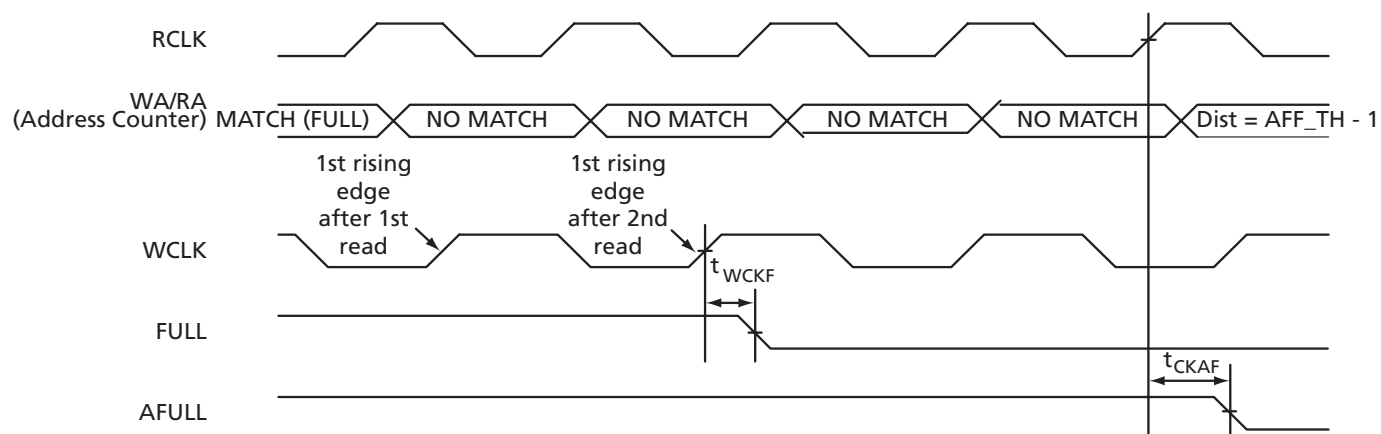


Figure 3-40 • FIFO FULL Flag and AFULL Flag Deassertion

Timing Characteristics

Table 3-86 • FIFO
Commercial-Case Conditions: $T_j = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	-2	-1	Std.	-F	Units
t_{ENS}	REN_B, WEN_B Setup time	0.21	0.24	0.29	0.35	ns
t_{ENH}	REN_B, WEN_B Hold time	0.02	0.02	0.02	0.03	ns
t_{BKS}	BLK_B Setup time	0.19	0.22	0.26	0.31	ns
t_{BKH}	BLK_B Hold time	0.00	0.00	0.00	0.00	ns
t_{DS}	Input data (DI) Setup time	0.18	0.21	0.25	0.29	ns
t_{DH}	Input data (DI) Hold time	0.00	0.00	0.00	0.00	ns
t_{CKQ1}	Clock High to New Data Valid on DO (pass-through)	2.36	2.68	3.15	3.79	ns
t_{CKQ2}	Clock High to New Data Valid on DO (pipelined)	0.89	1.02	1.20	1.44	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	1.72	1.96	2.30	2.76	ns
t_{WCKFF}	WCLK High to Full Flag Valid	1.63	1.86	2.18	2.62	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	3.77	4.30	5.05	6.07	ns
t_{RSTFG}	RESET_B Low to Empty/Full Flag valid	1.69	1.93	2.27	2.72	ns
t_{RSTAF}	RESET_B Low to Almost-Empty/Full Flag Valid	3.66	4.17	4.90	5.89	ns
t_{RSTBQ}	RESET_B Low to Data out Low on DO (pass-through)	0.92	1.05	1.23	1.48	ns
	RESET_B Low to Data out Low on DO (pipelined)	0.92	1.05	1.23	1.48	ns
$t_{REMRSTB}$	RESET_B Removal	0.25	0.28	0.33	0.39	ns
$t_{RECRSTB}$	RESET_B Recovery	1.46	1.65	1.94	2.33	ns
$t_{MPWRSTB}$	RESET_B Minimum Pulse Width	0.20	0.23	0.27	0.32	ns
t_{CYC}	Clock Cycle time	1.85	2.09	2.46	2.95	ns

Note: For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.

Embedded FlashROM Characteristics

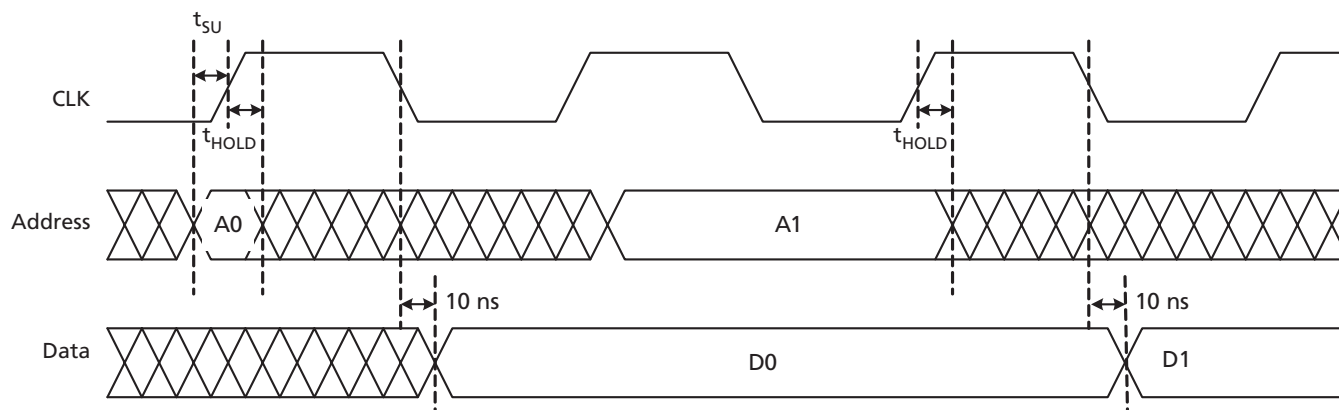


Figure 3-41 • Timing Diagram

Timing Characteristics

Table 3-87 • Embedded FlashROM Access Time

Parameter	Description	-2	-1	Std.	Units
t_{SU}	Address setup Time	TBD	TBD	TBD	ns
t_{HOLD}	Address Hold Time	TBD	TBD	TBD	ns
t_{CK2Q}	Clock to out	TBD	TBD	TBD	ns
FMAX	Maximum Clock frequency	TBD	TBD	TBD	MHz

JTAG 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected, refer to the I/O Timing characteristics for more details.

Timing Characteristics

Table 3-88 • JTAG 1532

Commercial-Case Conditions: $T_j = 70^\circ\text{C}$, Worst Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	-2	-1	Std.	Units
t_{DISU}	Test Data Input Setup Time				ns
t_{DIHD}	Test Data Input Hold Time				ns
t_{TMSSU}	Test Mode Select Setup Time				ns
t_{TMDHD}	Test Mode Select Hold Time				ns
t_{TCK2Q}	Clock to Q (Data Out)				ns
t_{RSTB2Q}	Reset to Q (Data Out)				ns
F_{TCKMAX}	TCK maximum frequency	20	20	20	MHz
$t_{TRSTREM}$	ResetB Removal time				ns
$t_{TRSTREC}$	ResetB Recovery time				ns
$t_{TRSTMPW}$	ResetB minimum pulse				ns

Note: For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.