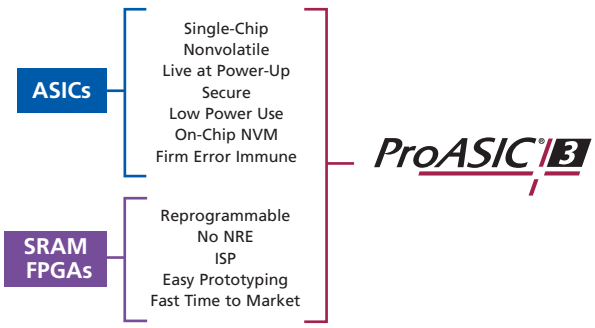
Actel®

ProASIC®3 Flash FPGAs

THE SINGLE-CHIP, LOWEST COST PRODUCTION FPGA SOLUTION

The ProASIC3 and ProASIC3E families of Flash FPGAs offer a breakthrough in price, performance, density, and features for today's most demanding high-volume applications. ProASIC3/E devices support the ARM7™ soft processor IP core offering the benefits of programmability and time-to-market at an ASIC-level unit cost. The ProASIC3/E families are based on nonvolatile Flash technology and support 30 k to 3 M gates and up to 616 high-performance I/Os.



Key Features

- Cost-Optimized, Reprogrammable, and Nonvolatile
- 1,024 Bits of User Flash Memory
- Single-Chip and Live at Power-Up
- In-System Programming (ISP) with Optional On-Chip AES Decryption
- Firm Error Immune

FlashLock

Flash FPGA Advantages that Extend B

Based on Flash technology, ProASIC3/E FPGAs provide the best features per cost solution, offering superior and unprecedented benefits over other FPGA technologies.

In addition to being low cost and high performance, Flash has the unique advantage in the FPGA market of being a secure, low-power, live-at-power-up, single-chip solution. ProASIC3/E devices are reprogrammable and offer time-to-market benefits at an ASIC-level unit cost. These features enable engineers to create high-performance, high-density systems using existing FPGA design flows and tools. In addition, the ProASIC3/E devices offer an on-chip, user nonvolatile memory storage and clock conditioning circuitry based on up to six on-board phase-locked loops (PLLs). The ProASIC3/E devices also have up to 504 kbits of true dual-port SRAM and provide typical system performance in excess of 150 MHz.

Single Chip

Flash-based FPGAs store the configuration information in on-chip Flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure and no external configuration data load is required at system power-up. Flash-based ProASIC3/E FPGAs do not require additional system components such as configuration serial nonvolatile memory (EEPROM) or a Flash-based microcontroller in order to load the device configuration data at every system power-up.

Live at Power-Up

Flash-based ProASIC3/E devices are live at power-up. As soon as system power is applied and within normal operating specifications, ProASIC3/E devices are working. The live-at-power-up feature of Flash-based ProASIC3/E devices greatly simplifies total system design and often allows for the removal of complex programmable logic devices (CPLDs) from the system that are used for this purpose. Glitches and brownouts in system power will not corrupt the ProASIC3/E devices' Flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This allows designers to reduce or completely remove the expensive power sequencing, voltage monitor, and brownout detection devices from printed

eyond Performance and Cost

circuit boards (PCB). Simplifying the total system design by using Flash-based ProASIC3/E devices reduces cost and design risk while increasing system reliability and improving system initialization time.

Security

ProASIC3/E devices incorporate the Actel FlashLock® security feature, providing a unique combination of reprogrammability and design security without external overhead. These advantages can only be offered by an FPGA with nonvolatile Flash memory. ProASIC3/E devices have a 128-bit Flash-based lock and industry-leading on-chip AES decryption core used to secure programmed intellectual property (IP) and configuration data. The AES-128-block cipher is a faster, more secure government-approved replacement for DES. ProASIC3/E devices have the most comprehensive programmable logic device security solution available today. ProASIC3/E devices with AES-based security allow for secure, remote field updates (over public networks such as the Internet) and ensure that valuable intellectual property remains out of the hands of system overbuilders, system cloners, and IP thieves. The contents of programmed ProASIC3/E devices cannot be read back, though secure (AES-based) design verification is possible. Many device design and layout techniques have been used to make invasive attacks extremely difficult. For example, Flash cells are located beneath seven metal layers, making tampering with the Flash elements extremely difficult and care has been taken to remove single points of attack in the device's programming control logic.

Firm Errors

Firm errors occur when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell in SRAM FPGAs and thus change the logic, routing, or I/Os in an unpredictable and uncontrollable way. These errors are impossible to prevent in SRAM FPGAs and can result in failure-in-time (FIT) rates in the thousands. The consequences of these types of errors may result in a complete system failure and major support and product liability issues. The configuration element of ProASIC3/E FPGAs, the Flash cell, cannot be altered by high-energy neutrons and is therefore immune to neutron effects.

Low Power

The Actel Flash-based ProASIC3/E devices exhibit power characteristics similar to an ASIC, making them an ideal choice for battery-operated and other power-sensitive applications. With ProASIC3/E devices, there is no power-on current surge and no high-current transition, which exists on many SRAM FPGAs. ProASIC3/E devices also have low static and dynamic power consumption, further maximizing power savings.

Actel | ProASIC3/E

ProASIC 3—Actel Third-Generation Flash FPGA Architect ure

1 SRAM and FIFOs

ProASIC3/E devices have embedded dual-port SRAM and FIFO blocks along the north and south sides of the device. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are: 256x18, 512x9, 1kx4, 2kx2, or 4kx1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. Dedicated FIFO control logic enables flexible and efficient FIFO implementations.

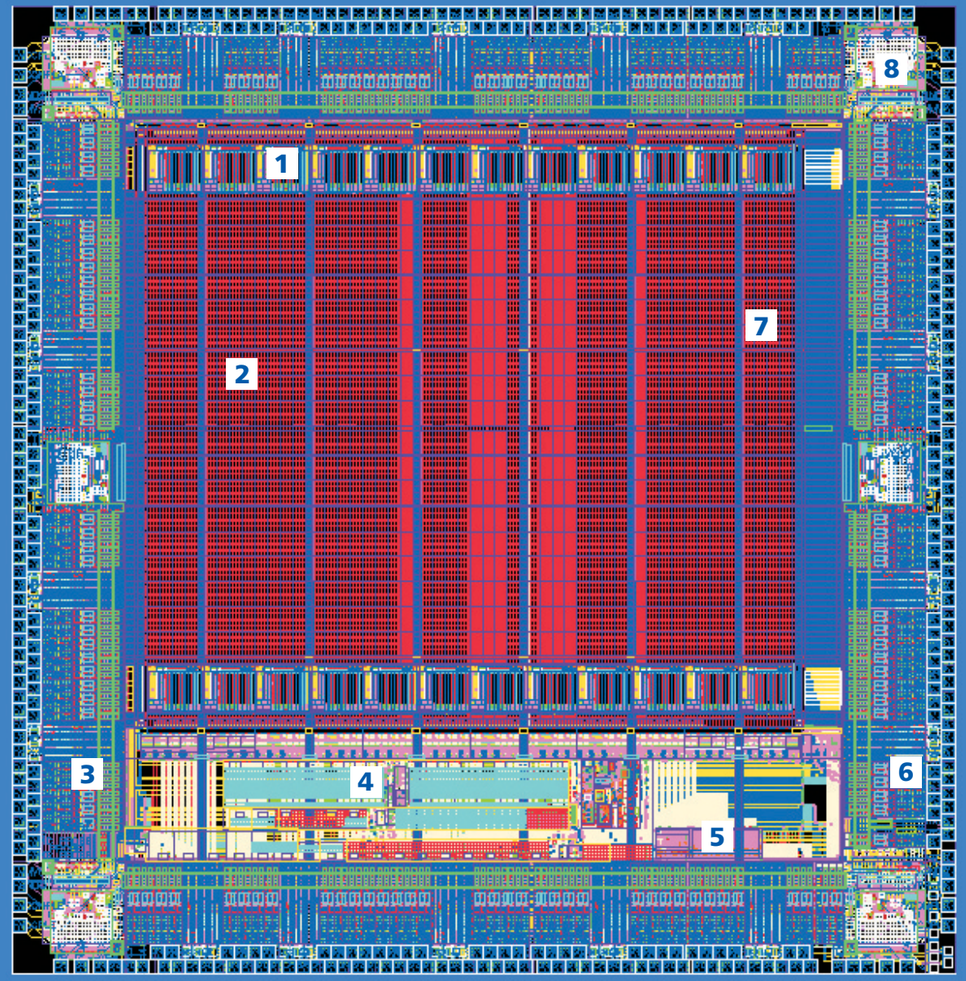
2 VersaTile

The ProASIC3/E VersaTile elements allow synthesis and mapping tools to use any tile as a three-input look-up table equivalent, a D-flip-flop, or latch (with or without enable). ProASIC3/E devices with VersaTiles offer an abundance of registers so you can often choose a smaller device and still meet register requirements.

3 Advanced I/O Standards

ProASIC3/E devices support up to 19 advanced I/O standards:

- 700 Mbps LVDS capable DDR I/Os
- Up to 8 different I/O banks per chip
- Single-Ended I/O Standards: LVTTL, LVCMOS3.3 V / 2.5 V / 1.8 V / 1.5 V, 3.3 V PCI / 3.3 V PCI-X, and LVCMOS 2.5 V / 5.0 V input
- Differential I/O Standards: LVPECL and LVDS
- Voltage-Referenced I/O Standards (ProASIC3E only): GTL+2.5 V / 3.3 V, GTL2.5 V / 3.3 V, HSTL Class 1 and 2, SSTL2 Class 1 and 2, SSTL3 Class 1 and 2
- Registered I/Os
- Hot-swap compliant I/Os
- Programmable slew rate and drive strength on outputs
- Programmable delay, weak pull-up/down
- Schmitt-trigger option on inputs (ProASIC3E only)
- Pin compatibility across a given package



4 Charge Pumps

ProASIC3/E devices can be programmed from a single 3.3 V supply voltage. If remote programming is not required, then ProASIC3/E devices can be run off a single 1.5 V supply.

5 FlashROM (FROM)

ProASIC3/E Flash FPGAs include user Flash memory. 1 kbit of Flash memory, arranged in eight 128-bit pages, allows for diverse applications support, such as device serialization, secure application key storage, revision control, and selective feature enabling.

6 JTAG (IEEE1532)

ProASIC3/E devices use industry-standard JTAG programming (IEEE1532). In addition, ProASIC3/E devices support board-level JTAG (IEEE1149) I/O boundary scan.

7 Routing Structure

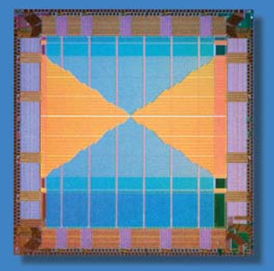
ProASIC3/E provides millions of Flash cell switches and an abundance of hierarchical routing resources, enabling extensive design and routing flexibility.

VersaNet (segmented global) routing allows high-fanout nets to traverse small or large areas of the ProASIC3/E devices with low skew and flexibility. The VersaNet network is used automatically by the software tools to route clocks and high-fanout nets.

8 PLL and CCC

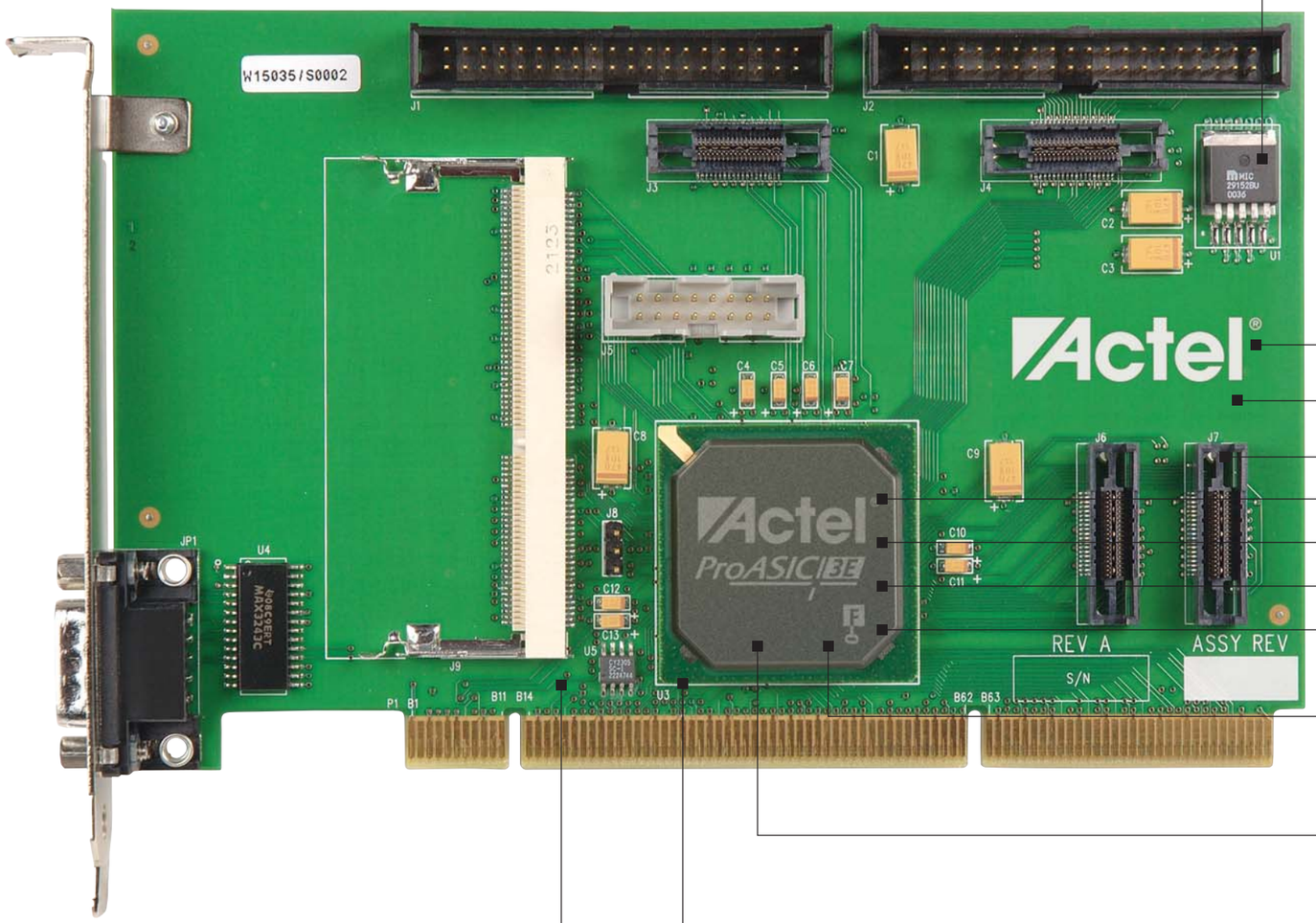
ProASIC3/E devices have six Clock Conditioning Circuits (CCCs) with up to six PLLs.

- Wide input frequency range (f_{IN_CCC}) = 1.5 to 350 MHz
- Output frequency range (f_{OUT_CCC}) = 0.75 to 350 MHz
- Output phase shift = 0°, 90°, 180°, and 270°



Extensive power bussing gives ProASIC3 micro-photography its distinctive “bow tie” appearance.

The Lowest Total System Cost with ProASIC3/E Flash FPGAs



Single-Voltage Solution

Once the ProASIC3/E device has been programmed, and assuming 1.5 V I/O standards are used, the device can be powered from a single 1.5 V supply. Unlike some SRAM FPGAs, there is no requirement for a 2.5 V or 3.3 V supply for power-up. The FPGA configuration information is stored on the chip in nonvolatile Flash as part of the FPGA fabric. Running the whole system on a single 1.5 V supply saves the cost and area associated with voltage regulators.

No Live At Power-Up (LAPU) CPLD Required

ProASIC3/E Flash-based FPGAs are live at power-up (LAPU). CPLDs are unnecessary to start your system during power-up, saving total system cost.

Reduced Board Space

Fewer components in your system lead to reduced PCB area, increased reliability, simpler inventory management, and total system cost savings.

ISP Header

ISP uses the industry-standard JTAG (IEEE1532) protocol. In addition, configuration data can be decrypted using the on-chip AES-decryption core. This allows for secure FPGA updates to be sent over public networks (e.g., the Internet) and decrypted on-chip. The FROM data can also be sent to the ProASIC3/E device encrypted if required. No expensive service call is required to update the FPGA code.

Single Chip

No boot PROM or Flash MCU is required to load the FPGA at system power-up. This results in a reduced PCB area and simplified inventory management, which reduces total system cost.

No Power Sequencing

I/O power-up/down management is built into ProASIC3/E devices. Reliable and predictable I/O and device behavior during power-up and power-down eliminates the need for a system power sequence device and reduces total system cost.

Low Power

ProASIC3/E Flash-based FPGAs have low static and dynamic power consumption and no power-up current spike. This allows you to use a smaller and cheaper power source, reducing total system cost, and increasing system reliability.

Clock Management

Simplify system complexity and reduce component count and cost by using Actel ProASIC3/E devices for "instant-on" derivative clock generation and distribution. The live-at-power-up clock conditioning circuitry and PLLs of the ProASIC3/E devices allow for removal of additional external clock distribution chips often used to boot SRAM FPGAs or microcontrollers during system start-up.

Single-Voltage ISP

In-system programming can be done with a single 3.3 V connection to the part. The 3.3 V V_{PUMP} voltage can be provided directly from the programmer via the ISP header and does not need to be generated on the board.

Reduced Liability and Enhanced Reliability

Secure and firm error immune ProASIC3/E Flash devices allow you to protect your designs from theft, tampering, and cloning. In addition, ProASIC3/E devices protect your systems from costly firm-error related support and litigation liability concerns.

Superior Noise-Reduced I/Os

ProASIC3/E devices support separate power and ground supplies for input and output pins. This contributes to I/O noise immunity and may help remove EMI emission.

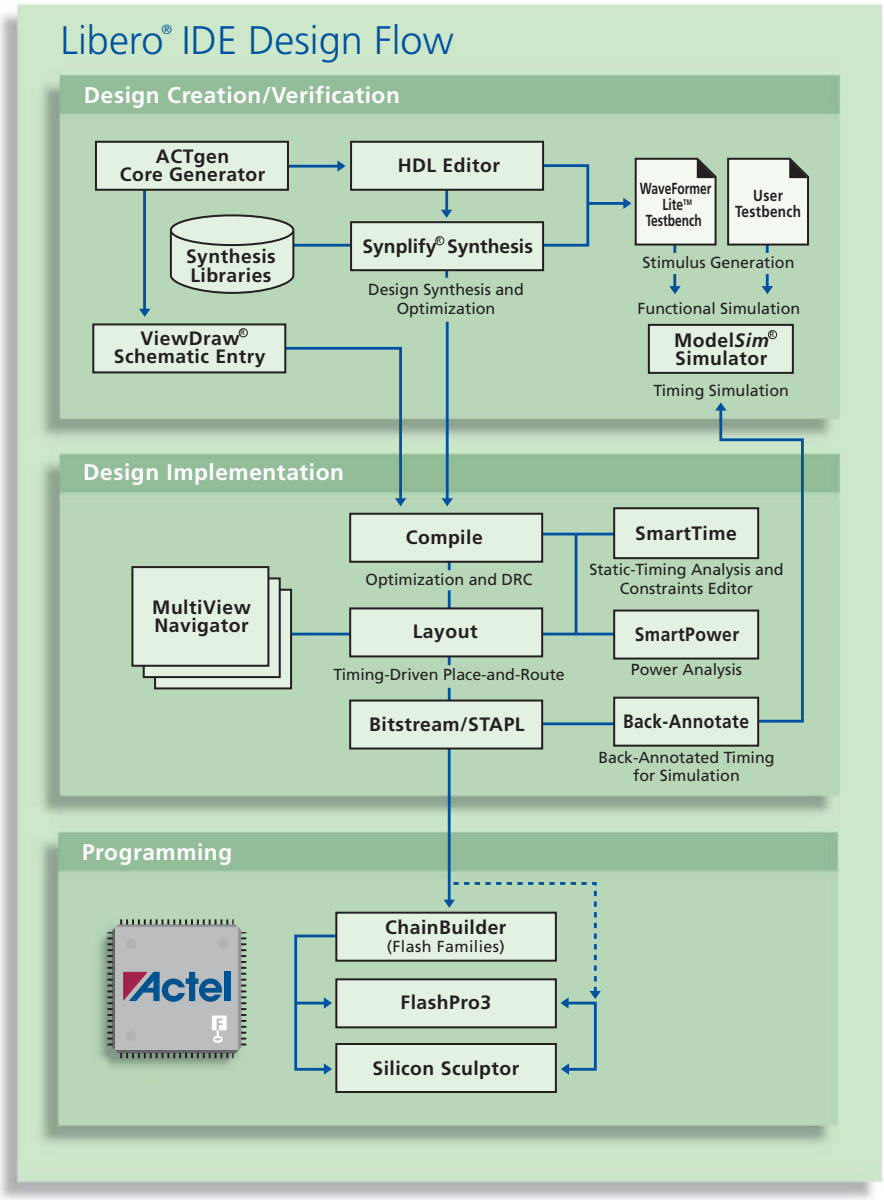
No Power-Up Monitor Chip

Unlike SRAM configuration bits, Flash configuration switches do not brownout. No voltage monitor chip is required to ensure reliable operation and clean power-up/down of the system, reducing total system cost.

Design Tools

The ProASIC3/E devices are fully supported by the Actel Libero® Integrated Design Environment (IDE) and Actel Designer software. Libero IDE, which includes Designer, is the most comprehensive FPGA design and development software available, providing start-to-finish design flow guidance and control for novice and experienced users. Libero IDE includes all necessary design tools to bring your ProASIC3/E product to market quickly with the highest possible device performance.

By combining Actel internally developed tools with EDA tools from industry leaders such as Magma Design Automation,™ Mentor Graphics,® SynaptiCAD,™ and Synplicity® into a single package, Libero IDE clearly provides a "one-stop shopping" approach. The Libero IDE integrated development environment ensures complete tool interoperability, a streamlined design flow, management of all source, design, run, and log files, and seamless passing of all design data between tools from schematic/HDL entry through synthesis, simulation, place-and-route, and device programming.



For those preferring to use their own design and verification tools, the Actel Designer software offers all of the tools needed for efficient design implementation. Designer is an interactive design implementation tool that can import designs created with Libero IDE or third-party schematic and HDL CAE tools. After completing design entry and functional verification using your preferred EDA packages, simply import a standard EDIF, VHDL, or Verilog netlist into Designer for constraints, place-and-route, timing analysis, and STAPL file or program file generation. The Actel FlashPro3 programming software is also included in Designer. Designer is compatible with the most popular design entry and verification packages from industry leaders such as Cadence,® Mentor Graphics, Synopsys,® and Synplicity.

Running on PC Microsoft® Windows,® Red Hat® Linux, and Sun Solaris™ operating systems, Libero IDE with Designer

provides three basic licensing levels, with additional flexibility at each level. The Libero IDE Silver edition, a free license product, contains all of the features except simulation and allows you to work with the A3P030, A3P060, A3P125, and A3P250 from the ProASIC3 family, and the A3PE600 from the ProASIC3E family. Libero IDE Gold contains the same features as Libero IDE Silver, plus simulation. Libero IDE Platinum edition contains all tools and allows you to work with all ProASIC3/E device sizes.

For detailed information about Libero IDE and Designer, please go to **http://www.actel.com/products/tools/sw.html**.

Programming

ProASIC3/E devices offer ISP capabilities. To program a device mounted on a system board, a programmer can simply be connected to the ISP header. The configuration data is supplied through a standard JTAG interface from a microprocessor, Silicon Sculptor II, or FlashPro3. The FlashPro3 programmer, with its small size, ease of portability, and USB programming port connections, is ideal for prototyping. FlashPro3 allows high-speed programming; even the largest ProASIC3/E parts may be programmed in less than two minutes.

FlashPro3 Programmer

By connecting several FlashPro3 programmers via USB 2.0 hubs, low-cost parallel programming is possible. The FlashPro3 programmers allow ISP of ProASIC3/E parts already board-mounted via a single ISP header. Commonly used ISP headers are provided in FlashPro3. The FlashPro software provides a simple GUI to allow parallel programming of ProASIC3 devices and serialization of the FROM.

Multiple ProASIC3/E devices, as part of a large JTAG programming chain on a single board, may be programmed via a single header using the ChainBuilder software. ChainBuilder allows standard JTAG (IEEE1152) programming of ProASIC3/E parts, one by one, automatically bypassing the non-Flash parts. ChainBuilder and the FlashPro software work together to simplify and reduce the costs of programming complex systems. The concurrent version of ChainBuilder extends this capability to allow multiple devices on the same board to be programmed at the same time.

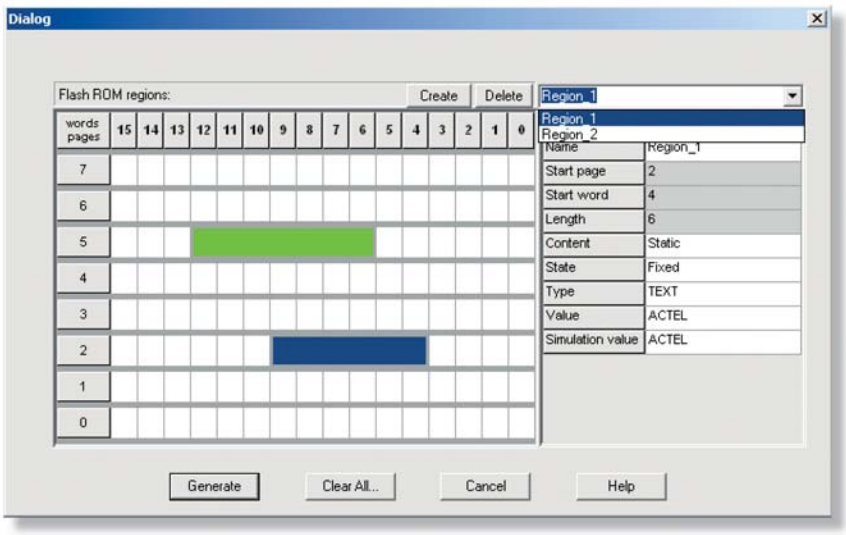
Finally, microprocessor-based ISP programming for ProASIC3/E devices is handled by Actel DirectC software, which provides a high-speed solution for low-speed microprocessors.

Starter Kit

The ProASIC3/E Starter Kit is a complete package consisting of an evaluation board with a ProASIC3/E device, Actel Libero IDE Gold, the FlashPro3 programmer with a USB cable, FlashPro software, programming cables with an ISP header, a power supply, tutorials, and support documentation. You can explore the various benefits of nonvolatile ProASIC3/E FPGAs, including ISP, device serialization, and FlashLock on-chip system security. Additionally, this kit enables you to efficiently evaluate the performance and functionality of designs for cost-sensitive, ASIC-alternative applications.

Configuring and Programming the FROM

The FROM provides designers with unprecedented flexibility in storing secure data such as device serial numbers or keys. The FROM can be configured through a simple interface. Actel provides extensive software support for programming the ProASIC3/E devices' FROM contents. Several different serialization scenarios are supported, including static value, random numbers, auto increment, and auto decrement. Methodologies that support different multi-device programming scenarios have also been provided in the tools' flow. For example, if you were programming 10,000 parts, all 10,000 may have the same FPGA (logic) programming, but each of the 10,000 parts could have unique programming for the FROM contents. Programming of the FPGA fabric and the FROM contents can be performed selectively with encrypted text or plain text.



FROM Interface

Actel IP Cores

With over 90 cores optimized for the Actel Flash-based ProASIC3/E families of devices, Actel supports the communications, consumer, military, industrial, automotive, and aerospace markets.

DirectCores are sourced, verified, supported, and maintained by Actel. They come complete as pre-implemented, synthesizable building blocks and have been thoroughly tested and verified in Actel FPGAs. They are designed and optimized for use in Actel Flash-based families of devices. DirectCores are delivered with excellent documentation and support to simplify the integration of the design.

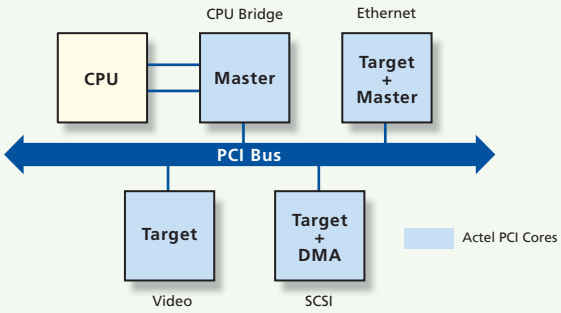
CompanionCores are sourced, verified, supported, and maintained by Actel IP partners. They are proven, prebuilt IP cores optimized for use in Actel devices. CompanionCores, like DirectCores, streamline your designs, enable faster time to market, and minimize design costs and risks.

One Company Serving All Your Design Needs

Actel DirectCores and CompanionCores provide an abundance of IP choices to complete your design. Actel IP cores allow the system designer to focus on differentiating capabilities, not recreating building blocks. Additionally, Actel IP cores are optimized for use with Actel silicon. Because Actel thoroughly verifies all IP cores, you can spend more of your time verifying the system instead of the IP component.

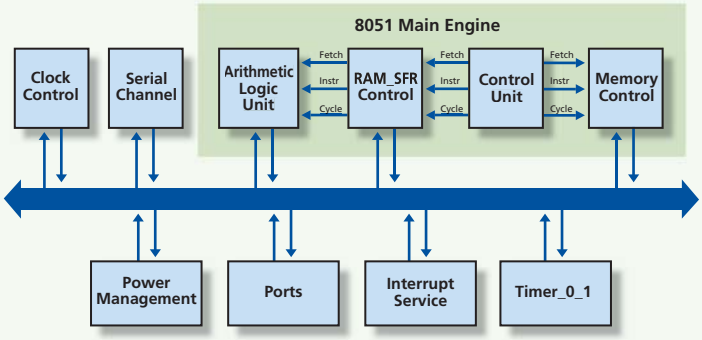
CorePCI

- PCI specification 2.3 compliant
- Zero wait-state burst mode transfers
- Silicon-proven 33 MHz or 66 MHz performance
- 32-bit or 64-bit PCI bus
- Backend support options for synchronous DRAM, SRAM, and generic I/O subsystems
- Flexible backend data flow control



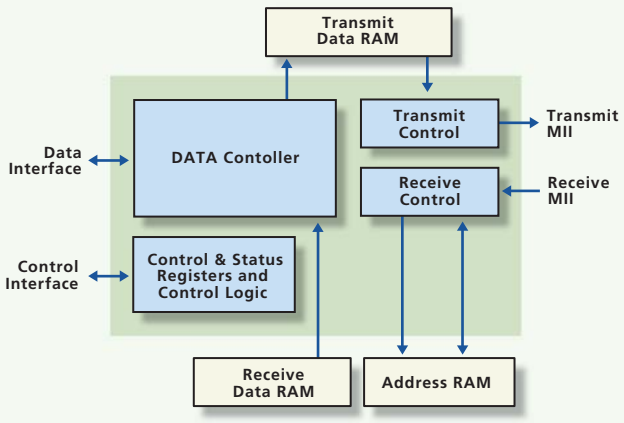
Core8051

- 100% 80C51/80C31/8051 (ASM51) instruction-compatible
- Single-cycle instruction execution
- 8-bit arithmetic logic unit
- Four 8-bit programmable input/output ports
- One programmable serial port
- Two 16-bit timer/counters
- Four priority-level interrupt controllers
- 256-byte internal data memory interface
- 64-kilobyte external program and data memory interfaces



Core10/100

- Ethernet media access controller
- Data controller has a built-in DMA engine with selectable 8-, 16-, or 32-bit data-bus width
- Supports 10/100 Mbps half/full-duplex operations
- Supports CSMA/CD defined by IEEE 802.3 standard



ProASIC 3/E Product Table

ProASIC3/E ARM-Enabled ProASIC3/E		A3P030	A3P060	A3P125	A3P250 M7A3P250	A3P400 M7A3P400	A3P600 M7A3P600	A3P1000 M7A3P1000	A3PE600 M7A3PE600	A3PE1500 M7A3PE1500	A3PE3000 M7A3PE3000
System Gates		30 k	60 k	125 k	250 k	400 k	600 k	1 M	600 k	1.5 M	3 M
VersaTiles (D-Flip-Flop)		768	1,536	3,072	6,144	9,216	13,824	24,576	13,824	38,400	75,264
RAM kbits (1,024 bits)		–	18	36	36	54	108	144	108	270	504
4,608-Bit Blocks		–	4	8	8	12	24	32	24	60	112
FlashROM (FROM)		1 k	1 k	1 k	1 k	1 k	1 k	1 k	1 k	1 k	1 k
Secure (AES) ISP		No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PLLs		–	1	1	1	1	1	1	6	6	6
VersaNet Globals		6	18	18	18	18	18	18	18	18	18
I/O Standards		Std. & Hot Swap	Std.+	Std.+	Std.+/ Advanced	Std.+/ Advanced	Std.+/ Advanced	Std.+/ Advanced	Pro	Pro	Pro
I/O Banks (+ JTAG)		2	2	2	4	4	4	4	8	8	8
Single-Ended I/O / Differential I/O Pairs[1]	**QN132**	81									
	VQ100	79	71	71	68/13						
	FG144		96	97	97/24	97/25	97/24	97/25			
	TQ144		91	100							
	PQ208			133	151/34	151/34	154/35	154/35	147/65	147/65	147/65
	FG256				157/38[2]	178/38	179/45	177/44	165/79		
	FG484					194/38	227/56	300/74	270/135	280/136	280/136
	FG676									439/209	
	FG896										616/300

[1] *Advanced information subject to change.* [2] *This is not supported on the M7A3P250 device.*

For more information regarding **ProASIC3/E Flash FPGA families**, please visit the Actel website at **www.actel.com** or contact your local sales representative.

Actel®
www.actel.com

Actel Corporation
2061 Stierlin Court
Mountain View, CA
94043-4655 USA
Phone 650.318.4200
Fax 650.318.4600

Actel Europe Ltd.
Dunlop House, Riverside Way
Camberley, Surrey GU15 3YL
United Kingdom
Phone +44 (0) 1276 401 450
Fax +44 (0) 1276 401 490

Actel Japan
www.jp.actel.com
EXOS Ebisu Building 4F
1-24-14 Ebisu Shibuya-ku
Tokyo 150, Japan
Phone +81.03.3445.7671
Fax +81.03.3445.7668

Actel Hong Kong
www.actel.com.cn
Suite 2114, Two Pacific Place
88 Queensway, Admiralty
Hong Kong
Phone +852 2185 6460
Fax +852 2185 6488

ONECHIP is all you need

© 2005 Actel Corporation. All rights reserved. The Actel name and logo are trademarks of Actel Corporation. All other trademarks and service marks are the property of their respective owners. 55700003-6/4.06