Key Benefits

- Specialized Low Power Modes for Portable Applications
- No Additional Power Management Circuitry Needed
- No Inrush Current Spikes at Power-Up for Configuration
- Real-Time Power Optimization with Actel SmartPower Analysis Tool

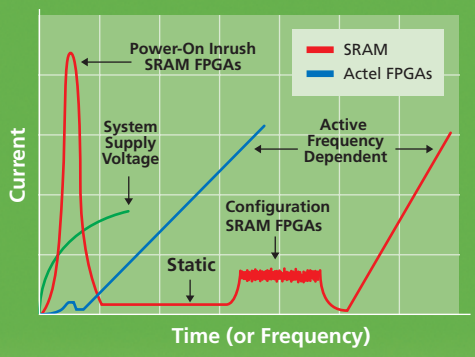


Figure 1: Comparison of SRAM FPGA Power Profiles with Antifuse and Flash FPGAs

Total System Power

UNDERSTANDING THE POWER PROFILE OF FPGAs

Although often promoted as ASIC alternatives, not all FPGA technologies offer the complete feature set available with ASICs. Of the three primary FPGA technologies, only Flash and antifuse have power characteristics similar to those of an ASIC. When selecting FPGAs, design engineers often focus on standby and dynamic power, frequently neglecting to take the entire power profile of the programmable logic solution into account. The various FPGA core technologies have significantly different power profiles, and these differences in power can have a profound impact on the overall system design and power budget.

The Power Profile

The power profile of an FPGA is determined by the base technology of the interconnect element used. Two of the base technologies, antifuse and Flash, possess traditional power profiles. The third technology, SRAM, has a unique profile that is not as well understood and has not been well documented in the past.

Nonvolatile, reprogrammable Flash FPGAs use a single Flash cell to form their efficient interconnect. SRAM FPGAs utilize a six-transistor SRAM cell to perform the interconnection between routing lines and logic cells, resulting in higher static and dynamic power.

Antifuse FPGAs offer the lowest power consumption and highest performance of any of the FPGA technologies. Once programmed, the antifuse metal-to-metal interconnect delivers low-impedance connections with less than 1 fF capacitance and typically less than 50 Ω of resistance.

When evaluating the respective programmable technologies, there are four components to the FPGA power profile that must be considered: inrush current, configuration current, static power, and dynamic power. Unlike SRAM FPGAs, Flash and antifuse FPGAs have no power-up or configuration power components.

Actel "devices are live at power-up, highly secure, and require no separate configuration memory, all characteristics shared by ASICs."

"Programmable Logic Fills the Bill for Portable Applications"

Richard Nass,
Editor-in-Chief,
Portable Design™

Inrush Current

SRAM FPGAs typically power up in an unconfigured state. Until the device completes the initial power-up and reset sequence, the various configuration bits are in unknown states. As these bits are reinitialized each time power is cycled, a current surge is created that may generate a spike as high as several Amps. This event may also last as long as a few hundred microseconds—all during the time the power supply is ramping up and the rest of the system is attempting to power up.

This inrush current is often the largest single contributor to the SRAM power profile. Furthermore, this phenomenon can force system designers to oversize power supplies and add extra circuitry for power-up sequencing to avoid brownouts and erratic system start-up behavior.

Configuration Current

After an SRAM FPGA has completed its initial power-up and reset, it must also be configured. During configuration, a bitstream is downloaded to the device and the various configuration bits are programmed. This configuration programming can often consume more than a 100 mA and last for hundreds of milliseconds.

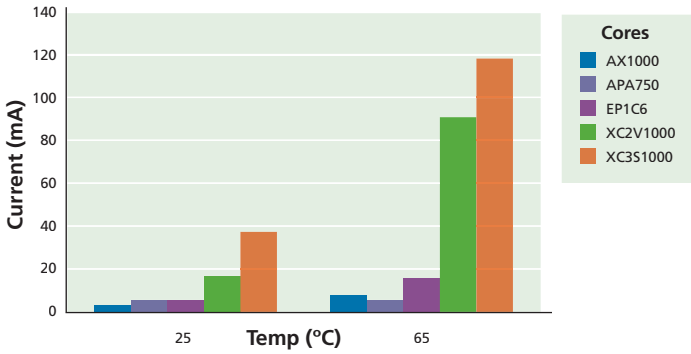
This configuration current can prove especially lethal to battery-based supplies, where constant loads are desirable to maximize battery life. This operating characteristic of SRAM FPGAs generally makes them poorly suited for portable applications where battery life is a concern.

Figure 2: Actual SRAM FPGA Inrush Current

Static Power

Static power is the minimum power required to maintain a device in user mode while the I/Os and logic cells are not switching. SRAM-based FPGAs consume significantly more static power than do their Flash and antifuse counterparts. At room temperature this difference may only be tens of milliamps; at higher operating temperatures this difference can exceed 100 mA. This higher current draw would drastically impact the operating life of any battery-supplied system.

Figure 3: Comparison of Static Current Between SRAM, Flash, and Antifuse FPGAs



Dynamic Power

The last component of the FPGA power profile is dynamic power—the power consumed when both the I/Os and logic cells are switching. Dynamic power is a function of the switching frequency and operating temperature. All FPGA technologies exhibit similar dynamic power performance.

Flash and Antifuse FPGA Power Profiles

The power profiles of both antifuse and Flash-based FPGAs more closely resemble those of ASICs and ASSPs than SRAM FPGAs. The power profile for these types of devices is composed of only two significant components: static and dynamic power.

As Flash and antifuse FPGAs are nonvolatile, the core cells enter a defined state immediately at power-up so there is minimal power-up switching required. Therefore, they do not suffer the severe inrush current spike that affects SRAM FPGAs.

Moreover, both Flash and antifuse FPGAs are live at power-up. They retain their programming information once they have been configured, even after power down. As a result, there is no configuration cycle during power-up that can consume tens of additional milliamps.

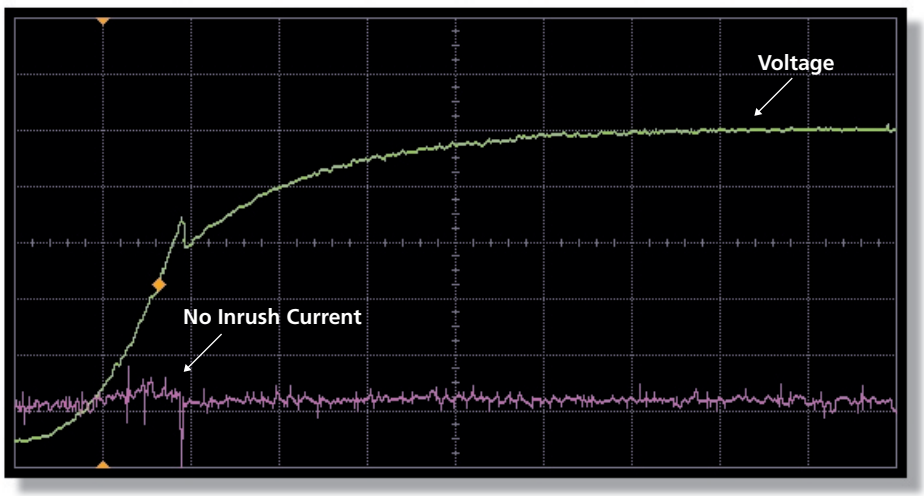


Figure 4: Actual Flash FPGA Power Profile

Total System Power

In addition to the high inrush and configuration currents of SRAM FPGAs, there are additional power components to consider. Unlike Flash and antifuse FPGAs, SRAM FPGAs are not single-chip. They require additional support devices to function properly. In addition to the on-board memory devices needed to store the configuration bitstreams, frequently a CPLD is needed to act as a configuration controller. Often additional circuitry is required to trap brownouts and power glitches in order to properly reset and reconfigure the FGPA. Besides the added board space and cost of these components, each adds to the overall power profile of the SRAM FPGA solution and makes system power-up more complex.

All FPGA solutions from Actel are single-chip and do not require any external components to operate. This aspect not only leads to reduced power consumption but also to a smaller overall footprint.

Summary

FPGA technologies differ widely in their power consumption characteristics. Both Flash and antifuse FPGAs are true live-at-power-up technologies that do not exhibit large inrush current spikes at power-up. Moreover, as both Actel FPGA technologies are nonvolatile, they do not suffer from the high configuration current needed during each power cycle.

SRAM-based FPGAs require additional components to create a complete solution, in contrast to the single-chip solutions offered by Actel. This additional design complexity adds to the complexity of the SRAM FPGA power profile.

The nature of the SRAM FPGA power profile can force system designers to unnecessarily oversize system power supplies and complicate the overall design. Actel FPGAs exhibit a power profile similar to that of ASICs and ASSPs, greatly reducing the demand on power supplies and simplifying the designer's task.

For more information regarding the **Power Profile of Actel FPGAs**, please contact your local **Actel** sales representative.

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