Power-Up/Down Behavior of ProASIC3/E Devices

Introduction

Actel ProASIC3/E devices are Flash-based FPGAs manufactured on a 0.13 µm process node. ProASIC3/E FPGAs offer a single-chip, reprogrammable solution and support Level 0 live at power-up (LAPU) due to their nonvolatile architecture.

Three main voltage pins are used by ProASIC3/E devices during normal operation:[1]

- V_{CC}: Voltage supply to the FPGA core
- V_{CCI}BX: Supply voltage to the bank's I/O output buffers and I/O logic. BX is the I/O bank number.
- VMVX: Quiet supply voltage to the input buffers of each I/O bank. X is the bank number.

The I/O bank VMV pin must be tied to the V_{CCI} pin of the same bank. Therefore, the supplies that need to be powered up/down during normal operation are V_{CC} and V_{CCI}. These power supplies can be powered up/down in any sequence during normal operation of ProASIC3/E FPGAs. During power-up, I/Os in each bank will remain tristated until the last supply (being either V_{CCI}BX or V_{CC}) reaches its functional activation voltage. Similarly, during power-down, I/Os of each bank are tristated once the first supply reaches its brownout deactivation voltage.

ProASIC3/E devices exhibit very low transient current on each power supply during power-up. The peak value of the transient current depends on the device size, temperature, voltage levels, and power-up sequence.

ProASIC3/E device inputs can be driven while the device is not powered. The driven I/Os do not pull up power planes, and the current draw is limited to very small leakage current. Therefore, ProASIC3/E FPGAs are suitable for applications in which cold sparing is required. All ProASIC3E devices and A3P030 device in ProASIC3 family are also designed to be compatible with hot-swap applications.[2]

Transient Current

The source of transient current, also known as inrush current, varies depending on the FPGA technology. Due to their volatile technology, the internal registers in SRAM FPGAs must be initialized before configuration can start. This initialization is the source of significant inrush current in SRAM FPGAs during power-up. Due to the nonvolatile nature of Flash technology, ProASIC3/E devices do not require any initialization at power-up, and there is very little or no crossbar current through PMOS and NMOS devices. Therefore, the transient current at power-up is significantly less than SRAM FPGAs. Figure 1 on page 2 illustrates the types of power consumption by SRAM FPGAs vs. Actel's Antifuse and Flash FPGAs.

1. *For more information on ProASIC3/E device voltage supplies, refer to the appropriate datasheet located at http://www.actel.com/techdocs/ds.*
2. *For more details on the levels of hot-swap compatibility in ProASCI3/E devices, refer to ProASCI3 and ProASIC3E datasheets located at http://www.actel.com/techdocs/ds.*

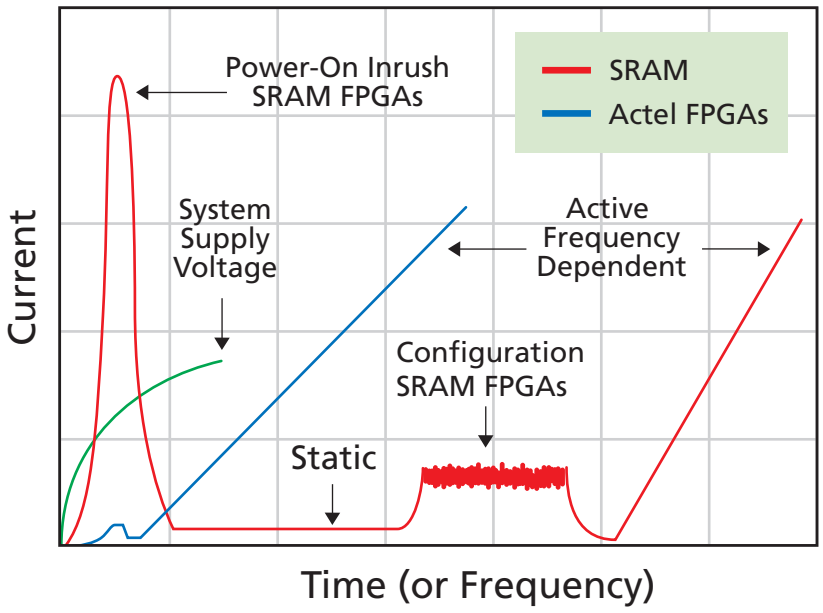

Figure 1 • **Types of Power Consumption in SRAM FPGAs and Actel Nonvolatile FPGAs**

Transient Current on V_{CC}[3]

The preliminary characterization of the transient current on V_{CC} has been performed on A3PE600-PQ208 EAS devices. The transient current measurements are performed on two A3PE600-PQ208 EAS parts while all the device I/Os were internally pulled down. The preliminary measurements at typical conditions show that the maximum transient current on V_{CC}, when the power supply is powered at ramp rates ranging from 15 V/ms to 0.15 V/ms, does not exceed the maximum standby current specified in the device datasheets. Refer to the *ProASIC3 Flash Family FPGAs* and the *ProASIC3E Flash Family FPGAs* datasheets for more information.

Transient Current on V_{CCI}[3]

The preliminary characterization of the transient current on V_{CCI} has been performed on A3PE600-PQ208 EAS devices similar to V_{CC} transient current measurements. The preliminary measurements at typical condition show that the maximum transient current on V_{CCI}, when the power supply is powered at ramp rates ranging from 33 V/ms to 0.33 V/ms, does not exceed the maximum standby current specified in the device datasheet. Refer to the *ProASIC3 Flash Family FPGAs* and the *ProASIC3E Flash Family FPGAs* datasheets for more information.

I/O Behavior at Power-Up/Down

This section discusses the behavior of device I/Os, used and unused, during power-up/down of V_{CC} and V_{CCI}. As mentioned earlier, VMVX and V_{CCI}BX are tied together and therefore inputs and outputs are powered up/down at the same time.

3. *The "Transient Current on V_{CC}" section will be updated after the full characterization of ProASIC3/E has been completed.*

I/O State during Power-Up/Down

This section discusses the characteristics of I/O behavior during device power-up and power-down. Before the start of power-up, all I/Os are in tristate mode. The I/Os will remain tristated during power-up until the last voltage supply (V_{CC} or V_{CCI}) is powered to its functional level (power supply functional levels are discussed in the "Power-Up to Functional Time" section on page 4). After the last supply reaches the functional level, the outputs will exit the tristate mode and drive the logic at the input of the output buffer. Similarly, the input buffers will pass the external logic into the FPGA fabric once the last supply reaches the functional level. The behavior of user I/Os is independent of the V_{CC} and V_{CCI} sequence or the state of other voltage supplies of the FPGA (V_{PUMP} and V_{JTAG}). Figure 2 shows the output buffer behavior during power-up with 10 kΩ external pull down. In Figure 2, V_{CC} is powered first, and V_{CCI} is powered 5 ms after V_{CC}. Figure 3 shows the state of the I/O when V_{CCI} is powered about 5 ms before V_{CC}. In the circuitry shown in Figure 3, the output is externally pulled down.

During power-down, device I/Os become tristated once the first power supply (V_{CC} or V_{CCI}) drops below its brownout voltage level. The I/O behavior during power-down is also independent of voltage supply sequencing.

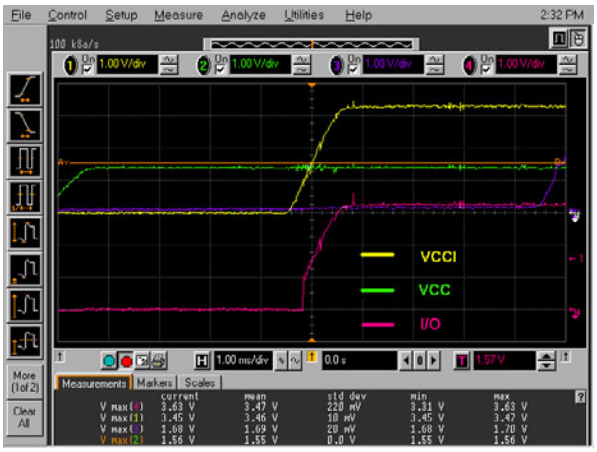

Figure 2 • **I/O State When V_{CC} is Powered before V_{CCI}**

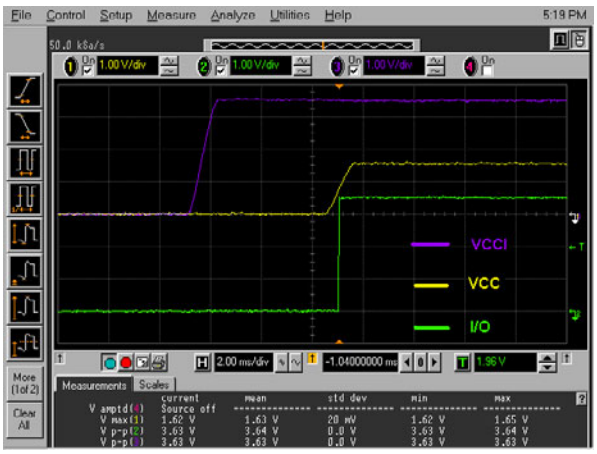

Figure 3 • **I/O State When V_{CCI} is Powered before V_{CC}**

Power-Up to Functional Time

At power-up, device I/Os exit the tristate mode and become functional once the last voltage supply in the power-up sequence (V_{CCI} or V_{CC}) reaches its functional activation level. Typical I/O behavior during power-up to functional time is illustrated in Figure 2 and Figure 3 on page 3.

The functional level of the voltage supplies at power-up is designed to be 0.85 V+/-0.25 V for V_{CC} and 0.9 V+/-0.3 V for V_{CCI} supply. Once the last voltage supply in the power-up sequence exceeds its functional level, the device I/Os will transition into a functional state. Therefore, the power-up to functional time is the time that it takes for the last supply to power-up from zero to its functional level. However, the functional level of the power supply during power-up may vary slightly within the specification in different ramp rates.

ProASIC3/E devices meet Level 0 LAPU, i.e., can be functional prior to V_{CC} reaching the regulated voltage required. This important advantage distinguishes ProASIC3/E Flash devices from their SRAM-based counter parts. SRAM-based FPGAs, due to their volatile technology, require hundreds of milliseconds after power-up to configure the design bitstream before they become functional. Refer to Figure 4 for more information.

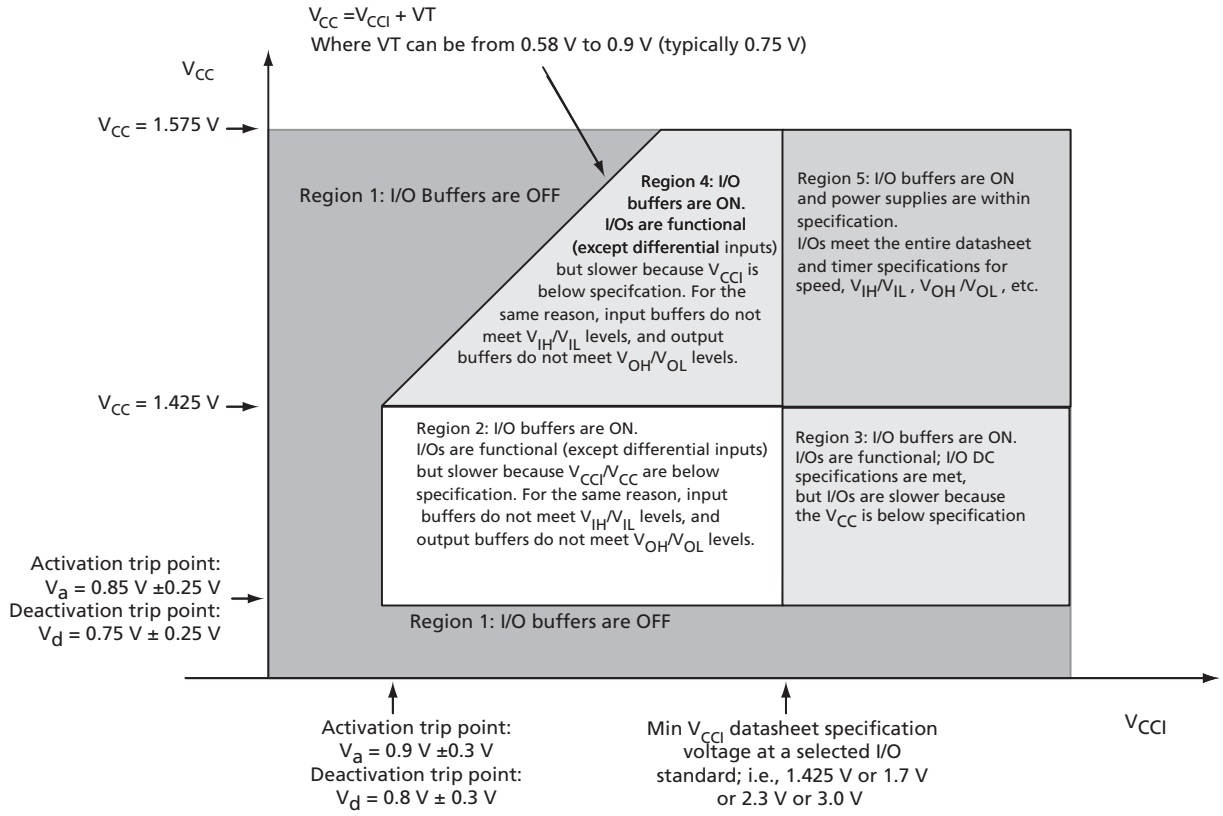

Figure 4 • **I/O State as a Function of V_{CCI} and V_{CC} Voltage Levels**

Brownout Voltage

Brownout is a condition in which the voltage supplies are lower than normal, causing the device to malfunction as a result of insufficient power. In general, Actel does not guarantee the functionality of the design inside ProASIC3/E devices, if voltage supplies are below their minimum recommended operating condition. Actel has performed measurements to characterize the brownout levels of FPGA power supplies. The brownout levels of the power supplies for ProASIC3/E devices are designed to be 0.75 V+/-0.25 V for V_{CC} and 0.8 V+/-0.3 V for V_{CCI}. For the purpose of characterization, a direct path from the device input to output is monitored while voltage supplies are lowered gradually. The brownout point is defined as the voltage level in which the output stops following the input. Characterization tests performed on two A3PE600-PQ208 EAS devices in typical operating conditions showed the brownout voltage levels to be within the specification.

During device power-down, the device I/Os become tristated once the first supply in the power-down sequence drops below its brownout deactivation voltage.

Internal Pull Up and Pull Down

ProASIC3/E device I/Os are equipped with internal weak pull-up/down resistors that can be used by designers. If used, these internal pull-up/down resistors will be activated during power-up, once both V_{CC} and V_{CCI} are passed their functional activation level. Similarly, during power-down these internal pull-up/down resistors will turn off once the first supply voltage falls below its brownout deactivation level.

Cold Sparing

In cold-sparing applications, voltage can be applied to device I/Os before and during power-up. Cold-sparing applications rely on three important characteristics of the device:

1. I/Os must be tristated before and during power-up.
2. Voltage applied to the I/Os must not power-up any part of device.
3. Device reliability must not be compromised if voltage is applied to I/Os before or during power-up.

As described in the "Power-Up to Functional Time" section on page 4, ProASIC3/E I/Os are tristated before and during power-up until the last voltage supply (V_{CC} or V_{CCI}) is powered up past its functional level. Furthermore, applying voltage to the ProASIC3/E I/Os does not pull up V_{CC} or V_{CCI} and therefore does not partially power-up the device. Table 1 includes the cold-sparing test results on A3PE600-PQ208 EAS devices. In this test, leakage current on the device I/O and residual voltage on the power supply rails were measured while voltage was applied to the I/O before power-up.

Table 1 • **Cold-Sparing Test Results for A3PE600 Devices**

Device I/O	Residual Voltage (V)		Leakage Current
	V_{CC}	V_{CCI}	
Input	0	0.003	<1 uA
Output	0	0.003	<1 uA

The reliability of ProASIC3/E I/Os is guaranteed if the voltage level, applied to the device I/Os, is less than 3.6 V, as specified in the product datasheets. Therefore, ProASIC3/E devices meet all three requirements stated earlier in this section and are suitable for cold-sparing applications.

Hot Swap

Hot swapping is the operation of hot insertion or hot removal of a card in (or from) a powered-up system. The I/Os need to be configured in hot insertion mode if hot swapping compliance is required. All ProASIC3E devices support hot swapping, and the only ProASIC3 device supporting hot swapping is the A3P030. Refer to the *ProASIC3 Flash Family FPGAs* and the *ProASIC3E Flash Family FPGAs* datasheets for more information about hot-swap capabilities of ProASIC3/E devices.

Conclusion

Actel's ProASIC3/E Flash FPGAs provide an excellent programmable logic solution for a broad range of applications. In addition to high performance, low cost, security, nonvolatility, and single chip, they are live at power-up (meet Level 0 of the LAPU classification) and offer clear and easy-to-use power-up/down characteristics. Unlike SRAM FPGAs, ProASIC3/E devices do not require any specific power-up/down sequencing and have extremely low power-up inrush current in any power-up sequence. ProASIC3/E FPGAs also support both cold sparing and hot swapping for applications requiring these capabilities.

Related Documents

ProASIC3 Flash Family FPGAs

http://www.actel.com/documents/PA3_DS.pdf

ProASIC3E Flash Family FPGAs

http://www.actel.com/documents/PA3E_DS.pdf

www.actel.com

Actel Corporation

2061 Stierlin Court
Mountain View, CA
94043-4655 USA
Phone 650.318.4200
Fax 650.318.4600

Actel Europe Ltd.

Dunlop House, Riverside Way
Camberley, Surrey GU15 3YL
United Kingdom
Phone +44 (0) 1276 401 450
Fax +44 (0) 1276 401 490

Actel Japan
www.jp.actel.com

EXOS Ebisu Bldg. 4F
1-24-14 Ebisu Shibuya-ku
Tokyo 150 Japan
Phone +81.03.3445.7671
Fax +81.03.3445.7668

Actel Hong Kong
www.actel.com.cn

Suite 2114, Two Pacific Place
88 Queensway, Admiralty
Hong Kong
Phone +852 2185 6460
Fax +852 2185 6488

51900097-0/6.05