A DIVISION OF CIRRUS LOGIC

CRD4923

Reference Design for CS4923

Features

- Demonstrates suggested connection topology for CS4923 & CS4226 Dolby AC3 Decoding solution
- Optical or RCA IEC61937 SPDIF reception capability for direct connection to a DVD
- Stereo Analog Inputs
- 6 channel output including Right, Left, Right Surround, Left Surround, Center, and Low Frequency Effect (LFE or Subwoofer) channels
- All necessary clocking provided
- Control from parallel port or “in system” during development

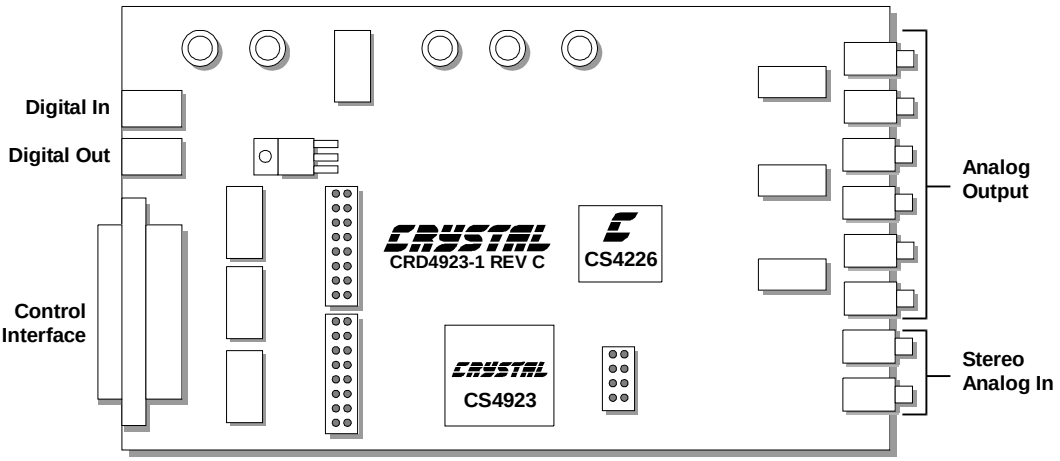
Description

The CRD4923 is a complete AC3 solution which takes optical SPDIF AC3 encoded digital data and outputs 6 channels of audio representing left, right, left surround, right surround, center and a low frequency effects (subwoofer) channel. This board can also take an analog input and do Dolby ProLogic decode and output 4 channels of audio representing left, right, center, and surround. Finally the CRD4923 can also take an analog input, apply stereo effects processing, and output a stereo pair with effects. This board is targeted as a system solution for home theater decoders.

The CRD4923 incorporates the CS4923 AC3 Multi Channel Audio Decoder and the CS4226 Surround Sound CODEC. The CS4923 provides all digital signal processing (DSP) of the system while the CS4226 takes care of all conversion requirements between the analog and digital domain. The CRD4923 demonstrates the recommended connection topology between the CS4923 and the CS4226 to ensure proper system operation.

ORDERING INFO

CRD4923



Preliminary Product Information | This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

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OPERATION

The CRD4923 includes the CS4923 AC3 Multi Channel Audio Decoder which handles all digital processing and the CS4226 Surround Sound CODEC which handles IEC61937 SPDIF reception, stereo differential analog to digital conversion, and six channel digital to analog conversion. The inputs to the board include one optical TOSLINK connector and one RCA connector for digital reception of compressed AC3 data in IEC61937 format and two RCA jacks for analog stereo input. The outputs to the board include six Analog outputs representing left, right, left surround, right surround, center and a low frequency effects (subwoofer) channel. There is also an optical transmitter connected to the S/PDIF transmitter on the CS4923.

Dolby Considerations

It should be noted by the system designer that additional circuitry may be required to obtain Dolby Certification, depending on the end product and what group of Dolby certification is desired. The designer should consult the Dolby Licensee Information Manual and contact Dolby Laboratories to determine exactly what is required to meet Dolby specifications for his/her system.

Power Requirements

The CRD4923 requires a +5 V input on J1 and digital ground on J2 for the digital side of the board. A +12 V input on J16, -12V input on J18 and analog ground on J17 are needed for the analog side of the board. The 5 V input feeds an on board regulator, U1, which provides the 3.3 V supply needed by the CS4923 and its interface components. The +5 V input also gives the CS4226, PC interface components, and the digital input and output components their power. The ±12 V are the power rails for the op amps used for the input and output buffers. Figure 7 shows the power portion of the schematic.

Digital Signal Processor and Codec

Control

Control of the CS4923 and the CS4226 can be handled in one of two ways. The system is shipped with a parallel computer cable and can be operated with accompanying software over any personal computer running with a Windows or DOS based operating system with a standard parallel port. Conversely the board can be operated “in system” by disabling the parallel interface and wire wrapping from an external microprocessor to the provided stake header J19. The parallel interface is disabled by tristating buffer U5 with jumper J20.

The system is wired to use the SPI interface mode for both the CS4226 and the CS4923. The chips share a common serial clock and control data input with a 74VHC244 translating the signals to 3.3 V for the CS4923. Each part receives an independent chip select and the board uses separate control data outputs for each part. The CS4923 additionally has an interrupt request used for requesting attention from a host when it ahs data to be read. Figures 1&2 shows the DSP & CODEC schematic and the control interface respectively.

Clocking Architecture & Digital I/O

The CRD4923 demonstrates the suggested clocking architecture that will work correctly with the hardware configurations utilized by the AC3 microcode. Figure 3 shows both the Digital I/O & the Clock Divider schematic. The onboard 49.152 MHz clock provides the DSP with it’s necessary clock input. The CLKSEL pin of the CS4923 is pulled high so that this clock will bypass the internal PLL and drive the DSP directly. The 49.152 MHz clock is also divided by 4 by U6 to provide a 12.288 MHz clock input for the CS4226.

In all modes the CS4226 masters MCLK. The CS4923 takes the MCLK as an input, divides this clock internally, and drives the LRCLK and SCLK so as to minimize level conversion buffers. This

LRCLK and SCLK are used as inputs to both the CS4226 and the CS4923's compressed data input port and digital audio input port. In this way all clocks for digital I/O between the chips are synchronized so that no buffer problems can occur. In all modes the data is passed in an I2S compatible format with 24 bits out of the CS4226 and into the CS4923 and 20 bits out of the CS4923 and into the CS4226.

When the system is configured for AC3 operation, the CS4226 receives the IEC61937 AC3 stream from J6, the digital optical connector or J22, the digital RCA connector. It recovers the clock from this stream, locks to it with the PLL and produces a 256 Fs clock on the CLKOUT which is used as MCLK for the entire system . In this way the entire digital I/O is slaved to the SPDIF stream so that no buffer problems will exist between the CS4226, the CS4923, and the incoming stream.

While operating in a PCM pass through mode, or PCM pass through with ProLogic decode mode, the CS4226 is configured by software to run off a divided down version of the on-board oscillator. The 49.152 MHz is divided by four with 2 D flip flops to give the 12.288 MHz clock input of the CS4226. The CS4226 CLKOUT then provides a 256 Fs clock for the system MCLK. The system sampling frequency is 48 kHz.

All data in the system passes through the CS4226 for data conversion into the digital I2C format, then into the CS4923 for digital signal processing, and then back to the CS4226 for conversion into the analog domain. The digital data lines from the CS4226 to the CS4923 are buffered from 5V down to 3.3 V through U4. SDATA1 contains data from the digital receiver and is routed to the compressed data input port of the CS4923 after being level shifted down to 3.3 V by U4. SDATA2 contains data from the analog to digital converter and is routed to the digital audio input port of the CS4923 after being level shifted down to 3.3 V by U4.

Input and Output

Digital Input and Output

Digital I/O is provided on board with two TOSLINK optical connectors and one RCA connector. S/PDIF digital input is handled in optical format by J6 and in electrical format by J22. The jumper J21 can be used to select (O)ptical input or (R)CA input. This stream is then routed to the CS4226's SPDIF receiver. The CS4923 SPDIF output is routed to the TOSLINK transmitter, J7, to provide an optical output..

Analog Input and Output

The CRD4923 has the capability to take a single ended stereo analog pair in. The single ended input is converted into a differential pair and routed to the CS4226. Input levels should not exceed 2 Vrms. The first stage of the input filter (U8A and U11B) provides a gain of ½. The second stage (U8B and U11A) provides unity inversion. The result is a 2 Vrms differential signal that is AC coupled with the CS4226 differential input Figure 5 shows the Analog Input Circuitry.

The six outputs from the CS4226 are routed to six output buffers which provide a non-inverting 2-pole filter with a gain of two. The six signals represent left, right, left surround, right surround, center, and a low frequency effects (LFE) channel. The output signals coming from the board are 2 Vrms. Figure 6 shows the analog output circuitry.

Analog Relay Control

To prevent pops on power up and power down, relays are on all six output channels. These relays are controlled with the power on/off circuitry shown in Figure 4. The common mode out (CMOUT) of the CS4226 controls the relays at power up. The relays will not turn on until the DACs have been calibrated and the common mode has risen. This prevents any popping on power up. The signal RELAY_CTRL comes from the power failure out-

put (PFO) indicator of the Maxim 708 part. The power failure indicator input (PFI) tracks the level of the 5 volt supply. When this signal (PFI) falls more than ½ volt below 5 volts the output (PFO) falls low, cutting off the relays. The reset line is also tied into the relay control so that the relays will open when reset is low.

Headers and Jumpers

Power

Table 1 shows the connections necessary for operation of the CRD4923.

Section	Jumper	Voltage (volts)
Digital	J1	+5
Digital	J2	Ground
Analog	J16	+12
Analog	J17	Ground
Analog	J18	-12

Table 1. CRD4923 Connections

Control

Two stake headers are provided to enable the user to control the system from an external microprocessor. J20 enables and disables the onboard control by tristating the parallel port control buffer U5. When U5 is tristated all control signals for the board can be accessed on J19. Figure 2 shows a diagram of the signals available on J19. These signals can all be 5 volt as they are buffered by U4 before being routed to the CS4923.

Digital I/O

The TOSLINK connector J6 provides an optical input for IEC61937 S/PDIF reception on the board. The RCA jack J22 provides an electrical IEC61937 SPDIF input. Jumper J21 can be used to select either the (R)CA signal from J22 or the (O)ptical signal from J6 to be routed to the receiver on the CS4226.

The TOSLINK connector J7 provides an optical output from the digital transmitter on the CS4923.

Analog I/O

Table 2 shows input signal and table 3 shows output signals for the board. All analog signals are 2 Vrms for input and output.

Signal Name	Connector
Left Input	J8
Right Input	J12

Table 2. Analog Input Signals

Signal Name	Connector
Left	J15
Right	J14
Left Surround	J10
Right Surround	J9
Center	J13
Subwoofer	J11

Table 3. Analog Output Signals

Debugger

Jumper J4 provides access to the CS4923 debugger. This jumper should be considered for factory use only

Memory

J3 is a stake header providing access to all signals needed for an external memory interface to the CS4923. A memory module for autoboot or for DTS capability will be available in Q1 1998.

Schematics & Layout

The schematics in Figures 1 thru 7 show the entire circuit for the CRD4923. Figures 8 thru 13 show the layout files used to produce the board.

Bill of Materials

The bill of materials at the end of this document shows the specific parts ordered for this design and the associated manufacturer. Most parts may be substituted as long as tolerances and voltage levels are adhered to.

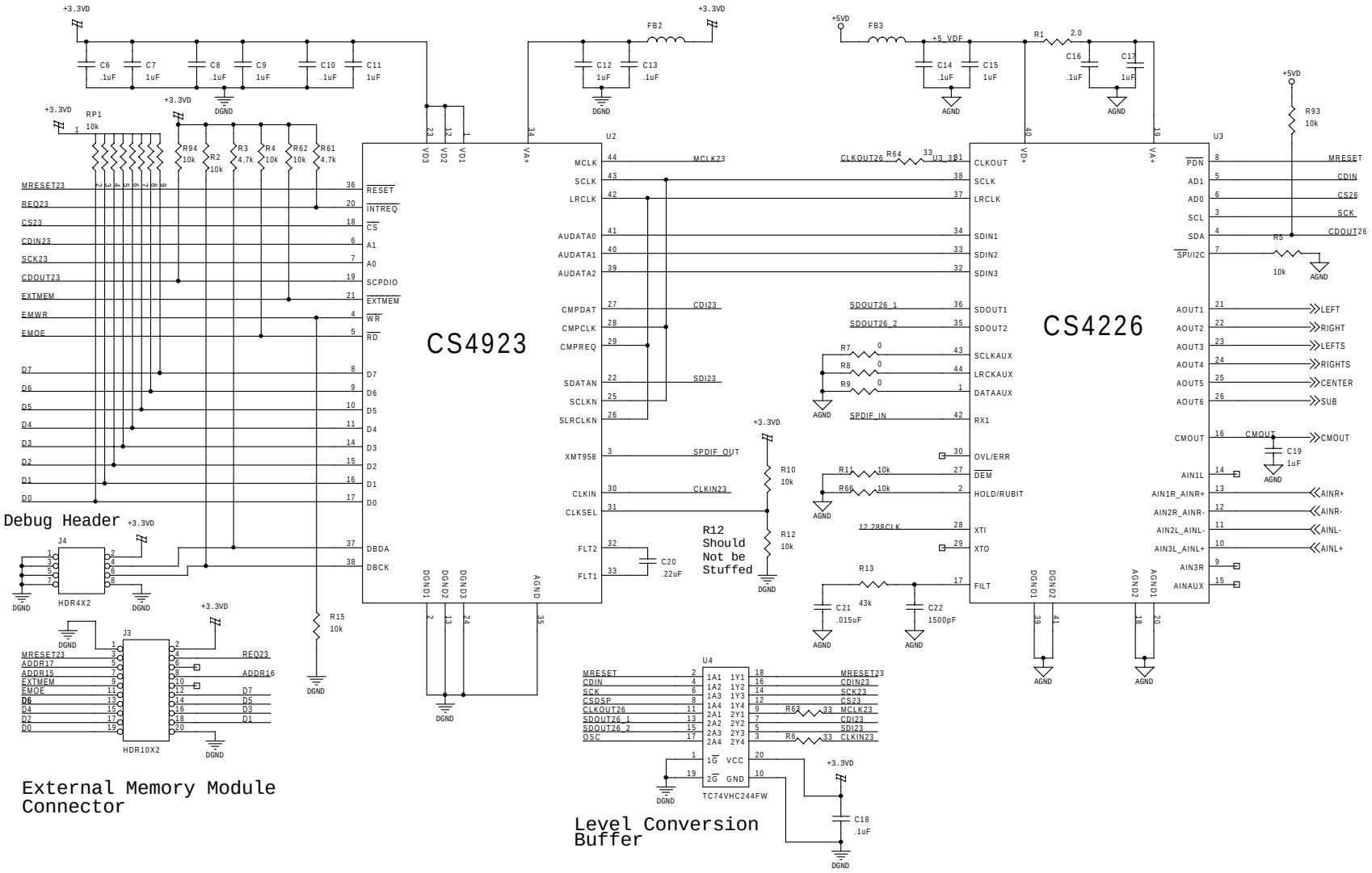

Figure 1. DSP and Codec

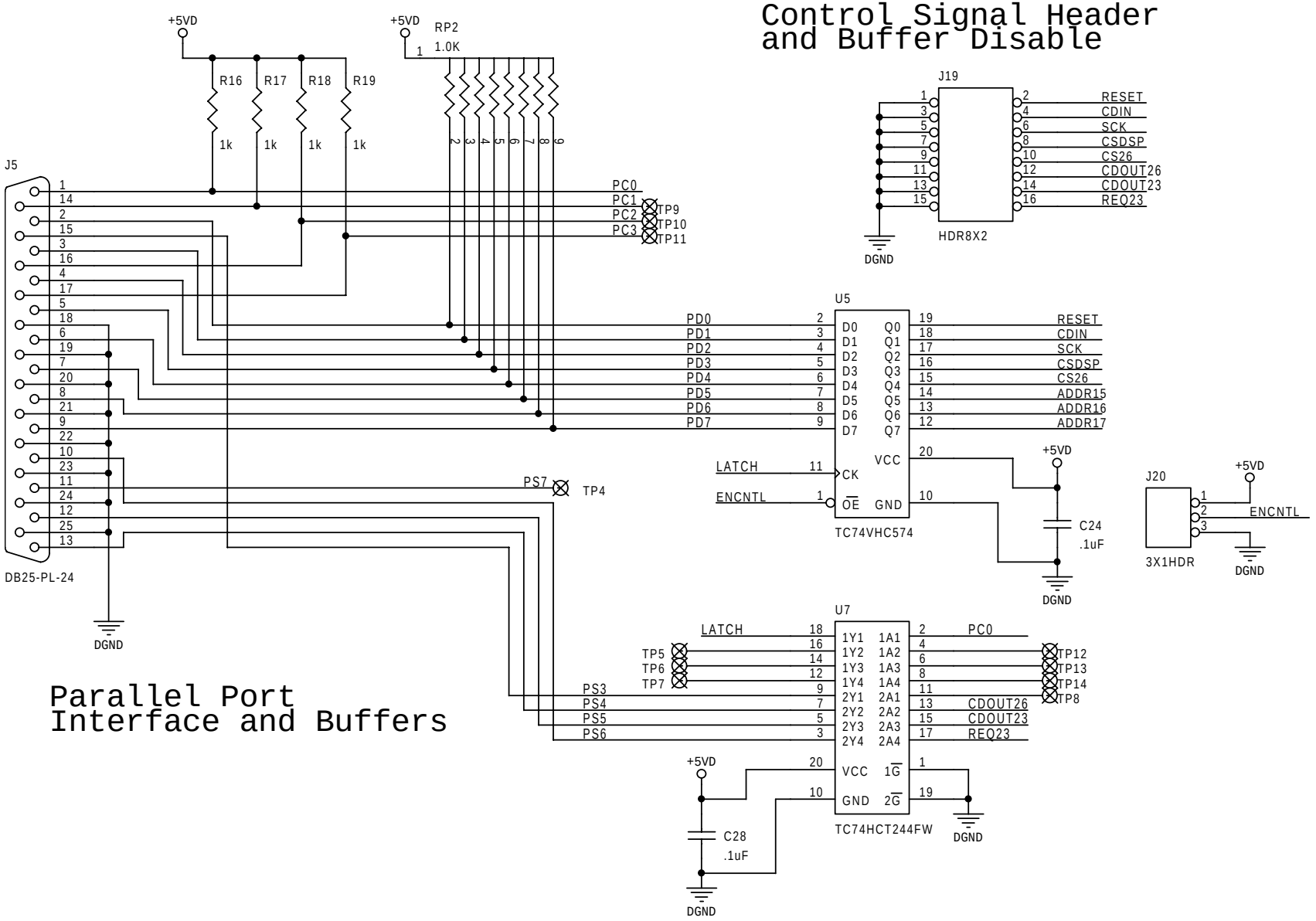

Figure 2. Control Interface

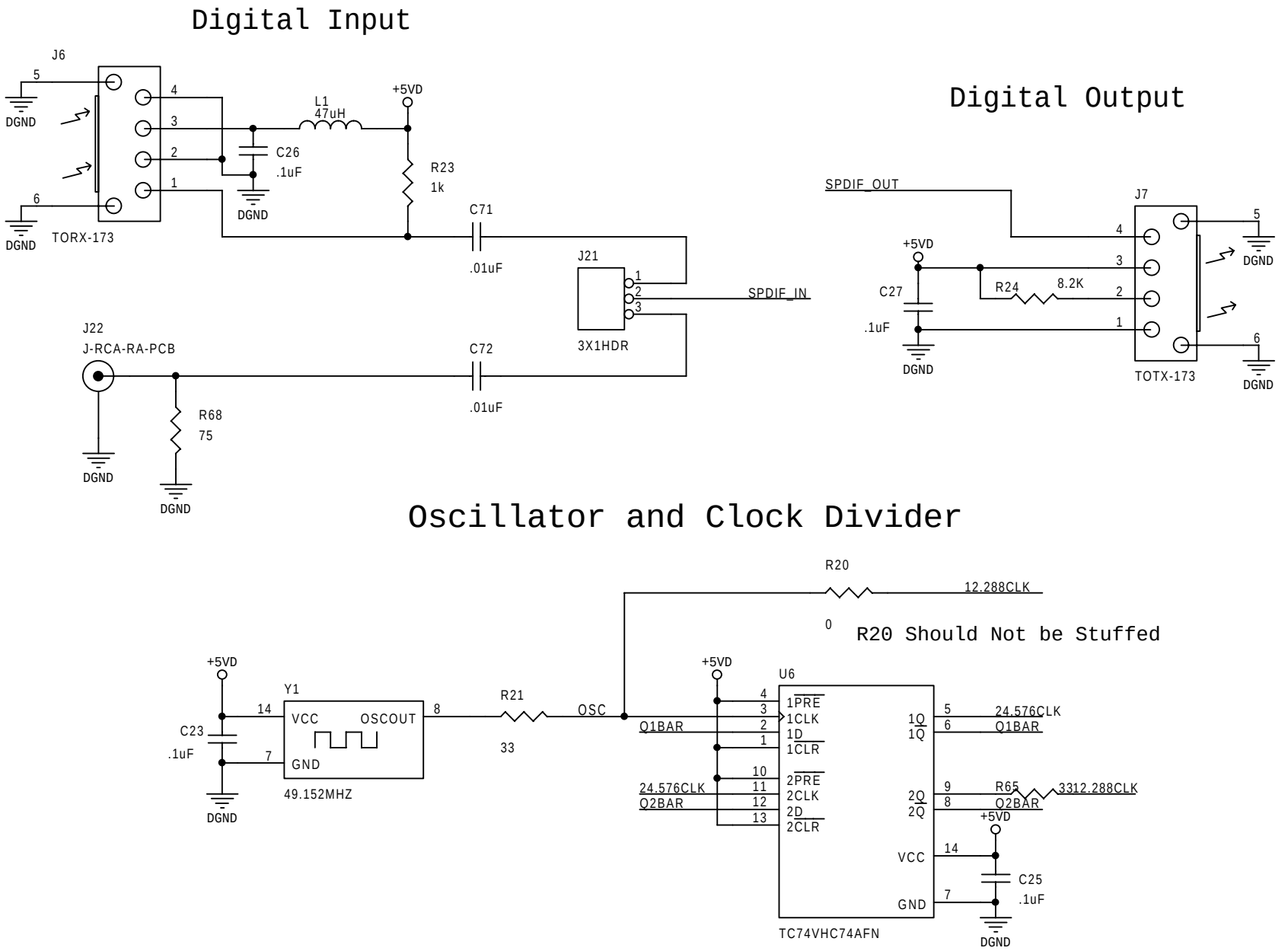

Figure 3. Digital I/O and Clock Divider

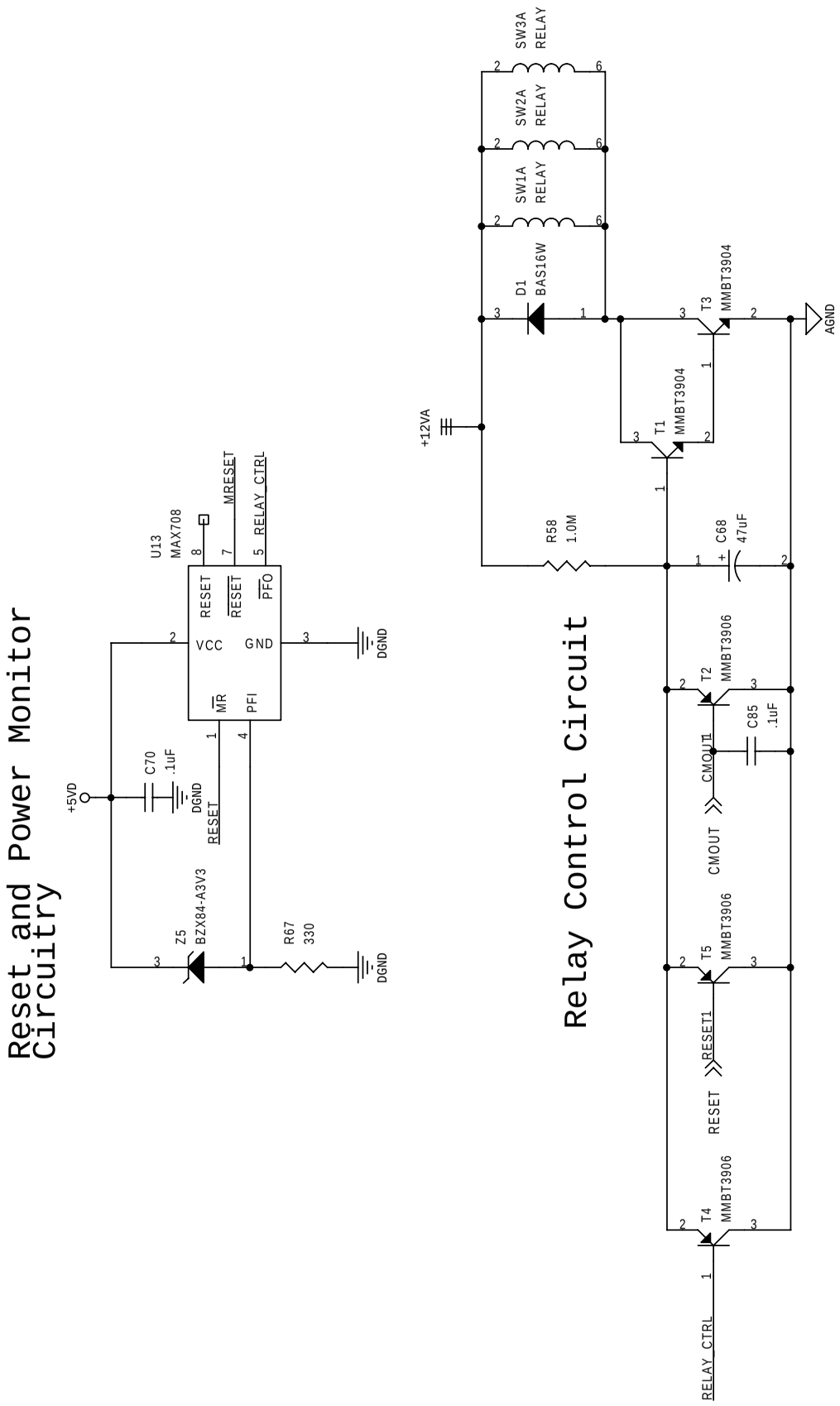

Figure 4. Reset and Power Monitor

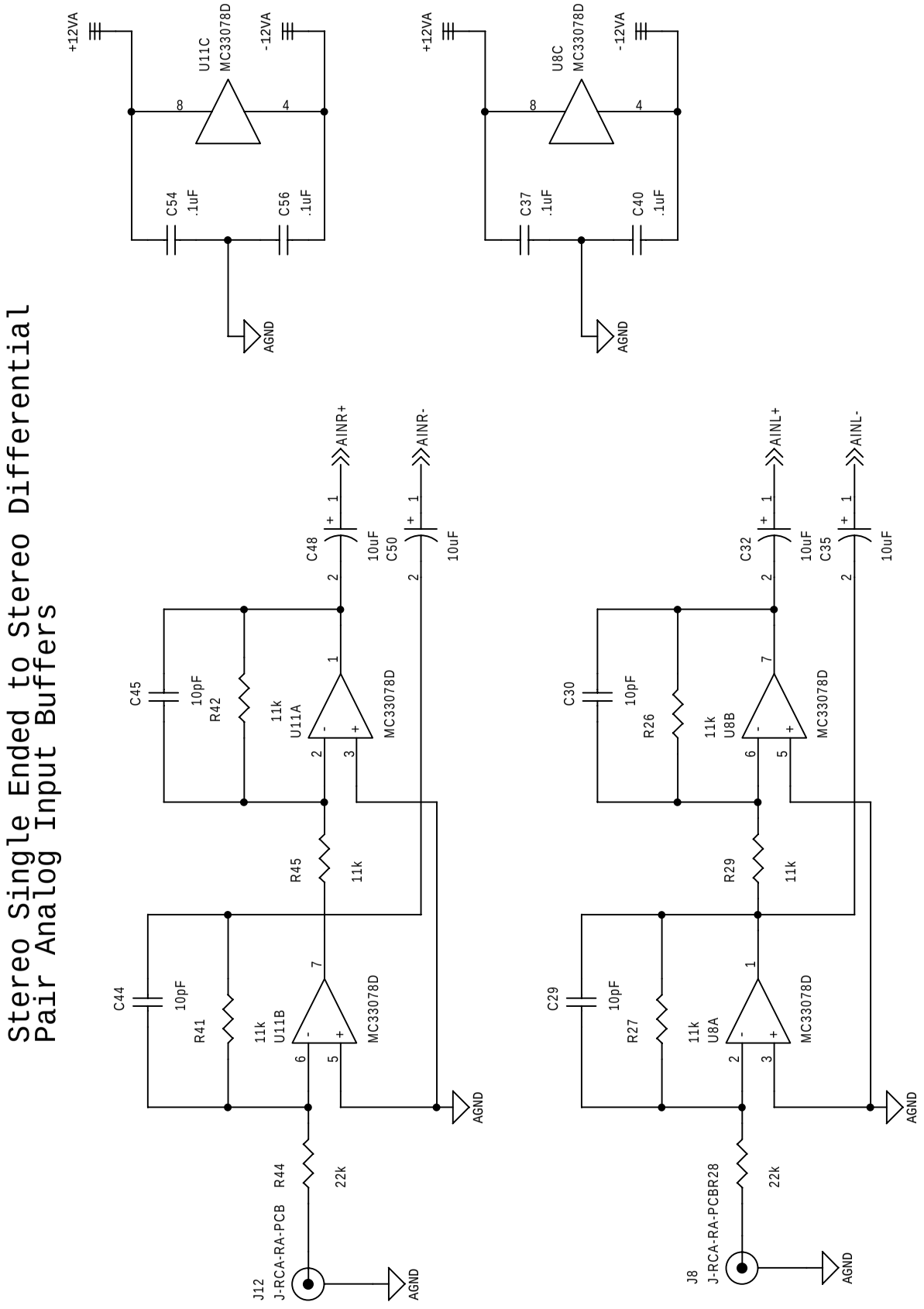

Figure 5. Analog Input

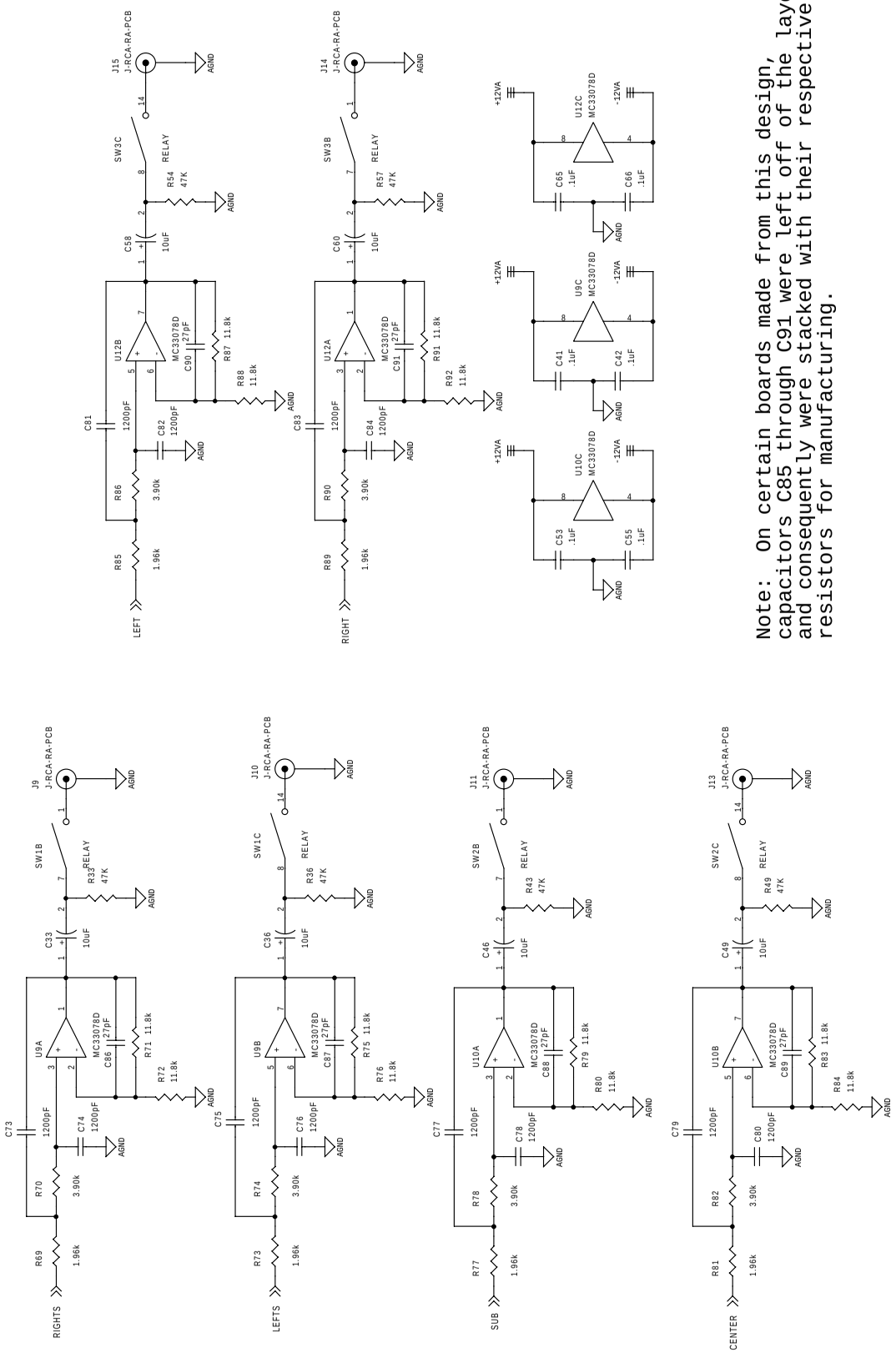

Figure 6. Analog Output

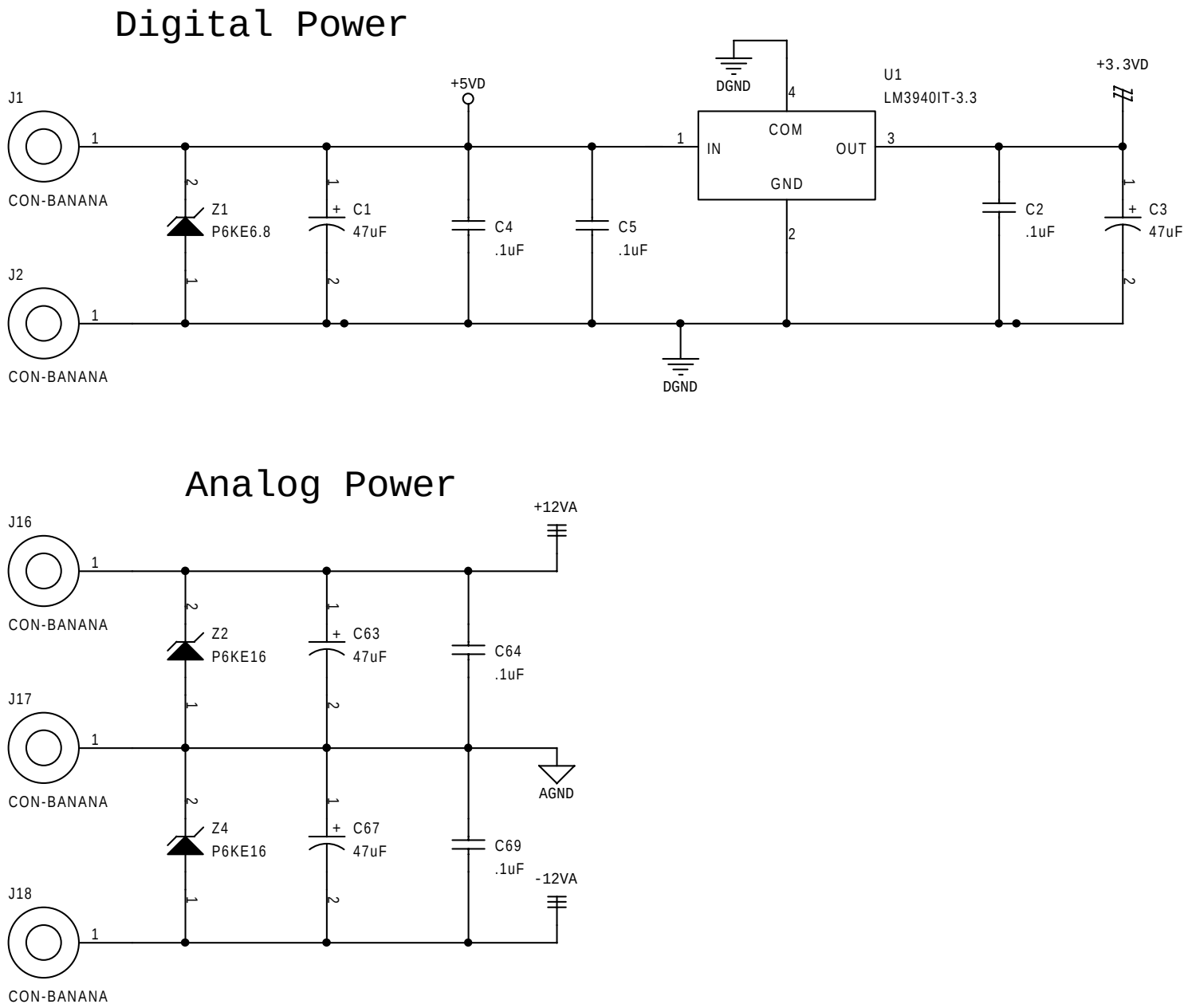

Figure 7. Power

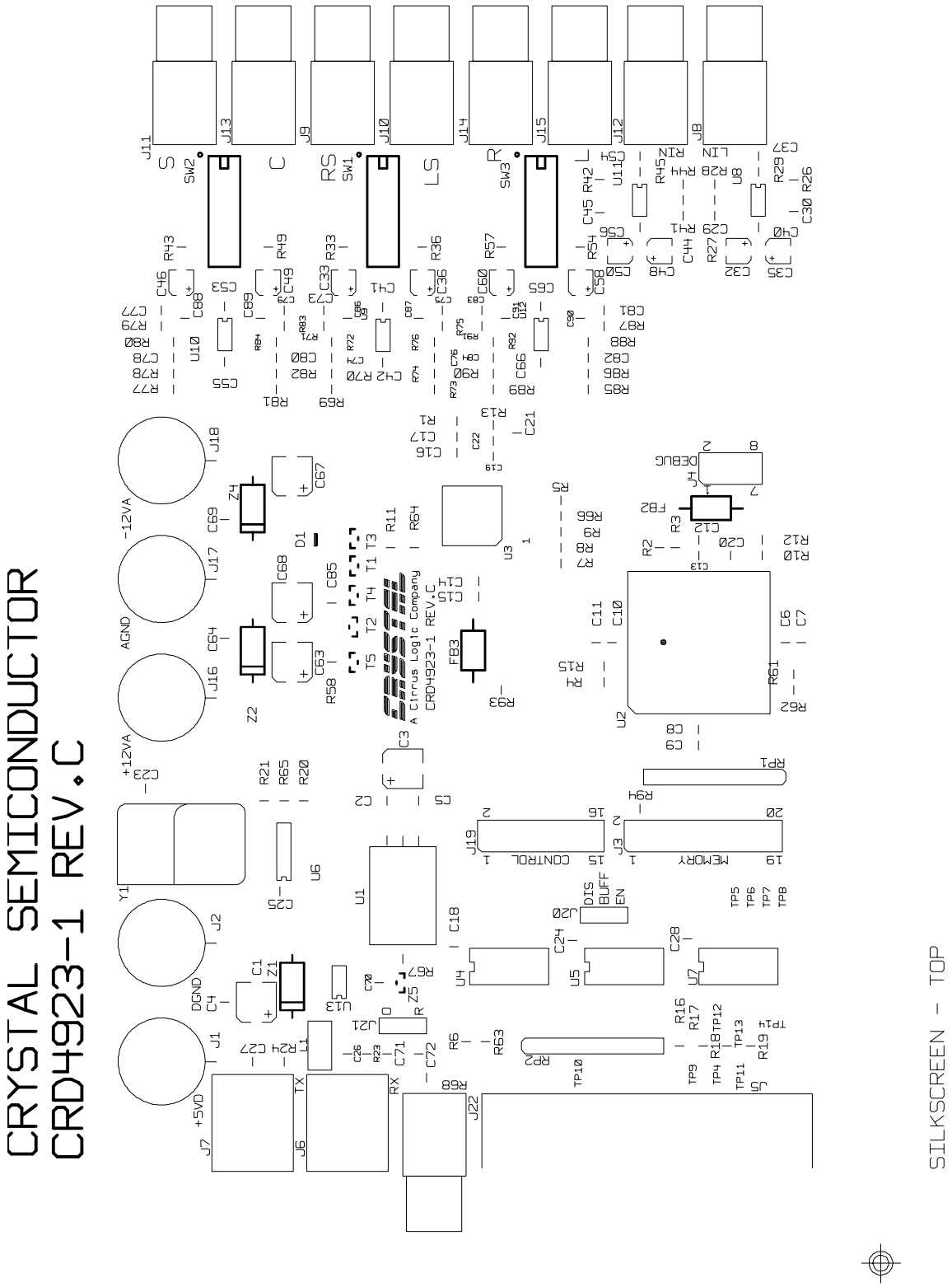

Figure 8. Silkscreen Top (SSTOP)

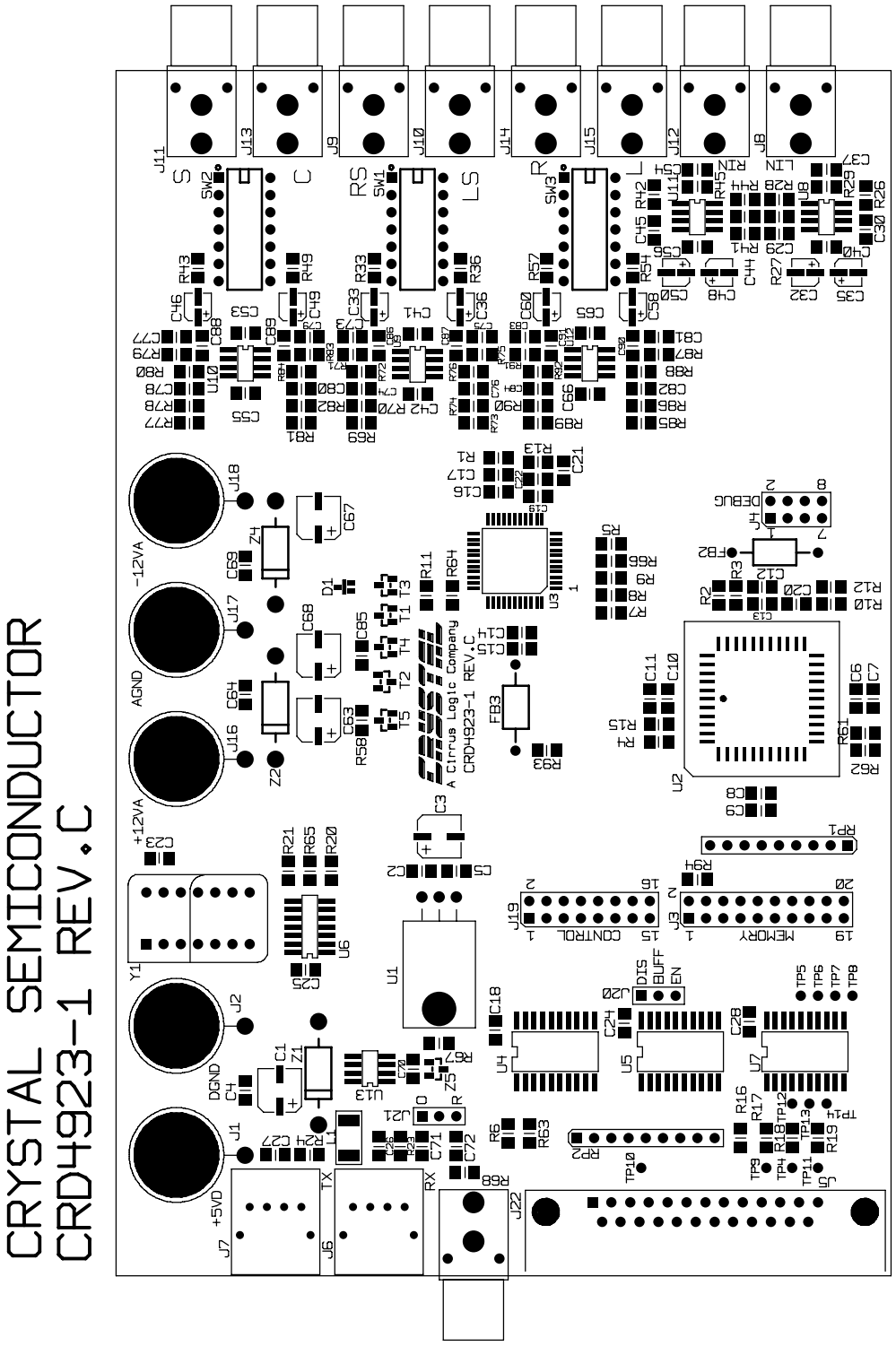

Figure 9. Silkscreen Top (ASSYTOP)

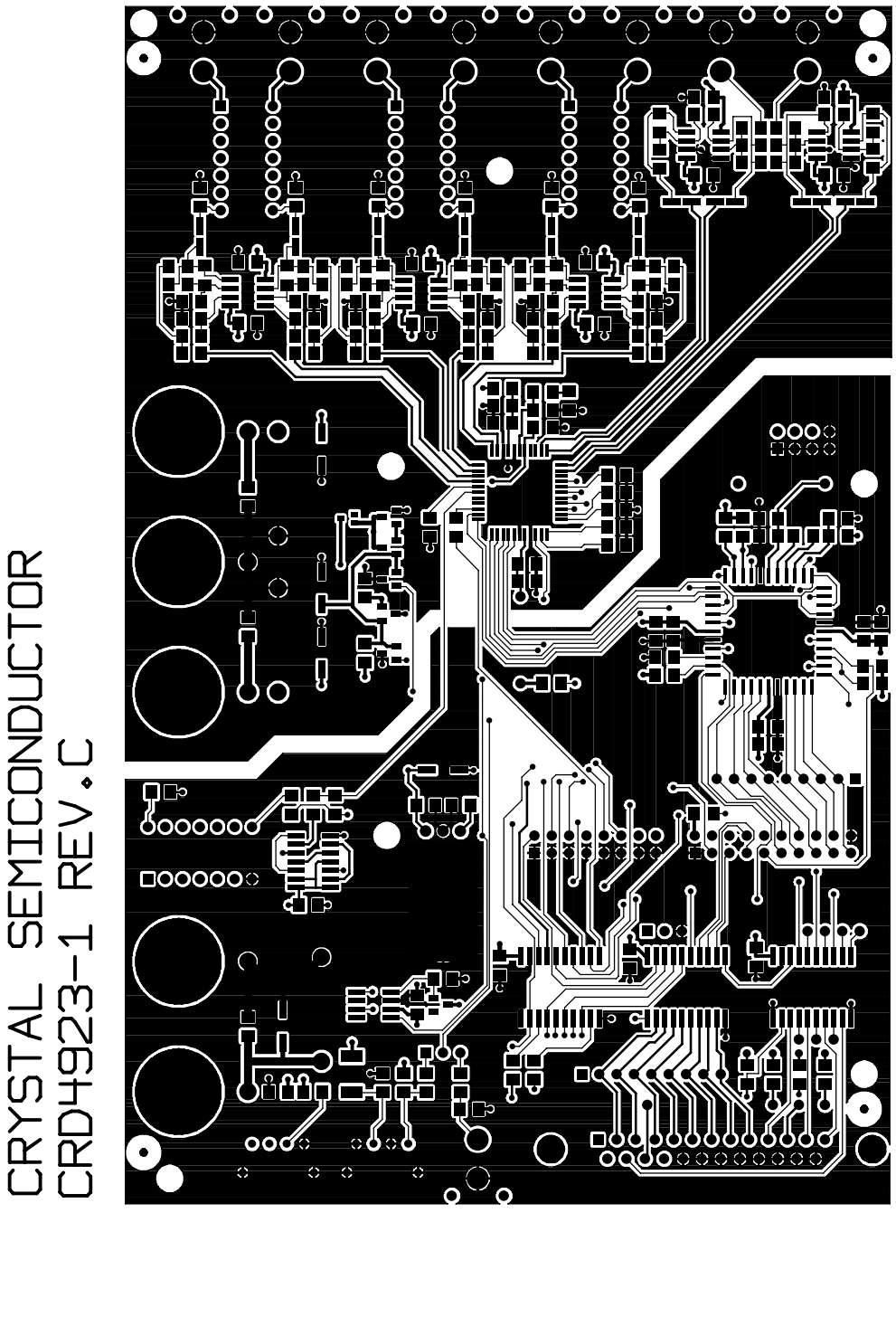

Figure 10. Copper Top

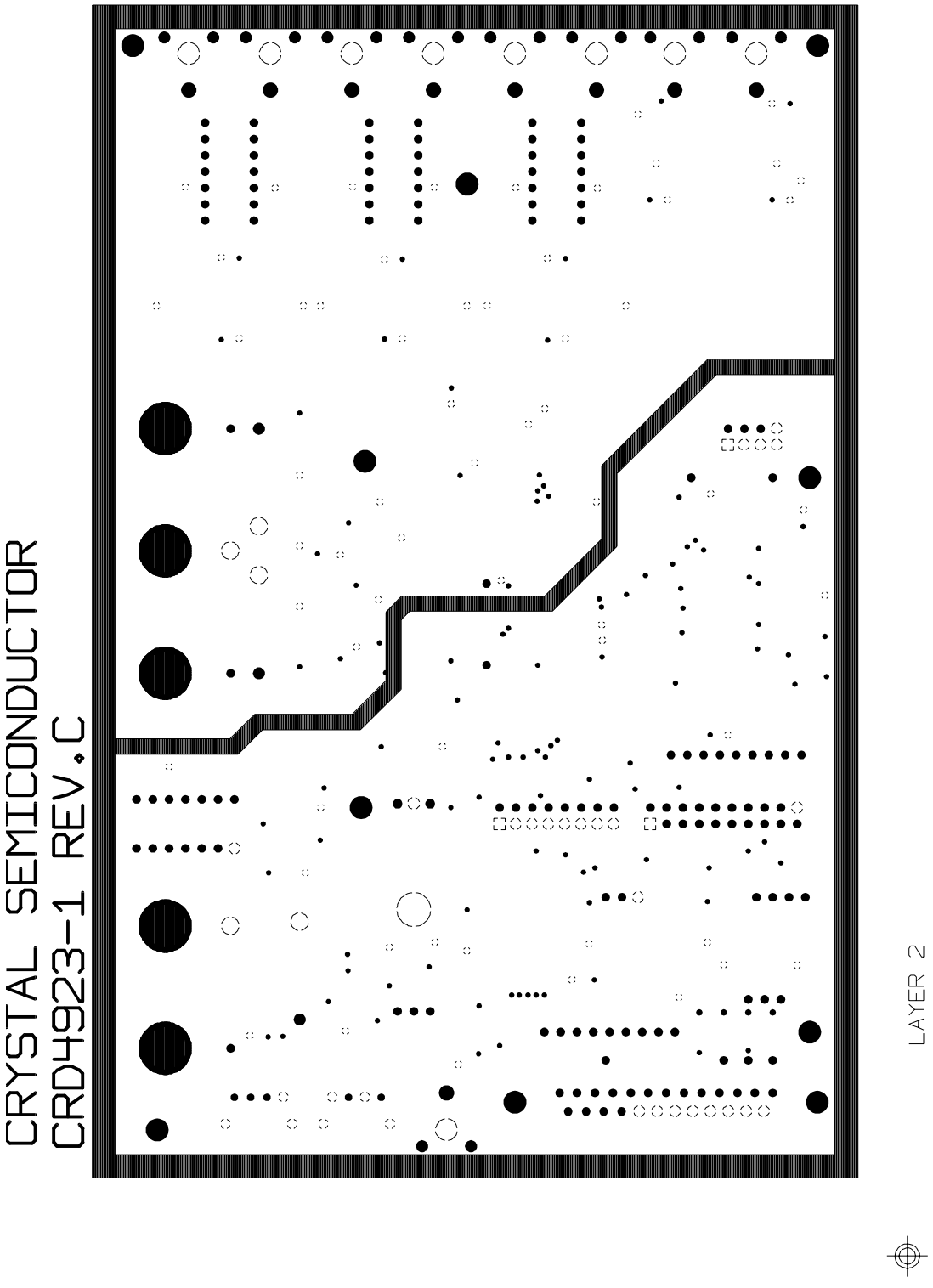

Figure 11. Ground

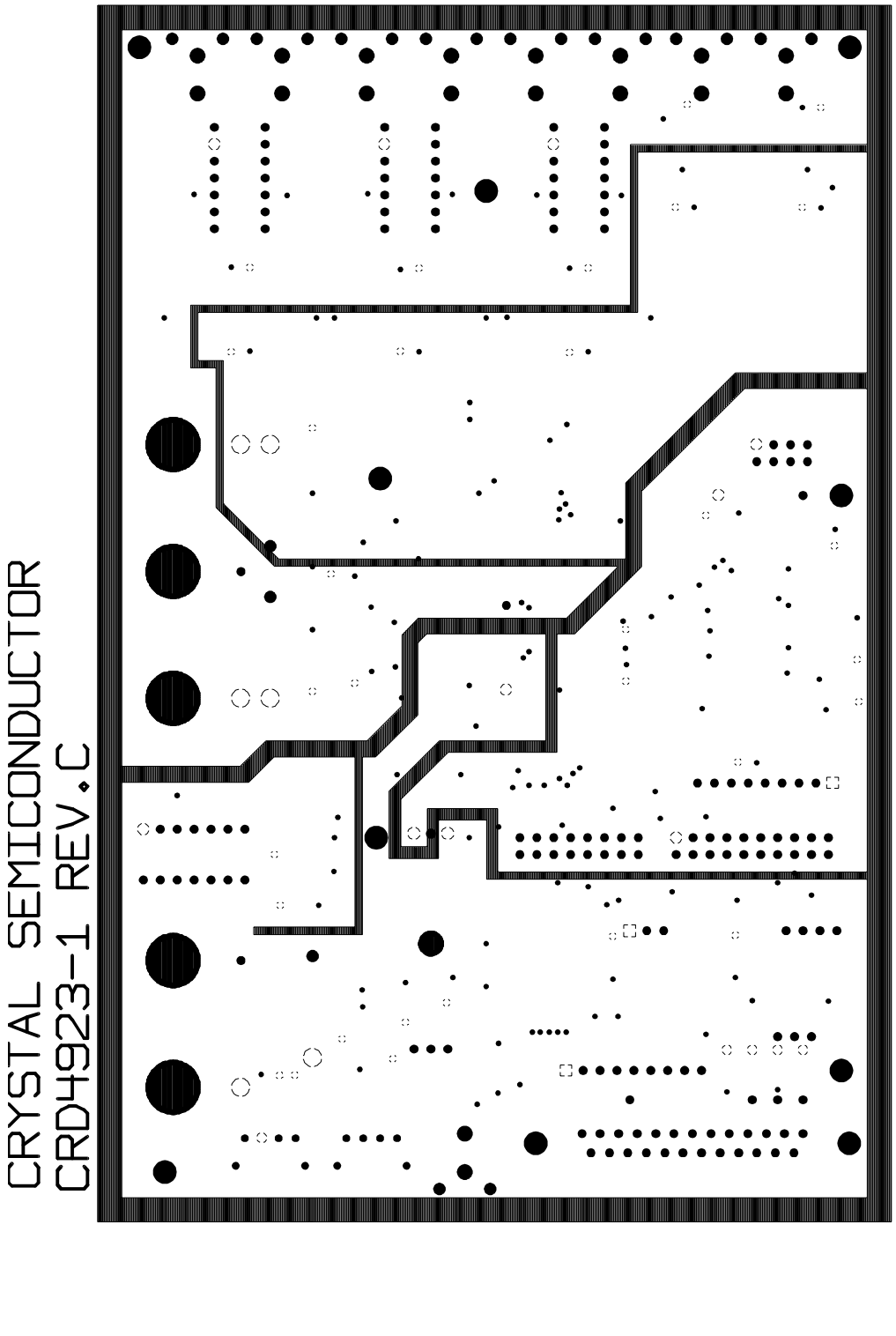

Figure 12. Power

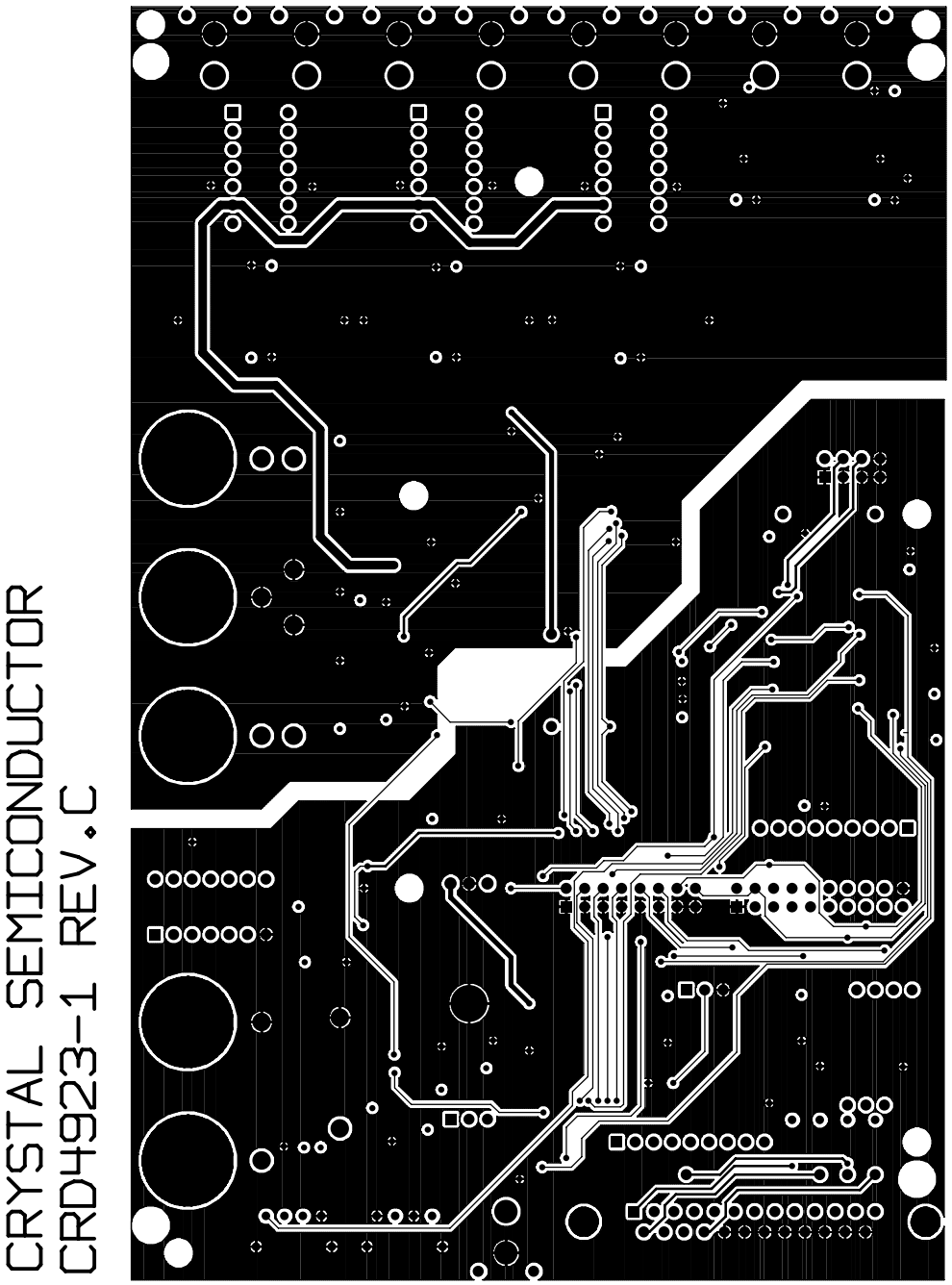

Figure 13. Copper Bottom

BILL OF MATERIALS - CRD4923-1 REV.C

Item	Quan.	Reference	Part Name	Manufacturer	Footprint	Value	Description
1	5	C1,C3,C63,C67,C68	ECEV1CA470SP	PANASONIC	CSP_ELEC_260SQ	47uF	CAP,ELEC,47uF,SM260SQ,20%,16V
2	30	C2,C4,C5,C6,C8,C10, C13,C14,C16,C18,C23, C24,C25,C26,C27,C28, C37,C40,C41,C42,C53, C54,C55,C56,C64,C65, C66,C69,C70,C85	C1206C104J5RAC	KEMET	CC1206	.1uF	CAP,.1uF,SM1206,5%,X7R,50V
3	7	C7,C9,C11,C12,C15,C17, C19	C1206C105K5RAC	KEMET	CC1206	1uF	CAP,1uF,SM1206,10%,X7R,50V
4	1	C20	C1206C224J5RAC	KEMET	CC1206	.22uF	CAP,.22uF,SM1206,5%,X7R,50V
5	1	C21	C1206C153J5RAC	KEMET	CC1206	.015uF	CAP,.015uF,SM1206,5%,X7R,50V
6	1	C22	C1206C152J5GAC	KEMET	CC1206	1500pF	CAP,1500pF,SM1206,5%,COG,50V
7	4	C29,C30,C44,C45	C1206C100J5GAC	KEMET	CC1206	10pF	CAP,10pF,SM1206,5%,COG,50V
8	10	C32,C33,C35,C36,C46, C48,C49,C50,C58,C60	ECEV1CA100SR	PANASONIC	CSP_ELEC_170SQ	10uF	CAP,10uF,ELEC,SM170SQ,20%,16V
9	2	C72,C71	C1206C103J5RAC	KEMET	CC1206	.01uF	CAP,.01uF,SM1206,5%,X7R,50V
10	12	C73,C74,C75,C76,C77, C78,C79,C80,C81,C82, C83,C84	C1206C122J5GAC	KEMET	CC1206	1200pF	CAP,1200pF,SM1206,5%,COG,50V
11	6	C86,C87,C88,C89,C90, C91	C1206C270J5GAC	KEMET	CC1206	27pF	CAP,27pF,SM1206,5%,COG,50V
12	1	D1	BAS16W	PHILLIPS	SOT323	BAS16W	DIODE,SOT323,SIGNAL DIODE
13	2	FB2,FB3	FERRITE BEAD	TDK	IND_FB43_226	FERRITE BEAD	FERRITE BEAD - THRU HOLE
14	2	J1,J16	111-0102-001	JOHNSON COMPONENTS	BANANA	CON-BANANA	CONN,BANANA,TH,BINDING POST,RED,INSULATED STANDARD
15	2	J2,J17	111-0103-001	JOHNSON COMPONENTS	BANANA	CON-BANANA	CONN,BANANA,TH,BLACK,BINDING POST,INSULATED STANDARÓ
16	1	J3	TSW-110-07-G-D	SAMTEC	HDR10X2	HDR10X2	HDR,10X2,.025"PIN,.1"CNTR
17	1	J4	TSW-104-07-G-D	SAMTEC	HDR4X2	HDR4X2	HDR,4X2,.025"PIN,.1"CNTR
18	1	J5	DB25-PL-24	ADAM TECH	DB25-HM	DB25-PL-24	CONN,RT.ANG,TH,D-SUB,25PN,MALE
19	1	J6	TORX173	TOSHIBA	TORX-173	TORX-173	OPTICAL TOSLINK RECIEVER
20	1	J7	TOTX173	TOSHIBA	TOTX-173	TOTX-173	OPTICAL TOSLINK TRANSMITTER
21	9	J8,J9,J10,J11,J12,J13, J14,J15,J22	16PJ097	MOUSER	J-RCA-RA-PCB	J-RCA-RA-PCB	CONN,.25",RCA,PHONO JACK
22	1	J18	111-0104-001	JOHNSON COMPONENTS	BANANA	CON-BANANA	CONN,BANANA,TH,GREEN,BINDING POST,INSULATED STANDARØ
23	1	J19	TSW-108-07-G-D	SAMTEC	HDR8X2	HDR8X2	HDR,8X2,.025"PIN,.1"CNTR
24	2	J20,J21	TSW-103-07-G-S	SAMTEC	HDR3	3X1HDR	HDR,3X1,.025"PIN,.1"CNTR

Item	Quan.	Reference	Part Name	Manufacturer	Footprint	Value	Description
25	1	L1	SIMID03-47uH	SIEMENS	IND1812	47uH	IND,47uH,10%,210mA
26	1	RP1	4609X-101-103	BOURNS	RES_SIP9	10k	RES,10K,9 PIN SIP PARALLEL NETWORK
27	1	RP2	4609X-101-102	BOURNS	RES_SIP9	1.0K	RES,1.0K,9 PIN SIP PARALLEL NETWORK
28	1	R1	9C12063A2R00J	Philips	RES/RC1206	2	RES,2.0,SM1206,5%,1/4W
29	11	R2,R4,R5,R10,R11,R12, R15,R62,R66,R93,R94	9C12063A1002J	Philips	RES/RC1206	10k	RES,10k,SM1206,5%,1/4W
30	2	R3,R61	9C12063A4701J	Philips	RES/RC1206	4.7k	RES,4.7k,SM1206,5%,1/4W
31	5	R6,R21,R63,R64,R65	9C12063A33R0J	Philips	RES/RC1206	33	RES,33,SM1206,5%,1/4W
32	4	R7,R8,R9,R20	9C12063A0R00J	Philips	RES/RC1206	0	RES,0,SM1206,5%,1/4W
33	1	R13	9C12063A4302F	Philips	RES/RC1206	43k	RES,43k,SM1206,1%,1/4W
34	5	R16,R17,R18,R19,R23	9C12063A1001J	Philips	RES/RC1206	1k	RES,1k,SM1206,5%,1/4W
35	1	R24	9C12063A8201J	Philips	RES/RC1206	8.2K	RES,8.2k,SM1206,5%,1/4W
36	6	R26,R27,R29,R41,R42, R45	9C12063A1102F	Philips	RES/RC1206	11k	RES,11k,SM1206,1%,1/4W
37	2	R44,R28	9C12063A2202F	Philips	RES/RC1206	22k	RES,22k,SM1206,1%,1/4W
38	6	R33,R36,R43,R49,R54, R57	9C12063A4702J	Philips	RES/RC1206	47K	RES,47k,SM1206,5%,1/4W
39	1	R58	9C12063A1004J	Philips	RES/RC1206	1.0M	RES,1M,SM1206,5%,1/4W
40	1	R67	9C12063A3300F	Philips	RES/RC1206	330	RES,330,SM1206,1%,1/4W
41	1	R68	9C12063A75R0J	Philips	RES/RC1206	75	RES,75,SM1206,5%,1/4W
42	6	R69,R73,R77,R81,R85, R89	9C12063A1961F	Philips	RES/RC1206	1.96k	RES,1.96k,SM1206,1%,1/4W
43	6	R70,R74,R78,R82,R86, R90	9C12063A3901F	Philips	RES/RC1206	3.90k	RES,3.90k,SM1206,1%,1/4W
44	12	R71,R72,R75,R76,R79, R80,R83,R84,R87,R88, R91,R92	9C12063A1182F	Philips	RES/RC1206	11.8k	RES,11.8k,SM1206,1%,1/4W
45	3	SW1,SW2,SW3	HE722A1200	HAMLIN	DIP14	RELAY	REED RELAY, 12V, DUAL PACKAGE
46	14	TP1,TP2,TP3,TP4,TP5, TP6,TP7,TP8,TP9,TP10,TP11,TP12,TP13,TP14	TP		VIA60	TP	TESTPOINT,VIA 60
47	2	T3,T1	MMBT3904	MOTOROLA	SOT23	MMBT3904	NPN TRANSISTOR, SOT23
48	2	T2,T4, T5	MMBT3906	MOTOROLA	SOT23	MMBT3906	PNP TRANSISTOR, SOT23
49	1	U1	LM3940IT-3.3	NATIONAL SEMICONDUCTOR	TO-220	LM3940IT-3.3	+3.3V REGULATOR, TO-220
50	1	U2	CS4923	CRYSTAL	PLCC44	CS4923	DSP
51	1	U3	CS4226	CRYSTAL	TQFP44	CS4226	CODEC
52	1	U4	TC74VHC244FW	TOSHIBA	SOIC20 300MIL	TC74VHC244FW	OCT BUFF,VHC,SOIC20 300MIL,3 & 5 V TOL

Item	Quan.	Reference	Part Name	Manufacturer	Footprint	Value	Description
53	1	U5	TC74VHC574FW	TOSHIBA	SOIC20 300MIL	TC74VHC574	OCT D FF,VHC,SOIC20 300MIL,3 & 5 V TOL
54	1	U6	TC74VHC74AFN	TOSHIBA	SOIC14 150MIL	TC74VHC74AFN	DUAL D FF,VHC,SOIC14 150MIL,3 & 5 V TOL
55	1	U7	TC74HCT244FW	TOSHIBA	SOIC20 300MIL	TC74HCT244FW	OCT BUFF,HCT,SOIC20 300MIL,3 & 5 V TOL
56	5	U8,U9,U10,U11,U12	MC33078D	MOTOROLA	SO-8	MC33078D	IC,SO-8,DUAL SUPPLY DUAL OP AMP
57	1	U13	MAX708CSA	MAXIM	SO-8	MAX708	IC, LOW COST uP SUPERVISORY CIR-QUIT
58	1	Y1	CX21AF-49.1520MHZ	CAL CRYSTAL	CLKOSC_GENERIC	49.152MHZ	OSC,49.152MHZ,TTL/CMOS,FULL SIZE
59	1	Z1	P6KE6.8A	MOTOROLA	CASE17-02	P6KE6.8	AXIAL ZENER DIODE,DO-7,6.8V
60	2	Z2,Z4	P6KE16A	MOTOROLA	CASE 17-02	P6KE16	AXIAL ZENER DIODE,DO-7,16V
61	1	Z5	BZX84-A3V3	Philips	SOT23	BZX84-A3V3	ZENER, 3.3V, 5ma

APPENDIX A: SOFTWARE TOOLS FOR THE CRD4923

A variety of tools is shipped with the CRD4923 to allow the user to communicate with the CRD4923. These tools are DOS based and run through the parallel port of a personal computer running DOS (or Windows running a DOS shell). Each program uses the default address of 0x378 for the parallel port. If your computer does not work with this address, the default can be changed with a command line switch.

CRD23_LD.EXE

CRD23_LD.EXE is a program that boots and loads the CS4923 and configures the CS4226. Its usage is as follows:

Usage: crd23_ld <input_file.ld> [-pXXX] [-v]
-p = parallel port address
XXX = address (0x278, 378 or 3bc)*
-v = disable verbose mode
** = default\n*

This program performs all necessary handshaking as described in the CS4923 Users Guide to perform a download. To download the file AC3.LD to a parallel port with address 0x3bc, one would type the following at the command line:

crd23_ld AC3.LD -p3bc

CRD23CMD.EXE

CRD23CMD.EXE is a program that sends messages to the CS4923 in the SPI format. This program can send commands from the command line or it can also send commands from a file. The CRD4923 is shipped with configuration files that allow the CS4923 to be configured in the modes given in the Application Messaging section of the CS4923 Users Guide. The following is its usage:

Usage: crd23cmd <[ABCDEF] or [-fY]> [-pXXX] [-v]
ABCDEF = Three byte hex command
Y = .cfg file containing configuration parameters");
-p = parallel port address
XXX = address (0x278, 378 or 3bc);*
-v = disable verbose mode
** = default*

The following example shows how the hex message 0x000001 would be sent with a parallel port address of 0x378:

crd23cmd 000001

The following example shows how the messages in the configuration file *AC3PRO.CFG* would be sent with a parallel port address of 0x278:

crd23cmd -fac3pro.scg -p278

CRD23_RD.EXE

CRD23_RD is a program that reads back responses from the CS4923. This program polls on the interrupt request line of the CS4923 to determine if the CS4923 has anything to be read. It should be noted that without sending a message via CRD23CMD that will illicit a response, this program will do nothing. For more on communicating with the CS4923, the CS4923 Users Guide should be read. The following is the CRD23_RD usage:

Usage: crd23_rd [-pXXX] [-v] [-h]
-p = parallel port address
XXX = address (0x278, 378 or 3bc)*
-v = disable verbose mode
-h = this message
** = default*

WRITE26.EXE

WRITE26.EXE is a program that writes registers in the CS4226 in the SPI format. This program sends values from the command line. The following is its usage:

Usage: write26 <[ABCD]> [-pXXX] [-v]
AB = Register to be written
CD = Value to be written to register
-p = parallel port address
XXX = address (0x278, 378 or 3bc);*
-v = disable verbose mode
** = default*

READ26.EXE

READ26.EXE is a program that reads messages from the CS4226 in the SPI format. After executing this program the value of the register is written to the screen. The following is its usage:

Usage: read26 <[AB]> [-pXXX] [-v]
AB = Register to be read
-p = parallel port address
XXX = address (0x278, 378 or 3bc);*
-v = disable verbose mode
** = default*

Batch Files

The batch files (.bat) shipped with the CRD4923 automate the control messages that need to be sent to the CRD4923 to set up the CS4923 and the CS4226 for different modes of operation. The different modes of operation are illustrated further in section 5, Application Messaging, of AN115, *The CS4923 Users Guide*. Specifically the batch files follow section 5.2, Application Modes of AN115. The batch files send the neccesary configuration messages thru CRD23CMD and a .CFG file and also set up the clocking scheme of the CS4226 for the mode.

The following list displays the different modes that are provided through batch files and how to initiate them. This list is in no way demonstrative of all the modes supported by the CRD4923.

SINE WAVES:

1. crd23_ld asine.ld -pXXX <return>

AC3 SPDIF INPUT:

1. crd23_ld ac303.ld -pXXX <return>
2. ac3.bat -pXXX <return>

AC3 SPDIF INPUT with Pro Logic Decode

1. crd23_ld ac303.ld -pXXX <return>
2. ac3pro.bat -pXXX <return>

PCM Mixing with AC3 SPDIF Input

1. crd23_ld ac303.ld -pXXX <return>
2. pcmmix.bat -pXXX <return>

PCM Prologic decode at 48Khz

1. crd23_ld ac303.ld -pXXX <return>
2. pcmpro48.bat -pXXX <return>

PCM pass through at 48KHz

1. crd23_ld ac303.ld -pXXX <return>
2. pcmps48.bat -pXXX <return>

• Notes •


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