Product Technical Brief

CS61584A Enhanced Dual T1/E1 LIU

The CS61584 Dual T1/E1 LIU has been modified and improved to create the CS61584A. The CS61584A has all of the features and performance of the CS61584, plus many additional features. Incorporating these improvements made it necessary to make several changes to the pinout and functionality which the user must account for when upgrading to the CS61584A. When reviewing the following information, refer to Table 1 for a description of the pinout changes and to Table 2 for changes to the timing specifications.

FUNCTIONAL CHANGES

- The CS61584A has two Remote Loopback pins, RLOOP1 and RLOOP2, and one Local Loopback pin, LLOOP. The CS61584 has one Remote Loopback (RLOOP) and two Local Loopbacks (LLOOP1 and LLOOP2). (See Table 1.) Local loopback can still be selected with the CS61584A on a per channel basis only in conjunction with TAOS for that channel.

  In addition, the LLOOP pin on the CS61584A selects local loopback 2 - the loopback all the way through the analog interface, rather than local loopback 1 - the data path loopback. See the CS61584A data sheet for a full explanation.

- During Parallel Port Host mode operation when BTS = 1, the IPOL pin is remapped to $\overline{\text{DTACK}}$ functionality to be compliant with the Motorola parallel interface specification. The polarity of the $\overline{\text{INT}}$ pin is active low when using parallel port mode with Motorola bus timing. See Table 1.

- In Serial Port mode, the pins SAD4 and SAD5 become ZTX1 and ZTX2, respectively. These pins must be driven low to enable the output drivers on TTIP and TRING. These pins were formerly no connects in this mode. The output drivers may also be enabled using the CON[3:0] pins or the CON[3:0] bits in the Control B registers. See Table 1.

- The JTAG and parallel port errata issues contained in document ER114A2 (items 1 to 3) are corrected. These include a restriction on the timing of ALE relative to $\overline{\text{CS}}$, a problem with the input of the IDCODE register, and an address dependent data corruption problem.

- The device no longer has to be reset following a change in the CON[3:0] pin settings.

- The Reserved bit in the Status register (channel 2, bit 1) is redefined to be “CLKLOST.” There is a corresponding mask bit in the Mask register (channel 2).

- The CS61584A driver output goes to high impedance if TCLK or REFCLK is absent. (The CS61584 driver puts out spaces if TCLK is absent; with no REFCLK, its behavior is undefined.) If the jitter attenuator is in the transmit path, the driver will go into the high impedance state after 175 to 182 TCLK clock cycles. If the jitter attenuator is not in the transmit path, the driver will go to high impedance after 5 to 12 TCLK clock cycles. The output starts driving again after valid transitions are detected on both REFCLK and TCLK and TCLK has been active for four cycles.

  The behavior of the CS61584A after power-up

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or reset depends on the interface mode. In hardware mode, the driver is in high impedance until REFCLK is present and four clock cycles are input to TCLK. (assuming the CON[3:0] pins are not set to a high impedance value). In serial or parallel host mode, the CON[3:0] bits in the Control B register are set to a high impedance state by power up or reset, so in addition to the presence of REFCLK and TCLK, the user must set CON[3:0] to a non Hi-Z value for the outputs to become active.

- The RPOS and RNEG (or RDATA) digital outputs may be forced to unframed all-ones on a per-channel basis during host mode operation. This is done on channel "n" by setting both LLOOP1n and LLOOP2n bits in the Control B register to "1". This feature is independent of the receive LOS condition.

- The Reserved bit in the Mask Register (channel 1, bit 1) is redefined to "AAO" (Automatic All Ones). When AAO = 1, the RPOS and RNEG (or RDATA) digital outputs are automatically forced to an unframed all-ones data pattern during a receive LOS condition.

- The RPOS, RNEG, and RCLK pins are forced to Zero (squelched) during an LOS condition. This is overridden by enabling Local Loopback 1 (digital loopback) or by setting AAO = 1.

- An excessive zeros test that complies with ANSI T1.231 has been added for T1 operation. The Reserved bit in the Control A register (channel 2, bit 7) is redefined to "EXZ" in the CS61584A. In coder mode (CODERn = 1) setting EXZ to 1 causes the BPV output pin to be OR'ed with excessive zero events. In AMI mode (AMI-Rn = 1), the BPV pin goes high for one RCLK bit period when 16 or more zeros are received on the RTIP/RRING pins. In B8ZS mode (AMI-Rn = 0), the BPV pin goes high for one RCLK bit period when 8 or more zeros are received on RTIP/RRING. For E1 operation, when AMI-Rn = 0 (HDB3), BPV will go high for one RCLK cycle when four or more consecutive zeros are received. The EXZ bits are disabled when the device is configured in E1-AMI mode.

PERFORMANCE IMPROVEMENTS

- The jitter attenuator is enhanced to meet ETSI ETS 300 011 and CTR 12 jitter attenuation specifications in E1 mode. The -3 dB knee of the jitter attenuator has moved from 5.5 Hz to 1.25 Hz. Setting the ATTEN[1:0] pins or Control A register bits to "11" will place the jitter attenuator in the receive path with a -3 dB knee at 1.25 Hz for both T1 and E1 modes.

- The serial port output timing on the SDO pin has been improved when data is output on the falling edge of SCLK (SPOL = 0). The first bit output from SDO has a setup and hold time around the falling edge of the 9^{th} SCLK cycle (instead of the 8^{th} cycle) to allow the SDI and SDO pins to be tied together for Intel microprocessors with bidirectional serial ports.

- All outputs of the device may be disabled to facilitate circuit board testing. In hardware mode, setting both the PD1 and PD2 pins to "1" will power down the device and tristate all outputs. In host mode, setting both the PD1 and PD2 bits to "1" will put all outputs into high impedance except the data outputs on the processor interface (SDO or AD[7:0]).

TIMING CHANGES IN PARALLEL PORT

The timing characteristics for the host mode access have been revised in the CS61584A. Table 2 shows a summary of the changes. Refer to the CS61584A data sheet for the latest timing specifications.

PLCC pin	TQFP pin	CS61584	CS61584A
		Hardware Mode	
7	63	RLOOP	RLOOP1
6	62	LLOOP1	RLOOP2
5	61	LLOOP2	LLOOP
		Host Mode - Parallel Port	
44	33	IPOL	IPOL/DTACK
		Host Mode - Serial Port	
24	15	N/C	ZTX1
45	34	N/C	ZTX2

Table 1. Pinout Differences Between CS61584, CS61584A

Parameter	Symbol	CS61584 (ns)	CS61584A (ns)
$\overline{CS}$ Setup Time	t_{cs}	20	50
$\overline{CS}$ setup for RAM/ROM	t_{csr}	-	130
$\overline{CS}$ Hold Time	t_{ch}	0	20
Write Data Hold Time	t_{dhw}	0	5
Delay Time AS or ALE to $\overline{WR}$, $\overline{RD}$	t_{ased}	20	40
$\overline{DTACK}$ Delay Time	t_{dkd}	-	5
$\overline{DTACK}$ Hold Time	t_{dkh}	-	5
AS/ALE Min Low for RAM/ROM	t_{aamir}	-	50

Table 2. Timing Differences Between CS61584, CS61584A


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