Crystal LAN™ 10Base-T and 100Base-T Transceiver Evaluation Board

FEATURES

- **IEEE 802.3 compliant 10Base-T and 100Base-T Physical Interface.**
- **Media Supported:**
  - — 10Base-T
  - — 100Base-T
- **IEEE 802.3u MII Interface with extended register support.**
- **LED indicators for Power, Link Status, Collision, Full/Half Duplex, Transmit Activity, Receive Activity, 100 Mb/s Speed, and 10 Mb/s Speed.**
- **Hardware configurable through jumper settings, or software configurable through the MII interface.**
- **Operates from single 5 V supply, or may be optionally configured for interface to 3.3 V MII.**

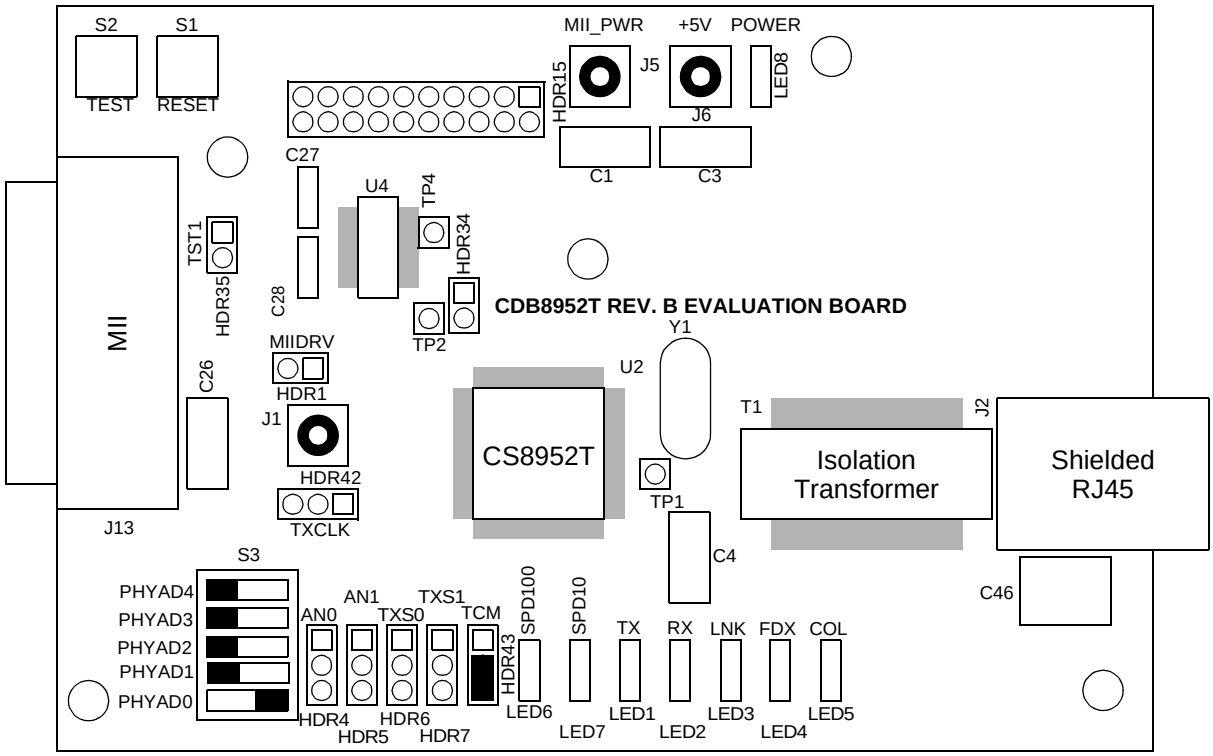
ORDERING INFORMATION

CS8952T-CQ 0° to +70° C	100-pin TQFP
CDB8952T	Evaluation Board

DESCRIPTION

The CDB8952T Evaluation Board provides a platform for evaluating the CS8952T 10Base-T and 100Base-T Transceiver. It is designed to plug into a transceiver test box via a standard 40-pin MII connector. System designers can use the CDB8952T to fully exercise the CS8952T without the time and expense of custom prototyping.

Though the CBD8952T is configured from the factory for 5 V operation with the power supplied from the test box, it may also be configured for 3.3 V MII systems.



INTRODUCTION

This manual provides information specifically on the CDB8952T Evaluation board and generally on any design incorporating the CS8952T CrystalLAN™ 10Base-T and 100Base-T Transceiver.

The reader should have a general knowledge of hardware design and Ethernet operation.

Background Information

- IEEE Std 802.3u-1995 (ISO/IEC 8802.3:1996) CSMA/CD Access Method and Physical Layer Specifications
- IEEE Std 802.3u-1995 Supplement Clause 28 (Auto-Negotiation)
- CS8952T CrystalLAN™ 10Base-T and 100Base-T Transceiver Datasheet

Evaluation Kit Contents

The CDB8952T Evaluation Board Kit includes the following:

Quantity	Item
1	CDB8952T Evaluation Board
1	CS8952T Datasheet
1	CDB8952T Reference Manual
1	CDB8952T Kit Packing List

Table 1. Evaluation Kit Contents

BOARD CONFIGURATION

I/O Connectors

J1 - External TX_CLK. This connector may be used to supply TX_CLK when HDR42 and HDR43 are set appropriately.

J2 - RJ45, Twisted-pair Media (Table 2).

Pin	Function
1	TD+
2	TD-
3	RD+
4	-
5	-
6	RD-
7	-
8	-

Table 2. Twisted-pair Media

J5 - MII Power. When the board is connected to a system that does not supply power through the MII connector, +5 V or +3.3 V must be supplied here.

J6 - CS8952T Core Power. +5 V must be supplied here from either J5 (if +5 V is supplied through the MII connector) or an external power supply.

J13 - MII Connector (Table 3).

Pin	Function	Pin	Function
1	MII Power	21	MII Power
2	MDIO	22	Ground
3	MDC	23	Ground
4	RXD3	24	Ground
5	RXD2	25	Ground
6	RXD1	26	Ground
7	RXD0	27	Ground
8	RX_DV	28	Ground
9	RX_CLK	29	Ground
10	RX_ER/RXD4	30	Ground
11	TX_ER/TXD4	31	Ground
12	TX_CLK	32	Ground
13	TX_EN	33	Ground
14	TXD0	34	Ground
15	TXD1	35	Ground
16	TXD2	36	Ground
17	TXD3	37	Ground
18	COL	38	Ground
19	CRS	39	Ground
20	MII Power	40	MII Power

Table 3. MII Connector

Configuration Jumpers and Switches

S1 - Board Reset. Depressing this push-button switch will force the CS8952T into a reset state.

S2 - Test 1 (not populated). This switch is used to select a factory test mode, and should not be pressed during normal operation.

S3 - Physical Address Select. This 5-position switch is used to select the physical address to which the CS8952T will respond. “Open” or “Off” will set the corresponding physical address bit to ZERO, while “Closed” or “On” will set it to ONE. The CS8952T checks the positions of this switch only during power-up or reset. If any switch position is changed, a reset or power cycle is required before the new settings will take effect.

NOTE: Physical address 00000 is a special broadcast address. All devices will respond to this address in addition to the one selected using S3. Setting S3 to 00000 will cause the CS8952T to set the ISOLATE bit in the Basic Mode Control Register, isolating itself from all MII signals except MDC and MDIO. It will remain isolated until this bit is cleared.

Care should be taken when reading from physical address 00000 when multiple devices reside on the same MII.

HDR1 - MII Drive Select. When this header is left open, the CS8952T MII drivers will conform to the IEEE 802.3u specification. When a shorting cap is installed, the CS8952T MII drivers will be reduced to 4mA.

The CS8952T checks the status of HDR1 only during power-on or reset. A reset or power cycle is required before any changes in this jumper setting will take effect.

HDR4, HDR5 - Auto-Negotiation Select 0 and 1. These headers are used to select the forced or advertised auto-negotiation modes as indicated in Table 4.

HDR5 (AN1)	HDR4 (AN0)	Speed	Forced/ Auto	Full/Half Duplex
pins 2-3 shorted	open	10	Forced	Half
pins 1-2 shorted	open	10	Forced	Full
open	pins 2-3 shorted	100	Forced	Half
open	pins 1-2 shorted	100	Forced	Full
open	open	100/10	Auto	Full/Half
pins 2-3 shorted	pins 2-3 shorted	10	Auto	Half
pins 2-3 shorted	pins 1-2 shorted	10	Auto	Full
pins 1-2 shorted	pins 2-3 shorted	100	Auto	Half
pins 1-2 shorted	pins 1-2 shorted	100	Auto	Full

Table 4. Auto-Negotiation Select

The CS8952T checks the status of HDR4 and HDR5 only during power-on or reset. A reset or power cycle is required before any changes in these jumper settings will take effect.

HDR6, HDR7 - Transmit Slew Rate Select 0 and 1. These headers are used to select the rise and fall times of the 100BASE-T transmitter output waveform as indicated in Table 5.

HDR7 (TXSLEW1)	HDR6 (TXSLEW0)	Rise/Fall Time
pins 2-3 shorted	pins 2-3 shorted	0.5 ns
open	pins 2-3 shorted	1.0 ns
pins 1-2 shorted	pins 2-3 shorted	1.5 ns
pins 2-3 shorted	open	2.0 ns
open	open	2.5 ns
pins 1-2 shorted	open	3.0 ns
pins 2-3 shorted	pins 1-2 shorted	3.5 ns
open	pins 1-2 shorted	4.0 ns
pins 1-2 shorted	pins 1-2 shorted	4.5 ns

Table 5. Transmit Slew Rate

HDR15 - Table 6 describes the effect of shorting the listed pin pairs.

HDR34 - Test 0. This header is for factory test purposes only, and should be left open for normal operation.

HDR35 - Test 1. This header is for factory test purposes only, and should be left open for normal operation.

HDR42 - TX_CLK Source Select. This header, in conjunction with HDR43, is used to select the TX_CLK source. When pins 1 and 2 are selected, TX_CLK is supplied from the CS8952T CLK25 output. When pins 2 and 3 are shorted, TX_CLK is supplied externally from J1. When no shorting cap is installed, HDR43 must be configured so that TX_CLK is an output from the CS8952T.

NOTE: No shorting cap should be installed on this header when TX_CLK is configured as an output (see HDR43).

HDR43 - TX_CLK Mode Select. (Table 7)

The CS8952T checks the status of HDR43 only during power-on or reset. A reset or power cycle is required before any changes in this jumper setting will take effect.

Pins	Function	Description
1-2	Low Power Start	The CS8952T will enter a low power mode following reset. Only the circuitry necessary to maintain media impedance and the MII Serial Management Interface will be operational. The CS8952T checks the status of these pins only during power-on or reset. A reset or power cycle is required before any changes in this jumper setting will take effect.
3-4	MII Receive Enable	MII signals RXD[3:0], RX_CLK, RX_DV, and RX_ER are tristated.
5-6	Power Down	The CS8952T is forced into a low power mode. Only the circuitry necessary to maintain media impedance will be operational.
7-8	CRS Mode Control	The CRS pin will be asserted for receive activity only. The CS8952T checks the status of these pins only during power-on or reset. A reset or power cycle is required before any changes in this jumper setting will take effect.
9-10	Open	Not connected
11-12	Bypass 4B/5B Coders	The 4B5B encoder and decoder are bypassed and 5-bit code groups are used. RX_ER is used as the fifth receive bit, and TX_ER as the fifth transmit bit. The CS8952T checks the status of these pins only during power-on or reset. A reset or power cycle is required before any changes in this jumper setting will take effect.
13-14	Bypass Symbol Alignment	4B5B coders and scramblers are bypassed and the CS8952T will make no attempt to identify code-group boundaries. Data on RXD[4:0] and TXD[4:0] may contain bits from two code groups. The CS8952T checks the status of these pins only during power-on or reset. A reset or power cycle is required before any changes in this jumper setting will take effect.
15-16	Loopback	The CS8952T will be place in loopback mode. When operating in 100 Mb/s mode, the loopback will be inside the PMD block. When in 10 Mb/s mode, the CS8952T will perform a local ENDEC loopback.
17-18	MII Isolate	The CS8952T will exit from reset with all MII signals tristated except MDIO and MDC. The CS8952T checks the status of these pins only during power-on or reset. A reset or power cycle is required before any changes in this jumper setting will take effect.
19-20	10BASE-T Serial Mode	If the CS8952T is in 10 Mb/s mode, data is transferred serially on RXD0 and TXD0, and the full MII interface is disabled. When the CS8952T is in 100Mb/s mode, shorting these pins has no effect. The CS8952T checks the status of these pins only during power-on or reset. A reset or power cycle is required before any changes in this jumper setting will take effect.

Table 6. Effect of shorting the listed pin pairs

HDR43	TX_CLK pin	CLK25 pin
pins 1-2 shorted	input	25 MHz clock
open	input	not used
pins 2-3 shorted	output	not used

Table 7. TX_CLK Mode Select

NOTE: When TX_CLK is an input, a shorting cap must installed on HDR42 to supply TX_CLK to the CS8952T (see HDR42).

LED Indicators

LED1 - Transmitter Active Indicator.

LED2 - Receiver Active Indicator.

LED3 - Link OK Indicator.

LED4 - Full Duplex Indicator.

LED5 - Collision Indicator.

3.3V Power Supply Option

Outlined below are several different way to supply power to the CDB8952T evaluation board.

5 V Supplied Through the MII Connector - When the CDB8952T is connected to a system which supplies +5 V through the MII connector, J5 and J6 may be connected together via a short cable. Alter-

natively, J6 may be connected to an external +5 V supply and J5 left unconnected.

NOTE: Under no circumstances should J5 be connected to an external power supply if power is also supplied through the MII connector.

3.3V Supplied Through the MII Connector - When the CDB8952T is connected to a system which supplies +3.3 V through the MII connector, J6 must be connected to an external +5 V supply and J5 left unconnected.

No Power Supplied Through the MII Connector - When the CDB8952T is connected to a system which does not supply power through the MII connector, J5 and J6 may both be connected to a single external +5 V supply. Alternatively, J5 may be connected to an external +3.3V supply and J6 to an external +5 V supply.

BOARD ASSEMBLY NOTES

Magnetics Vendors

Vendor	Part Number
Bel Fuse Inc. 198 Van Vorst St. Jersey City, NJ 07302 (201) 432-0463 www.belfuse.com	S558-5999-46
Halo Electronics, Inc. P.O.Box 5826 Redwood City, CA 94063 (650) 568-5800 www.haloelectronics.com	TG22-3506ND
Pulse Engineering, Inc. 12220 World Trade Dr. San Diego, CA 92128 (619) 674-8100 www.pulseeng.com	PE-68515

Crystal Vendors

Vendor	Part Number
Raltron Electronics Corp. 10651 NW 19th St. Miami, FL 33172 (305) 593-6033 www.raltron.com	AS-25.000-15-F- EXT-SMD-TR-CIR

SCHEMATICS

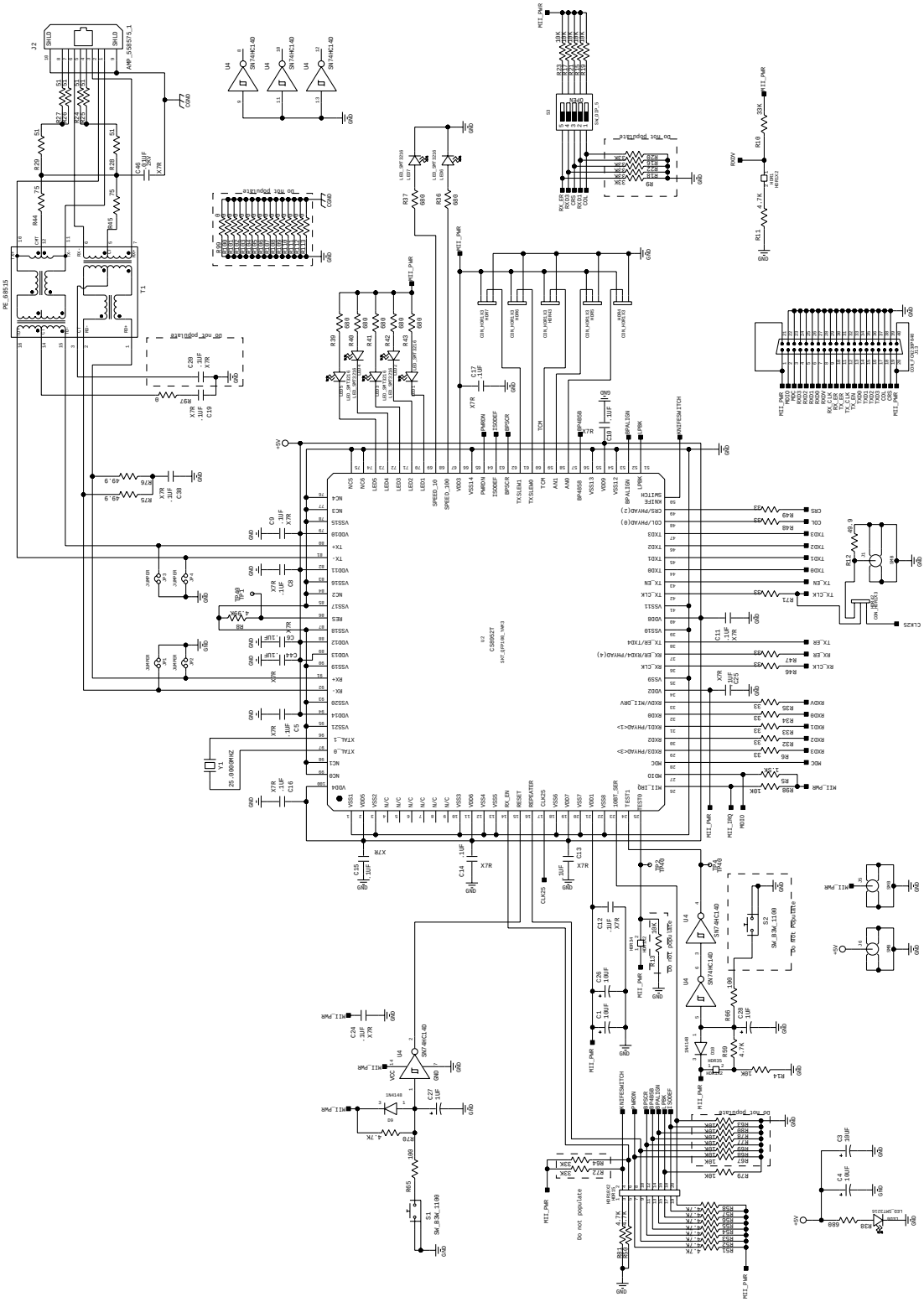


Figure 1. Schematic

CDB8952T BILL OF MATERIALS

Ref. Des.	Description	Manufacturer	Part Number
C1, C3, C4, C26	Cap, Tant, 10uF, 20V, 20%, 6032	Kemet	T491C106M020AS
C5, C6, C8-C17, C19, C20, C24, C25, C38, C44	Cap, X7R, 0.1uF, 50V, 10%, 0805	Kemet	08055C104KAT2A
C27, C28	Cap, Tant, 1uF, 20V, 20%, 3216	Kemet	T491A105M020AS
C46	Cap, X7R, 0.01uF, 2KV, 20%, 2225	AVX	2225GC103MA11A
D9, D10	Diode, BAS16LT1, SOT23	Motorola	BAS16LT1
HDR1, HDR34, HDR35	Header, 2x1, 0.1” centers		
HDR4-HDR7, HDR42, HDR43	Header, 3x1, 0.1” centers		
HDR15	Header, 10x2, 0.1” centers		
JP1, JP2, JP3, JP4	Socket, 2x1, 0.1” centers	Samtec	SS-102-G-22
J1, J5, J6	Conn, SMB	Amp	413990-1
J2	Conn, RJ45, shielded	Amp	558575-1
J13	Conn, D Shell, 40 pin, High Density	Fujitsu	FCN238P040-G/S
LED1-LED8	LED, Green, SMT	Panasonic	LN1351C-TR
R5	Res, 1.5KΩ, 5%, 1/10W, 0805	Bourns	CR0805-JX-152-E
R6, R32-R35, R46-R49, R71	Res, 33Ω, 5%, 1/10W, 0805	Bourns	CR0805-JX-330-E
R8	Res, 4.99KΩ, 1%, 1/10W, 0805	Bourns	CR0805-FX-4991-E
R9-R10, R16, R18, R20, R22, R64, R72	Res, 33KΩ, 5%, 1/10W, 0805	Bourns	CR0805-JX-333-E
R11, R50-R59, R70, R81	Res, 4.7KΩ, 5%, 1/10W, 0805	Bourns	CR0805-JX-472-E
R12, R75-R76	Res, 49.9Ω, 1%, 1/10W, 0805	Bourns	CR0805-FX-49R9-E
R24-R29	Res, 51Ω, 5%, 1/10W, 0805	Bourns	CR0805-JX-510-E
R36-R43	Res, 680Ω, 5%, 1/10W, 0805	Bourns	CR0805-JX-681-E
R44, R45	Res, 75Ω, 5%, 1/10W, 0805	Bourns	CR0805-JX-750-E
R97, R99-R113	Res, 0Ω, 1A, 0805	Bourns	CR0805-JX-000-E
R65, R66	Res, 100Ω, 5%, 1/10W, 0805	Bourns	CR0805-JX-102-E
R13-15, R17, R19, R21, R23, R63, R67-R69, R77-R80, R98	Res, 10KΩ, 5%, 1/10W, 0805	Bourns	CR0805-JX-103-E
S1, S2	Switch, NO Push-button	C&K	PTS645TL50
S3	Switch, 5-position DIP	CTS	CTS208-5
TP1, TP2, TP4	Testpoint		
T1	Transformer, Isolation	Halo	
U2	IC, CS8952T, TQFP100	Cirrus	CS8952T-CQ
U4	IC, 74HC14, SO14	TI	SN74HC14D
Y1	Xtal, 25.00MHz, HC49U	See Page 5	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