10/9/2001

Errata: CS89712 Rev. B

(Reference CS89712 Data Sheet revision DS502PP2 dated FEB '01)

1. CACHE AND SDRAM INTERACTION

Problem Description

If the cache is not turned on for all SDRAM bus cycles, an internal bus arbitration problem may occur. This condition will cause the executing code running out of SDRAM to abort.

Workaround

Both MMU and cache must be enabled for systems which include SDRAM.

Status

Correct operation will be documented in the next revision of the Data Sheet and User's Manual.

2. SINGLE 32-BIT EXTERNAL SDRAM DEVICE UNSUPPORTED

Problem Description

When interfacing to a single 32-bit external SDRAM, the column address is never presented.

Workaround

Configure the SDRAM controller as two 16-bit SDRAM devices providing a 32-bit wide bus. The memory controller will then allow access to all memory locations, however the memory will not be contiguous as the bank select pins will be configured for two 16-bit external memory devices and not one 32-bit external memory device.

Using a debugger or the Angel monitor, access all memory locations to determine the physical location of the memory. Due to the internal bank selects, the physical memory may not be contiguous. If the memory is non-contiguous, program the MMU to translate the non-contiguous physical memory to contiguous virtual memory.

Status

To be fixed in the Rev. C silicon version.

3. MULTIPLE LOAD/STORE TO 16-BIT SDRAM ARRAY

Problem Description

When performing a load multiple or store multiple of two or more words using 16-bit SDRAM on a non-biword aligned address, the word data order will be swapped.

Workaround

For routines which use load or store multiple accesses, place that data array in on-chip memory (i.e. place the stack pointer in internal SRAM).

Status

To be fixed in the Rev C. silicon version.

4. LCD FRAME BUFFER STORED IN 16-BIT EXTERNAL SDRAM

Problem Description

When using 16-bit wide SDRAM for the frame buffer, the data may be rearranged.

Workaround

1) Do not perform any half-word or byte accesses.

2) Use two 16-bit SDRAM devices to generate a 32-bit wide bus.

Status

To be fixed in the Rev C. silicon version.

Please email questions concerning this information to ethernet@crystal.cirrus.com