11/16/00

Errata: CS61584A Revision E

(Reference CS61584A Data Sheet revision DS261PP4 dated JAN '99)

This document lists the errata for Revision E of the CS61584A device, and describes the differences between Revision E and the referenced Data Sheet.

1. Quartz Crystal Loading Issue

The load presented to the quartz crystal, across the pins 1XCLK/XTALOUT (pins 28/27, TQFP) is around 31 pF instead of 19 pF. This can make the quartz crystal run at frequencies up to 1.5 kHz lower than the nominal 12352/16384 kHz frequencies. The result is the frequency of RCLK (in the absence of input data and REFCLK oscillator), and the TAOS signal (blue alarm or all ones), will be lower than the expected T1/E1 frequency by up to 160 Hz. A work around is to add series capacitance to the quartz crystal, thus reducing the total loading; or using a crystal that runs at its nominal frequency with a 31 pF load, instead of 19 pF. If an external oscillator is being used to drive REFCLK, then this problem does not appear.

2. Status Register Read Issue

The first time that either Status register is read after a power up returns invalid results. This can be worked around by reading the status registers twice on the first read after the device has been powered up.

3. Invalid Saturation Interrupt Issue

The status register will indicate an Overflow condition when certain pre-stored waveforms are used. Some pre-stored waveforms use the maximum amplitude for their peak, which triggers the Overflow detector. This is an invalid error indication, since the pre-stored waveforms are specifically designed to not cause an overflow. There will also be an interrupt unless the Overflow bit is set in the Mask register. The recommended work around is to mask off the interrupt and ignore the Overflow bit in the Status register when pre-stored waveforms are used.

4. JTAG Reset Issue

The JTAG interface is reset by power-up reset and by the Reset pin. It should only be reset by holding the TMS pin low for five cycles of TCLK. Holding TMS low for five TCLK cycles also resets the JTAG circuitry. This can be worked around by resetting the part only during operation, not while the device is undergoing JTAG testing.

5. Parallel Port Issue

When in Intel or Motorola parallel port mode, the revision E device responds to reads and writes on the data bus independent of the state of CS. For a given memory access, if AD[7:4] = SAD[7:4] and AD[3:0] = 0xY8 or 0xY9, the device drives the data bus on a read cycle and writes data to its internal RAM on a write cycle. (See the data sheet for an explanation of the memory address notation.) The work around for this problem is to use external logic to gate the

ALE/AS signal to the CS61584A so that it doesn't latch the address unless it is the device to be accessed.

The device revision is the letter before the 4-digit assembly date code in the second line of the package marking.

For inquiries regarding this errata, please contact your local sales office, distributor, or representative. A list of these offices may be found at http://www.cirrus.com or by calling:
1 (800) 888-5016