Techniques to Measure and Maximize the Performance of a 120 dB, 24-bit, 96 kHz A/D Converter Integrated Circuit

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In order to realize maximum performance from an A/D converter chip, many subtleties must be addressed in the external environment in order to make sure that the performance is not degraded. This paper briefly describes the architecture of an example A/D converter, discusses some trade-offs in the external circuit design and concludes with some measurement issues and results. The techniques discussed also form a basis for users' own designs, allowing predictable realization of maximum performance.

1. INTRODUCTION

Analog-to-Digital (A/D) converter integrated circuits continue to improve their performance as new techniques and processes become available. In order to realize the potential performance of such devices, the external environment around the device must be carefully designed. This paper addresses a myriad of design issues including input buffer design, noise analysis, ground planes, clocking methods to reduce jitter, decoupling capacitor values and type, power supply arrangements, various digital to analog coupling mechanisms, and the impact of using sockets. In addition, various measurement subtleties are addressed including distortion cancellation, isolation and laboratory environmental conditions. The conclusion of the paper is that with careful attention to external environment details, integrated circuit A/D converters can easily yield their maximum performance. By following the techniques described in this paper, equipment designers can maximize the performance of their products, benefiting the entire audio community.

2. A/D CONVERTER ARCHITECTURE

The A/D Converter utilized for this discussion consists of an analog delta sigma modulator die, along with a digital filter die, housed in a single 28-pin SOIC plastic package. Figure 1 shows the block diagram of the device. Highlights of the delta-sigma modulator design include the use of a tri-level modulator which yields excellent linearity after calibration, a novel coding scheme for the modulator output data which removes data dependent variations in the number and polarity of data signal edges, and a fully differential design which yields low distortion and good common mode rejection. The decimation filter includes multiple word length output options, with optional psychoacoustic noise shaping. Also included is a low group delay output for real time use. References [1] and [2] describe the A/D converter architecture in great detail.

3. INPUT BUFFER DESIGN

The input buffer circuit for the A/D converter has to meet several stringent requirements. These include: negligible noise contribution, DC level shifting from an input signal typically centered at zero volts to an output signal centered at the common mode voltage of the A/D converter; isolation of the buffer amplifier from switched capacitor current transients while maintaining a low output impedance so as not to cause distortion and providing anti-alias filtering appropriate for the modulator sample rate.

Figure 2 shows the servo-balanced differential input buffer circuit selected for this application. This circuit supplies the required differential output with either a differential or a single-ended signal of either polarity at the input terminals. The gain structure of the input buffer was designed to attenuate a 24.5 dBu (13 Vrms) input signal to the 5.2 dBu (1.414 Vrms) required to produce a 0 dBFS digital output. The 6 dB attenuation in the buffer input structure is followed by the resistive network at the A/D converter input (Section 3.3) which supplies the additional 13.3 dB attenuation.

3.1 Input Buffer Noise Requirements and Analysis

The noise contribution of an optimal input buffer would be insignificant to the noise generated by the A/D converter and allow the system noise to be dominated by the A/D converter. It is therefore desirable to quantify the noise contribution of the A/D converter, the input buffer and the resulting system noise.

3.1.1 A/D Converter Noise Calculation

The equivalent RMS noise of the A/D converter, n_{adc}, over a 20 kHz bandwidth can be calculated as follows:

$$n_{adc} = \frac{V_{fs}}{10^{\left(\frac{DR_{adc}}{20}\right)}} = 1.997\ \text{mV}$$

Where V_{fs} is the rms voltage of a sine-wave that will produce a full-scale digital output and DR_{adc} is the unweighted dynamic range of the converter over a 20 kHz bandwidth. For this example, V_{fs} is equal to 1.414 Vrms and DR_{adc} is equal to 117 dB [6]. This calculation gives an equivalent rms A/D converter noise of 1.997 μV.

3.1.2 Input Buffer Noise Analysis

The analysis of the input buffer noise can be separated into differential and common mode noise. The analysis of differential noise contributed by the resistive and active components in the buffer circuitry is shown in Figure 3. The input 2-to-1 resistive network at the XLR connector input contributes 8.0 nV/√Hz, and the unity gain configured amplifier contributes 5.2 nV/√Hz. The noise at the output of

the buffer amplifier is about 9.5 nV/√Hz. The resistive network at the A/D converter input attenuates the noise contributed by the buffer by 13.3 dB and contributes 0.8 nV/√Hz of noise. Therefore, the total noise from the buffer network is 2.2 nV/√Hz at each input of the A/D converter and the combined differential noise is 3.1 nV/√Hz (441 nV over the 20 kHz bandwidth).

The analysis of common-mode noise contributed by the resistive and active components, including the servo network, in the buffer circuitry is shown in Figure 4. At the input of the A/D converter, the total common-mode noise from the buffer network is 31.5 nV/√Hz. However, the common-mode rejection of the A/D converter further suppresses this noise by 82 dB. Therefore, the resulting common-mode noise into the A/D converter is 2.5 pV/√Hz (354 pV over a 20 kHz bandwidth). Note that the common-mode rejection of the input buffer and this common-mode analysis is largely determined by the matching of the input buffer components which should be at least 1% tolerance.

3.1.3 System Noise Calculation

The total system noise (n_{total}) is the RMS sum of the converter noise and the buffer noise and can be calculated as follows:

$$n_{total} = \sqrt{n_{adc}{}^2 + n_{diff}{}^2 + n_{cm}{}^2} = 2.045\,\mu V$$

Therefore, the system dynamic range (DR_{total}) is equal to

$$DR_{total} = 20\log\left(\frac{V_{fs}}{n_{total}}\right) = 116.8\ dB$$

This shows that the input buffer circuit degrades the noise performance of the A/D converter by only 0.2 dB, yielding an overall system dynamic range of 116.8 dB.

3.2 DC Level Shifting of the Input Signal

To achieve the optimum THD+N performance, the A/D converter requires that the inputs are biased to a DC level within 10 mV of the internal common mode voltage. The common-mode bias voltage of the buffer circuit (V_{CM}) is derived from the VCOM output of the A/D converter, pin 2, and buffered using an OPA2132 op-amp, U15, as shown in Figures 2 and 5. The buffer is used to minimize the susceptibility to contamination of the common-mode voltage within the A/D converter. Notice that the location of the buffer in relation to the VCOM filter capacitors and pin 2 of the A/D converter minimizes the trace length attached to the A/D converter. Since the servo-amplifier network is shared by the differential signal paths, any resistive and active components in the network do not contribute differential noise to the output of the buffer circuit as discussed in 3.1.3.

3.3 Buffer Isolation and Anti-Alias Network

The front-end of the A/D modulator is implemented with a switched sampling capacitor as shown in Figure 6. A 71 pF capacitor is initially charged from the analog input with respect to the common-mode voltage. The sampling is completed by connecting the capacitor to an internal common-mode node and the modulator loop filter. This sequence is repeated at a rate of 6.144 MHz. Most commercially available amplifiers are unable to settle this large instantaneous switched-capacitor current at this frequency. As a result, linearity performance of the amplifier is degraded and some amplifiers may even become unstable. The RC network serves to isolate the buffer amplifiers from the switched capacitor input of the A/D converter and provides a charge reservoir for the internal sampling capacitor, thus allowing the amplifier to deliver rated linearity. However, a non-linear switched-capacitor current, originating from the signal dependent charge injection of MOS switches, exists which can react with the source impedance seen by the A/D converter to create distortion. This imposes an upper limit to the impedance of the RC attenuator. A source impedance less than 50 ohms does not significantly degrade the linearity performance of the A/D converter and still provides sufficient isolation between the buffer amplifier and the converter.

The components which meet the need for buffer isolation and a charge reservoir for the sampling capacitor also provide a single pole anti-alias filter. It is a general “rule-of-thumb” for the corner frequency of this filter to be located a decade below the sampling frequency of the modulator. Precision applications may also require that the input impedance of the A/D converter, 2.25 kohms at a modulator sampling rate of 6.144 MHz, be considered in the derivation of the resistive voltage divider. The previously discussed requirements of the RC network are: a source impedance less than 50 ohms, attenuation of the signal by 13.3 dB and a corner frequency one decade below the modulator sampling frequency. These requirements lead to the values shown in Figure 2.

3.4 Input Buffer Layout

It is important to preserve complete symmetry in the layout of each differential stage, as well as between left and right channels as shown in Figures 7- 9. Notice the close proximity of the differential input traces to minimize any differential noise pickup and the placement of the Vcm buffer op-amp very close to pin 2 of the A/D converter to minimize the length of the trace attached to pin 2.

4. EXTERNAL SUPPORT CIRCUIT DESIGN

The performance of the A/D converter can be degraded by poor design of the external environment. This section describes the immediate environment around the A/D converter, including ground plane recommendations, decoupling capacitor choices, the correct clock generator connections and over-voltage protection.

4.1 Ground Plane Issues

Harris [3] has previously discussed how ground planes are used to reduce digital signal emissions, reduce input susceptibility to emissions and control the current flow. Of particular concern is the reduction of unwanted current flow in the vicinity of the input signal traces. To this end, the system is designed to ensure that only signal currents are required to flow between the analog and digital regions. Separate analog and digital power supplies are configured to ensure that power supply currents remain in either the analog or digital regions. This technique simplifies the analysis of currents between the separate regions. The analog and digital grounds are joined under the A/D converter to minimize the loop area of the return currents from the analog die digital outputs driving the digital die signal inputs as shown in Figure 9.

4.2 Decoupling Capacitors

With a master clock frequency as high as 25 MHz, good power supply decoupling becomes mandatory. The parallel combination of a low value capacitor, mounted very close to the pin being decoupled, along with a higher value capacitor, has been shown to be most effective. The low value capacitor supplies the high frequency transient currents, while close mounting minimizes the series inductance, and minimizes the loop area of the transient current flow. The use of surface mount capacitors is essential. Such capacitors should be mounted on the same side of the board as the A/D converter package, thereby eliminating the inductance of vias in the decoupling path. The Vref decoupling capacitor is particularly critical, and should be mounted very close to pins 1 and 3. The use of a socket for the A/D converter package is not recommended, since extra inductance will inevitably be added between the decoupling capacitors and the die.

4.3 Clock Generation

The clock source for the A/D converter should have low jitter to minimize the risk of raising the noise floor or introducing tones [4]. In previous designs, the clock oscillator has been mounted in the digital region of the board and run from the digital +5V supply. In this design, the clock oscillator is run from the clean analog supply and is mounted in the analog region of the board. The clean supply minimizes the jitter induced through supply noise. Any clock oscillator noise induced on the analog supply or ground connections should only cause a DC offset in the A/D converter, since such noise would be completely synchronous to the operation of the converter.

4.4 Over-voltage Protection

Previous recommendations for over-voltage protection for a CMOS A/D converter have included using inverting configuration buffer amplifiers running from the same supply as the A/D converter, or using schottky diodes [5]. These approaches are not required in this case since improvements have been made in the latch-up immunity of CMOS circuits. These improvements, plus the use of 182 ohm series resistors, results in a design that is very robust. Even if the output of both op-amps were to clip at -12V,

the resulting 66 mA of current would not cause the input of the A/D converter to be damaged, or induce a latch condition in the A/D converter. Therefore no special over-voltage precautions are needed.

4.5 Power Supplies

In order to provide as clean an environment as possible for the A/D converter, several independent supplies are used. The input buffer amplifier is run from +12V and -12V analog supplies, referenced to analog ground. A separate +5V analog supply runs the analog die in the A/D converter, the Vcom buffer amplifier, the clock oscillator and, via an RC filter, the digital sections in the analog die. The digital die is operated from a completely independent +5V digital supply, referenced to digital ground. Ferrite beads are used in strategic locations to isolate different parts of the circuit [6].

4.6 High Frequency Contamination

It has been shown that contamination of the reference voltage can degrade system performance [3]. A very similar situation exists with the common-mode voltage on this converter since the reference voltage is derived from the VCOM voltage. Even a very slightly coupling of high frequency contamination into the voltage reference demodulates high frequency quantization noise into the baseband. Typically, these pins are adequately protected by a large low frequency decoupling capacitor and a small high frequency decoupling capacitor and care should be exercised in the location of these filter capacitors.

An unusual effect has been noticed in the output spectrum of the A/D converter when no input signal is present [2]. The noise floor, while being evenly distributed across the audio band, can take on an uneven appearance called scalloping (Figure 11). The cause appears to be a coupling of the serial data output line transitions into the external analog input circuitry. Scalloping does not occur if the A/D converter input is internally shorted, thus indicating an external coupling mechanism. This effect can be removed in a number of ways. Slowing down the edges of the serial data output of the digital die eliminates the effect. This can be done by the addition of ferrite beads in the serial data output lines [6]. Alternatively, decoupling the digital die very close to the supply pin reduces the effect. A third method of removing this effect is to add a small digital offset to the output data prior to driving the output data pins. This shifts the data chatter, which results from random noise, from the region that includes the 2's complement transition from 0 to -1. This transition of the data bits from all zero's to all one's appears to be a factor in causing the scalloping. Such a digital offset can be easily removed in subsequent processing. A control bit allows users to add the offset if desired.

5. TEST SET-UP DESCRIPTION

Figure 12 shows the main components of the test set-up. The goal of this set-up is to provide as favorable an environment as possible, allowing the A/D converter to deliver its best possible performance. An Audio Precision System Two is used as an analog test signal generator, and to confirm some of the measured results at 48 kHz sample rate. A PC is used to both control the A/D

converter via its control port, and also to collect A/D converter output data at 96 kHz. Custom software running on the PC allows control of the A/D converter and FFT analysis of the output data.

Extensive use of TOS link style fiber optic cable provides complete isolation of the PC from the A/D converter. These cables are preferred over traditional opto-couplers to reduce the coupling capacitance across the isolation barrier to insignificance. This helps ensure that only signal currents flow in the cable from the System Two signal generator to the A/D converter.

6. EXAMPLE RESULTS

Figure 13 shows an example FFT plot, illustrating the 120 dB dynamic range and >105 dB THD+N performance.

6.1 Practical Measurement Hints

To achieve the results shown, various practical techniques were used. All nearby equipment was turned off to ensure an electrically quiet environment. Occasionally, single discrete tones were evident. Changing the resolution, and therefore the scan rate, of nearby PC monitors, would cause the tones to move, identifying the source of the problem. Turning off the monitors while capturing data eliminated the tones. Since the A/D converter test board contained a buffer memory, the PC controlling the A/D converter can be turned off while capturing data, removing a local asynchronous noise source. The test board containing the A/D was not mounted in a metal enclosure. This would be a sensible addition to the set-up.

An excellent test of maximum dynamic range is to use the input shorting capability of the A/D converter input circuitry. A software controllable bit allows the analog inputs to be disconnected from the external circuitry, and internally shorted, thereby resulting in the lowest possible input signal and noise. This test also measures the added noise pickup of the external circuitry by comparing the internal short noise floor to the noise floor obtained by shorting the input to the external buffer.

The non-linearity of the A/D converter is extremely low. The non-linearity in the signal source is also extremely low. Under these circumstances, a non-linearity in the output FFT could be caused by a non-linearity in the A/D converter or in the input test sine wave. It is impossible to tell which is the cause of the residual distortion. In addition, non-linearity cancellation can occur. If the shape of the non-linearity of the A/D converter just happens to be opposite to the shape of the non-linearity of the signal source, then a very good FFT plot will be seen, with much reduced distortion components. Experimenting with different signal generators, and different examples of the A/D converter device, can lead to a better understanding of which distortions originate where.

7. CONCLUSION

Various techniques have been shown which allow the maximum performance of an integrated A/D converter to be realized. In addition, by rigorously applying noise analysis, circuit design, grounding,

isolation and layout techniques, the performance of the A/D converter has been verified. These guidelines also form a basis for users of the device to realize similar levels of performance.

ACKNOWLEDGEMENTS

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REFERENCES

[1] A 120 dB Dynamic Range, 96 kHz, Stereo 24-bit Analog-to-Digital Converter by Kafai Leung, Sarah Zhu, Ka Leung, Eric Swanson. Presented at the 102nd AES Convention, Munich, March 1997

[2] A 5V, 118 dB Delta Sigma Analog-to-Digital Converter for Wideband Digital Audio by Ka Y. Leung, Eric J Swanson, Kafai Leung, Sarah S. Zhu. Presented at ISSCC February 1997, paper FP 13.6

[3] How to Achieve Optimum Performance from Delta-Sigma A/D & D/A Converters by Steven Harris, JAES, Volume 41, Number 10, October 1993

[4] The Effects of Sampling Clock Jitter on Nyquist Sampling Analog-to-Digital Converters, and on Oversampling Delta-Sigma ADC's by Steven Harris, JAES, July 1990.

[5] ADC Input Buffer and Protection Techniques, Steven Green, AN20, February 1992, Crystal Semiconductor.

[6] CS5396/7 and CDB5396/7 data sheet, Crystal Semiconductor, 1997.

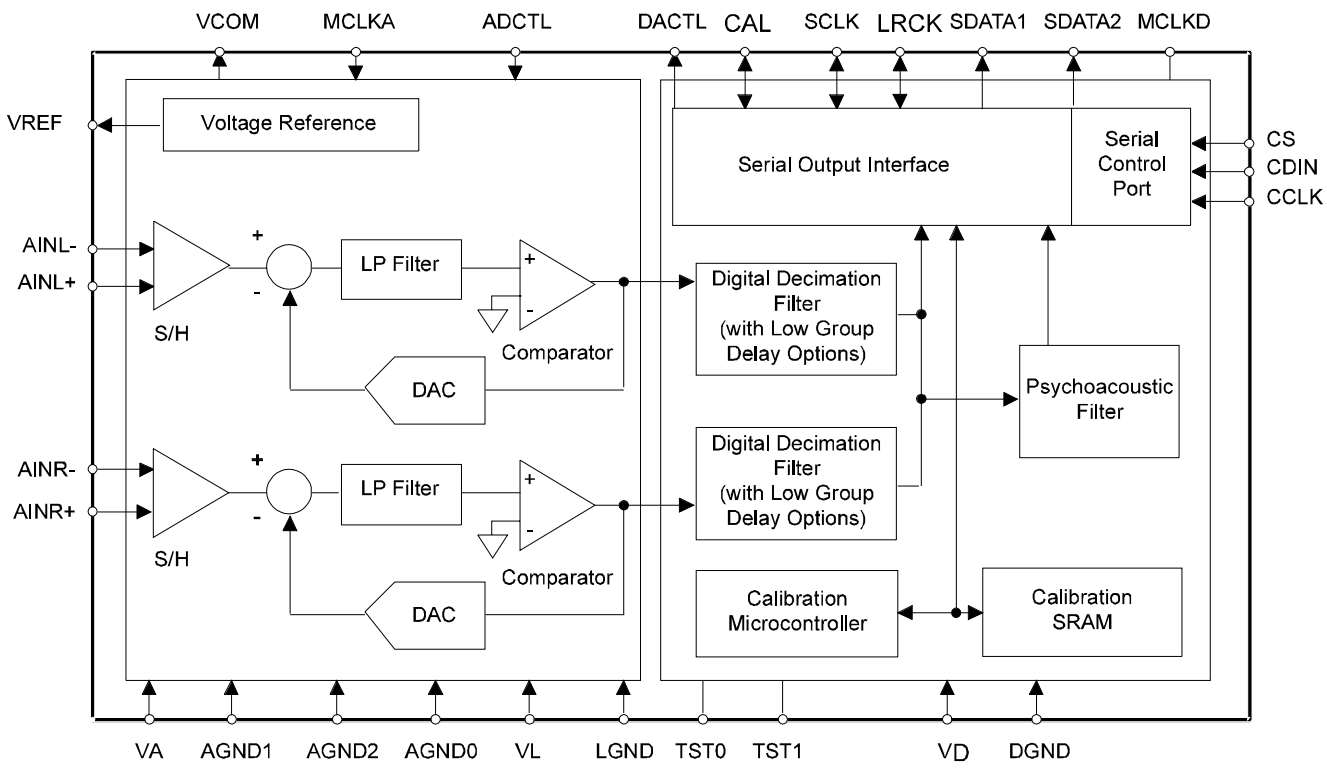


Figure 1. A/D Converter Block Diagram

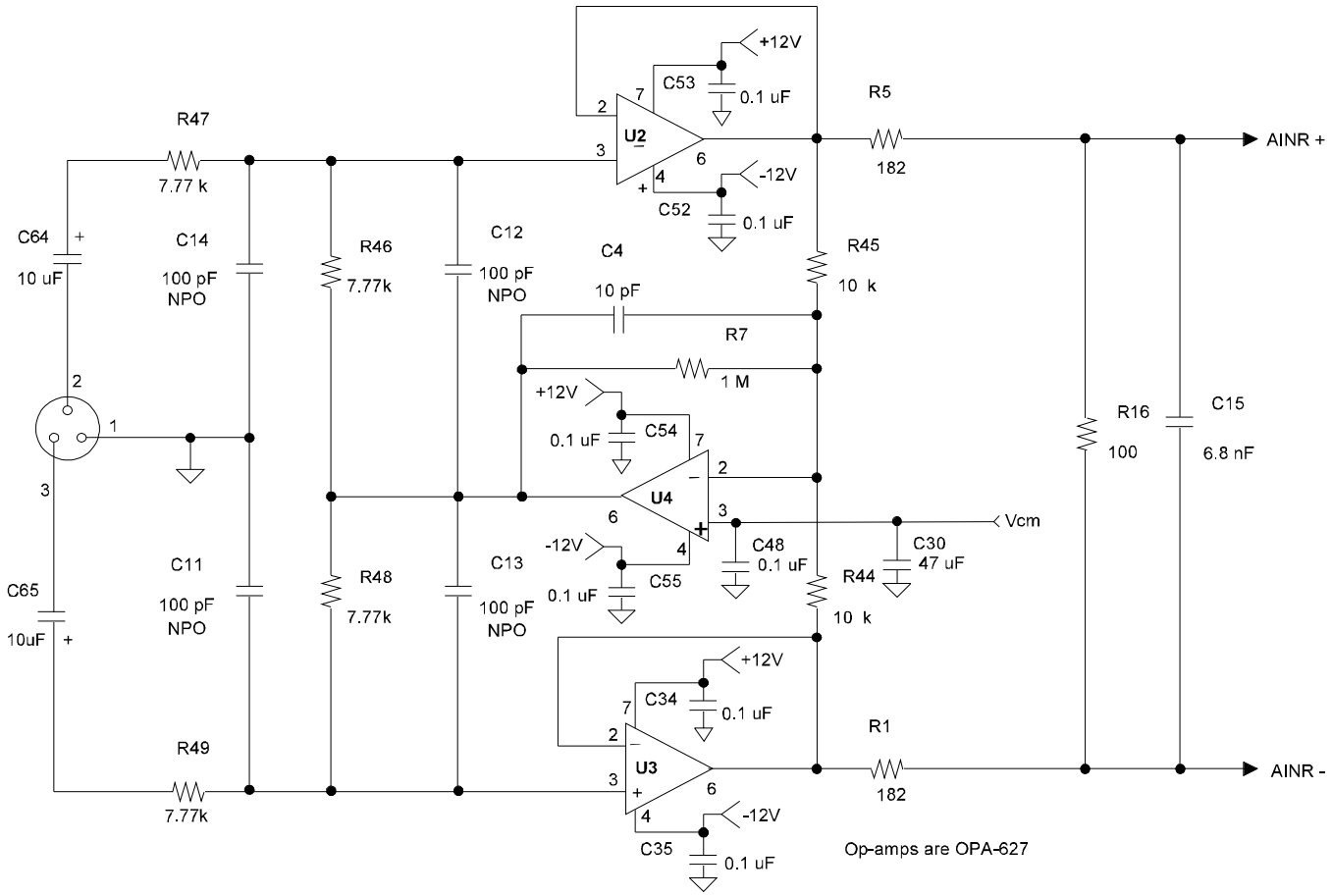
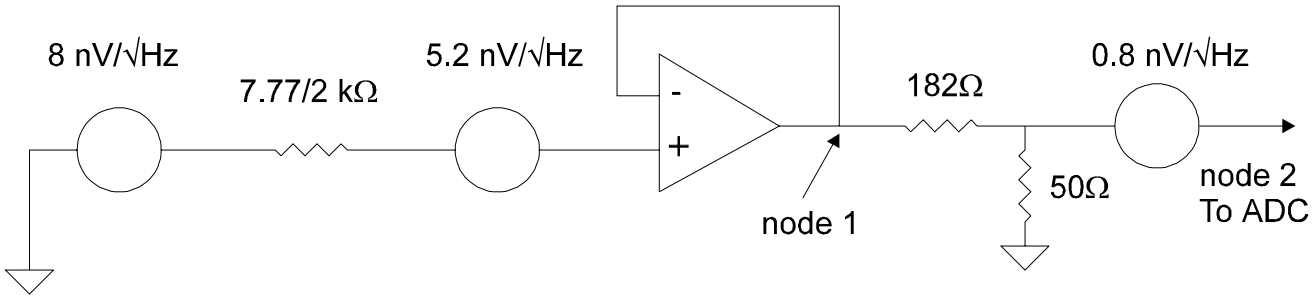


Figure 2. Input Buffer Circuit Diagram

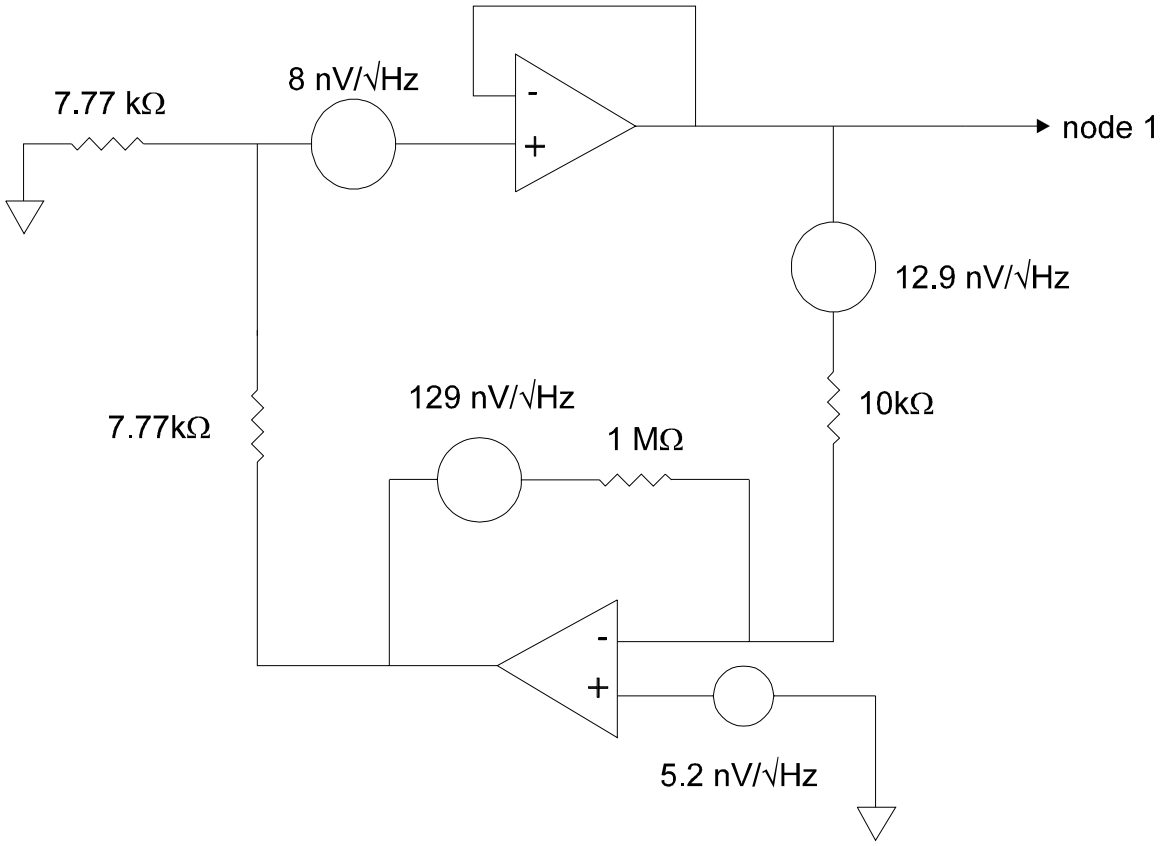


node 1: $e_n = \left(8^2 + 5.2^2\right) = 9.5 \text{nV}/\sqrt{\text{Hz}}$

node 2: $e_n = \sqrt{\left((9.5 \times 50)/(182+50)\right)^2 + 0.8^2} = 2.2 \,\text{nV}/\sqrt{\text{Hz}}$

Differential voltage noise $= 2.2 \text{ nV}/\sqrt{\text{Hz}} \times \sqrt{2} = 3.1 \text{ nV}/\sqrt{\text{Hz}}$

Figure 3. Input Buffer Differential Noise Analysis



node 1: $e_n{}^2 = (12.9 \times 1.96)^2 + (129/51)^2 + (8 \times 1.96)^2 + (5.2 \times 1.98)^2$

$e_n = 31.5\ \text{nV}/\sqrt{\text{Hz}}$

Common mode voltage noise $= 31.5\ \text{nV}/\sqrt{\text{Hz}}$

Figure 4. Input Buffer Common Mode Noise Analysis

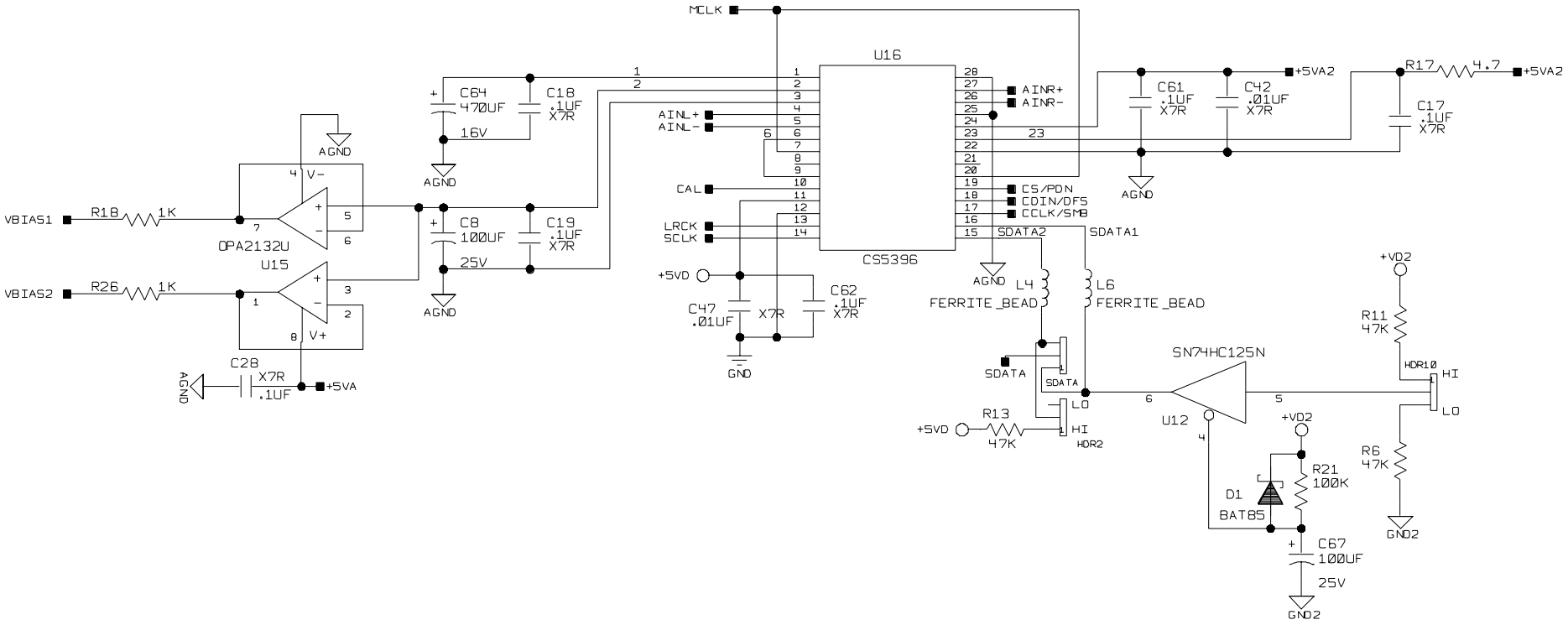


Figure 5. CS5394 and CS5396/7 Connections

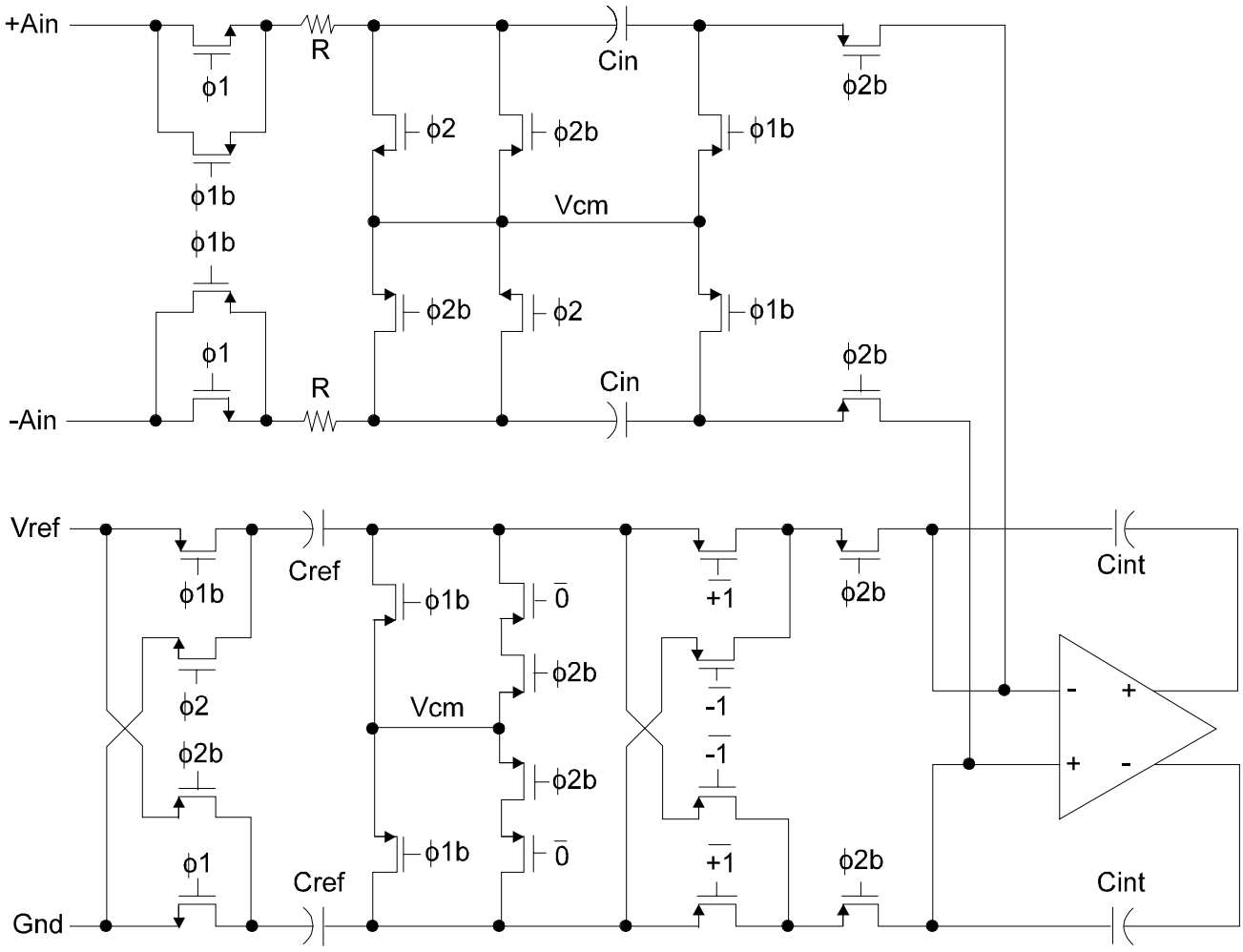


Figure 6. Switched-Capacitor Integrator Circuit

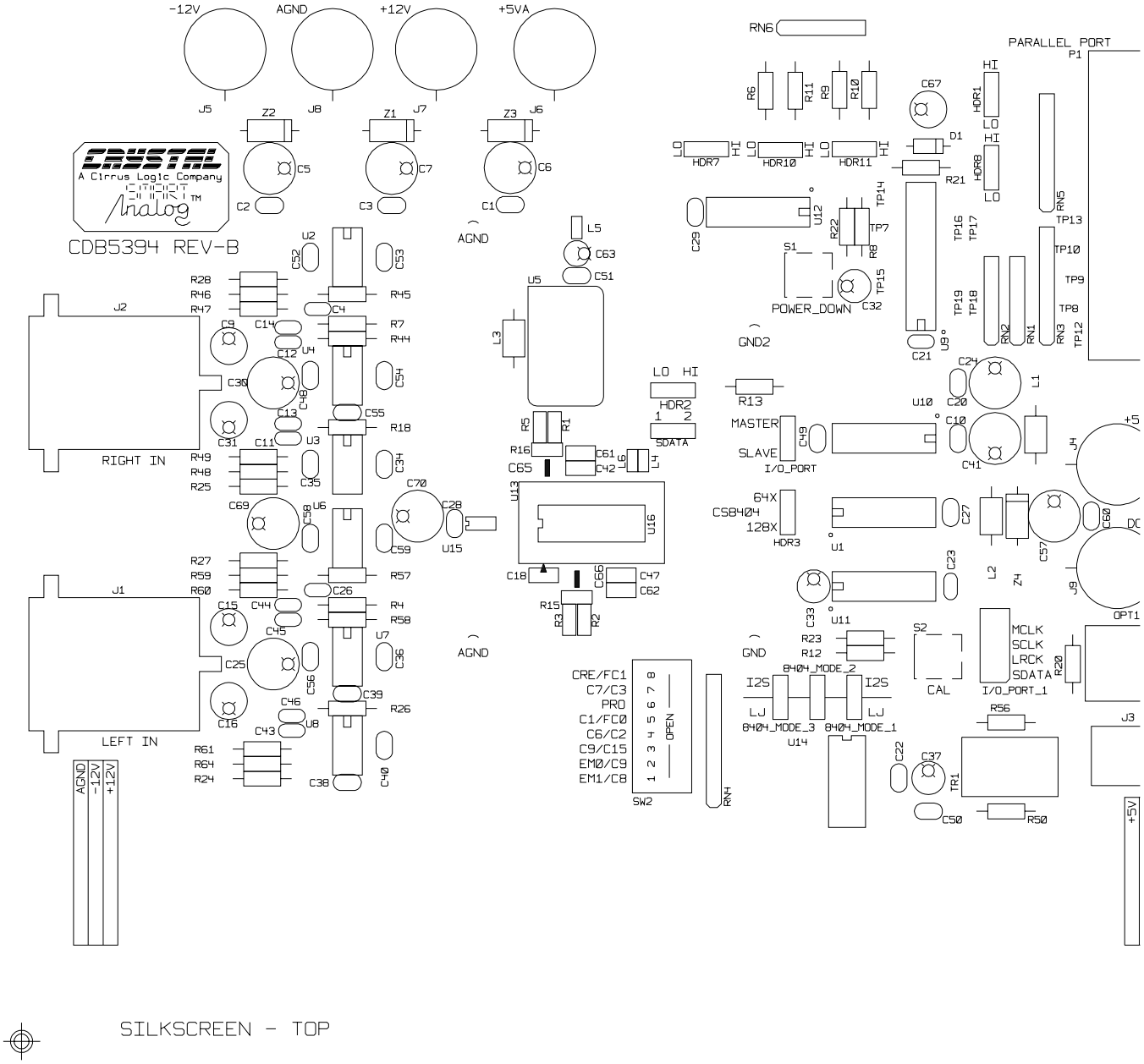


Figure 7. CDB5394 and CDB5396/7 Component Silkscreen Side (top)

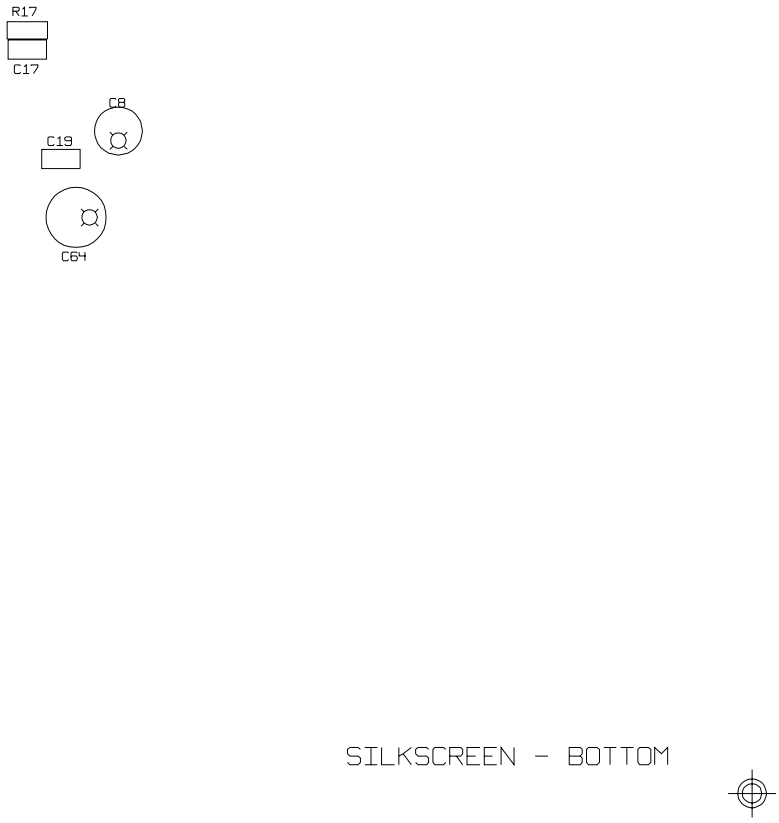
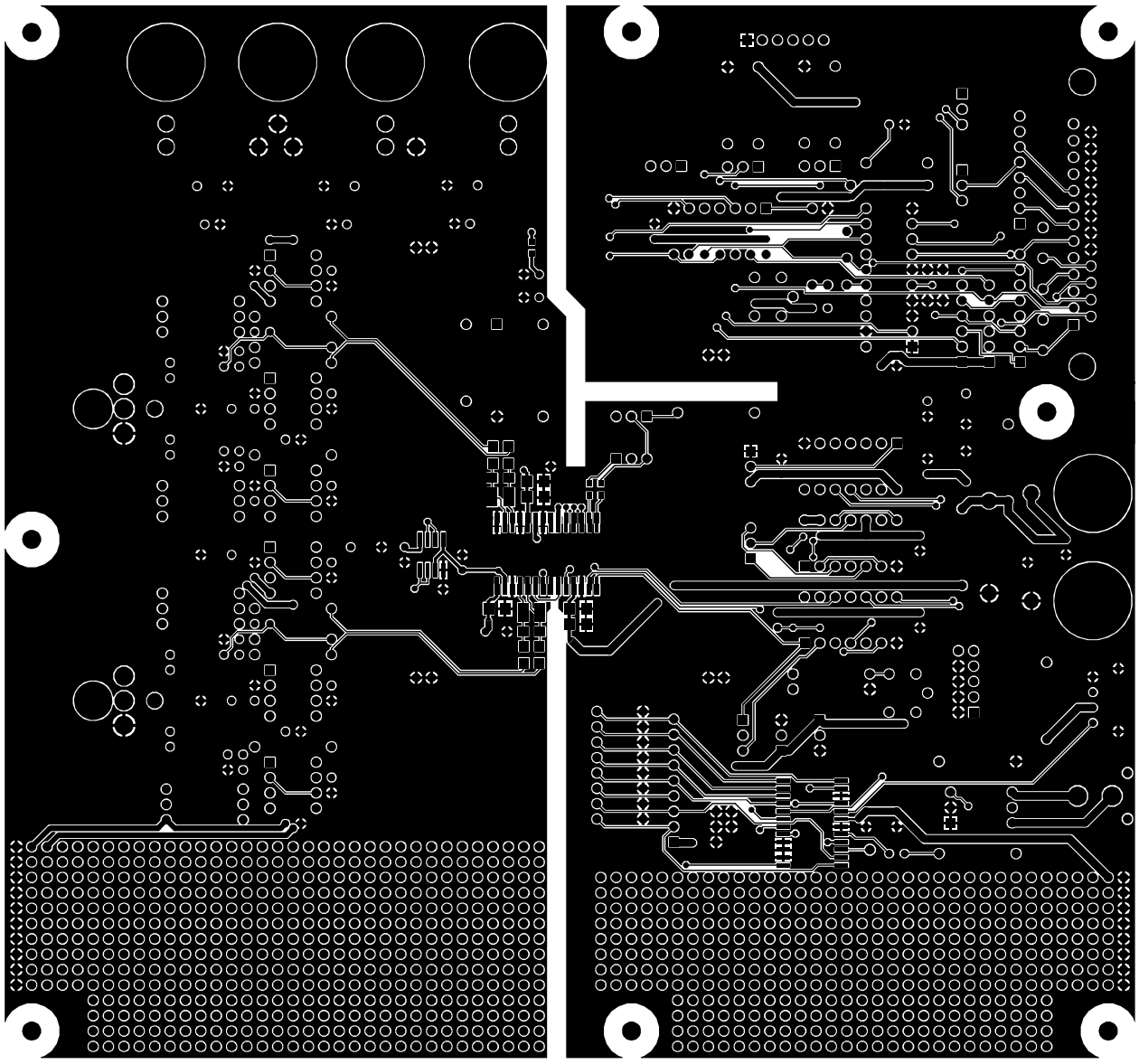


Figure 8. CDB5394 and CDB5396/7 Component Silkscreen Side (bottom)



TOP SIDE

Figure 9. CDB5394 and CDB5396/7 Component Copper Side (top)

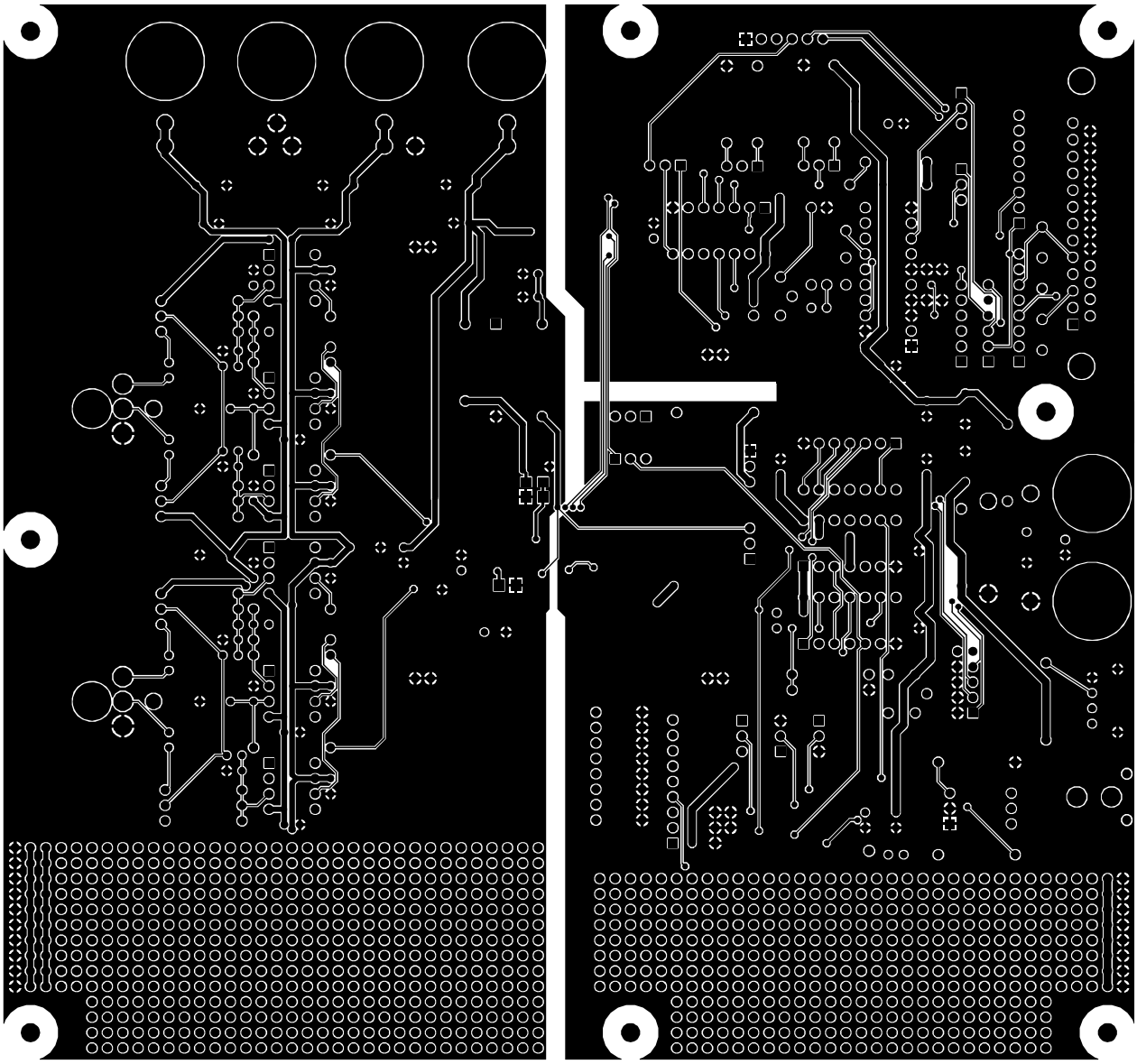
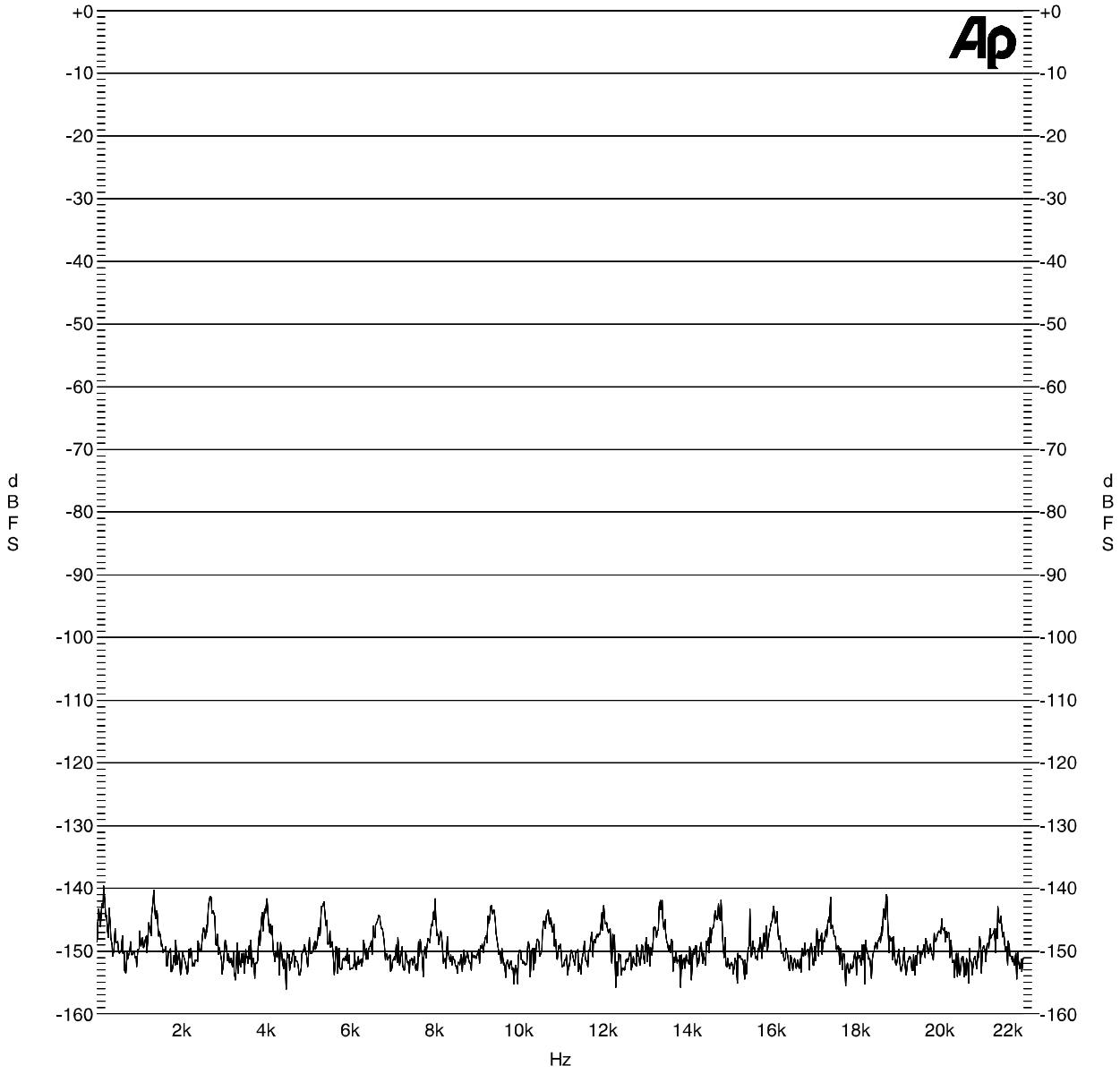


Figure 10. CDB5394 and CDB5396/7 Component Copper Side (bottom)



Line Style	Thick	Data	Axis
Solid	2	Fft.Ch.1 Ampl	Left
Solid	2	Fft.Ch.2 Ampl	Right

Figure 11. Effects of Serial Data Coupling

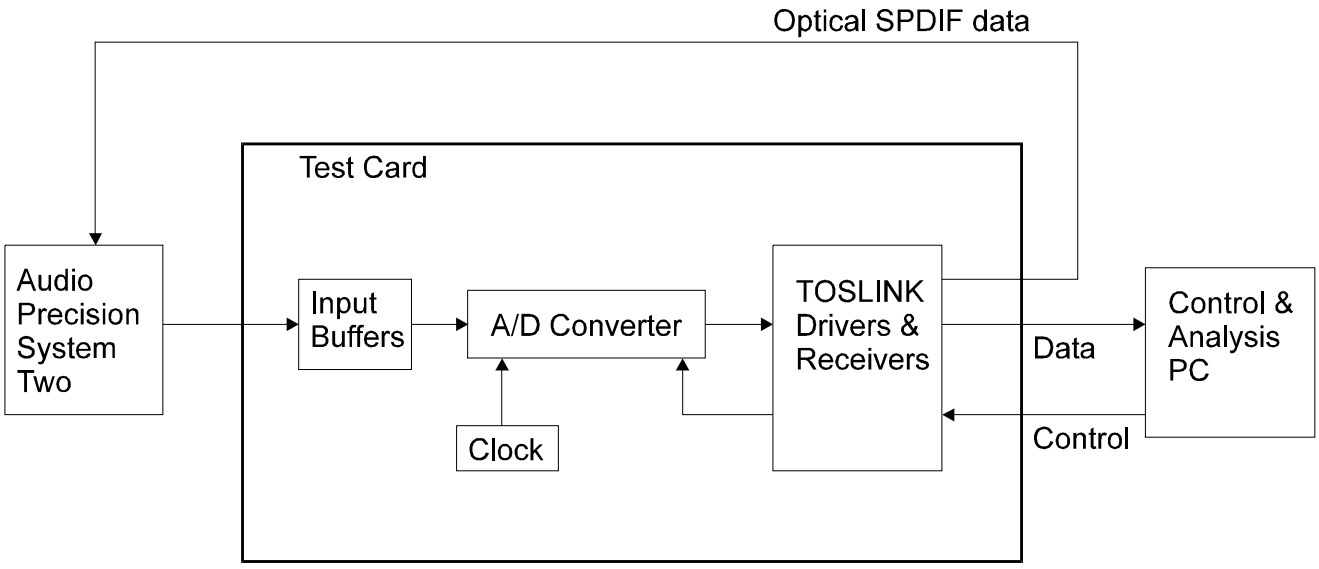


Figure 12. Test Set-up Signal Flow

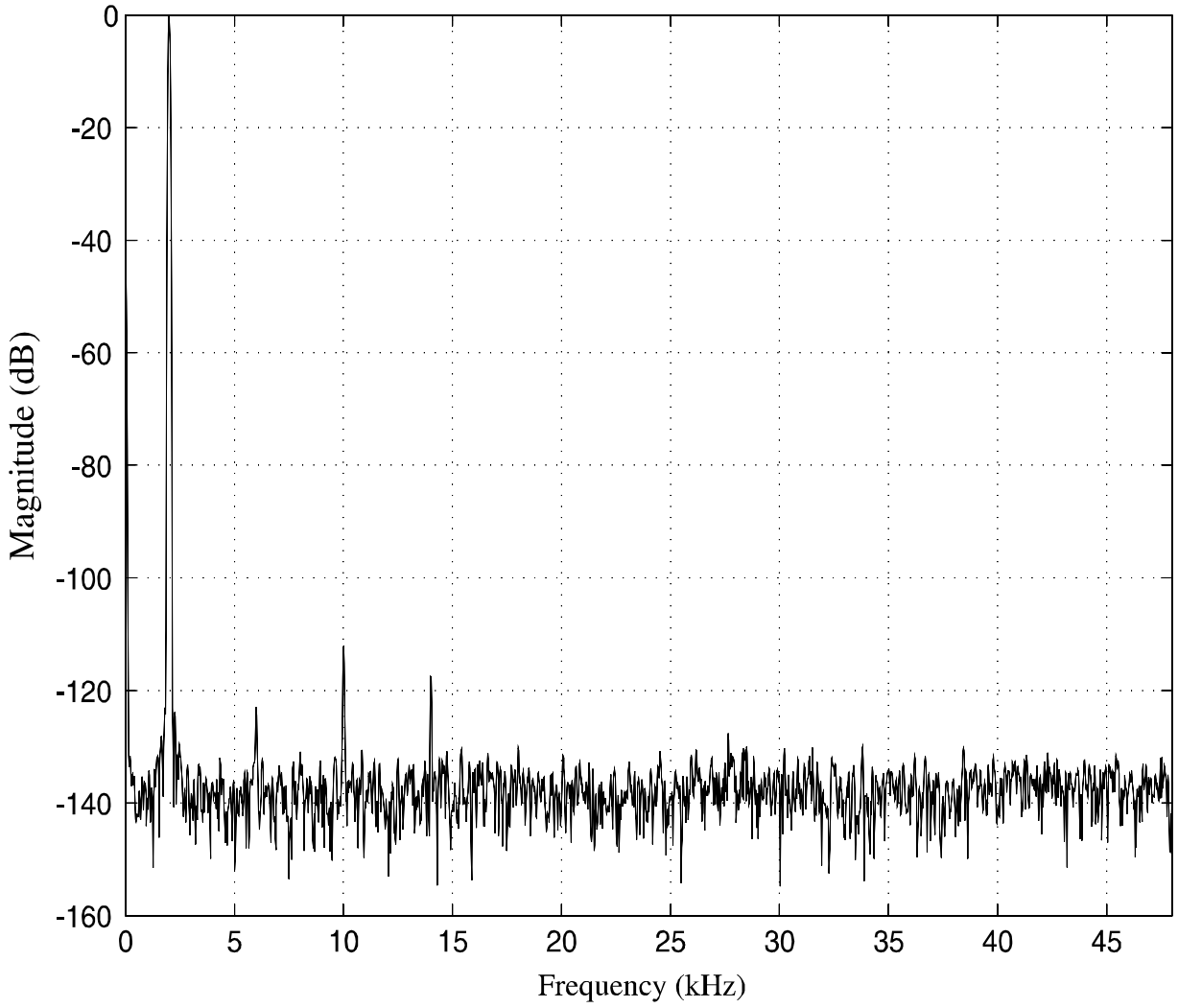


Figure 13. Measured Spectral Response at 96 kHz Output
(2 kHz full scale sinusoidal input)