Application Note

Buffer Amplifiers for the CS5012A/CS5014/CS5016/ CS5101A/CS5102A/CS5126 Series of A/D Converters

by

Jerome Johnston
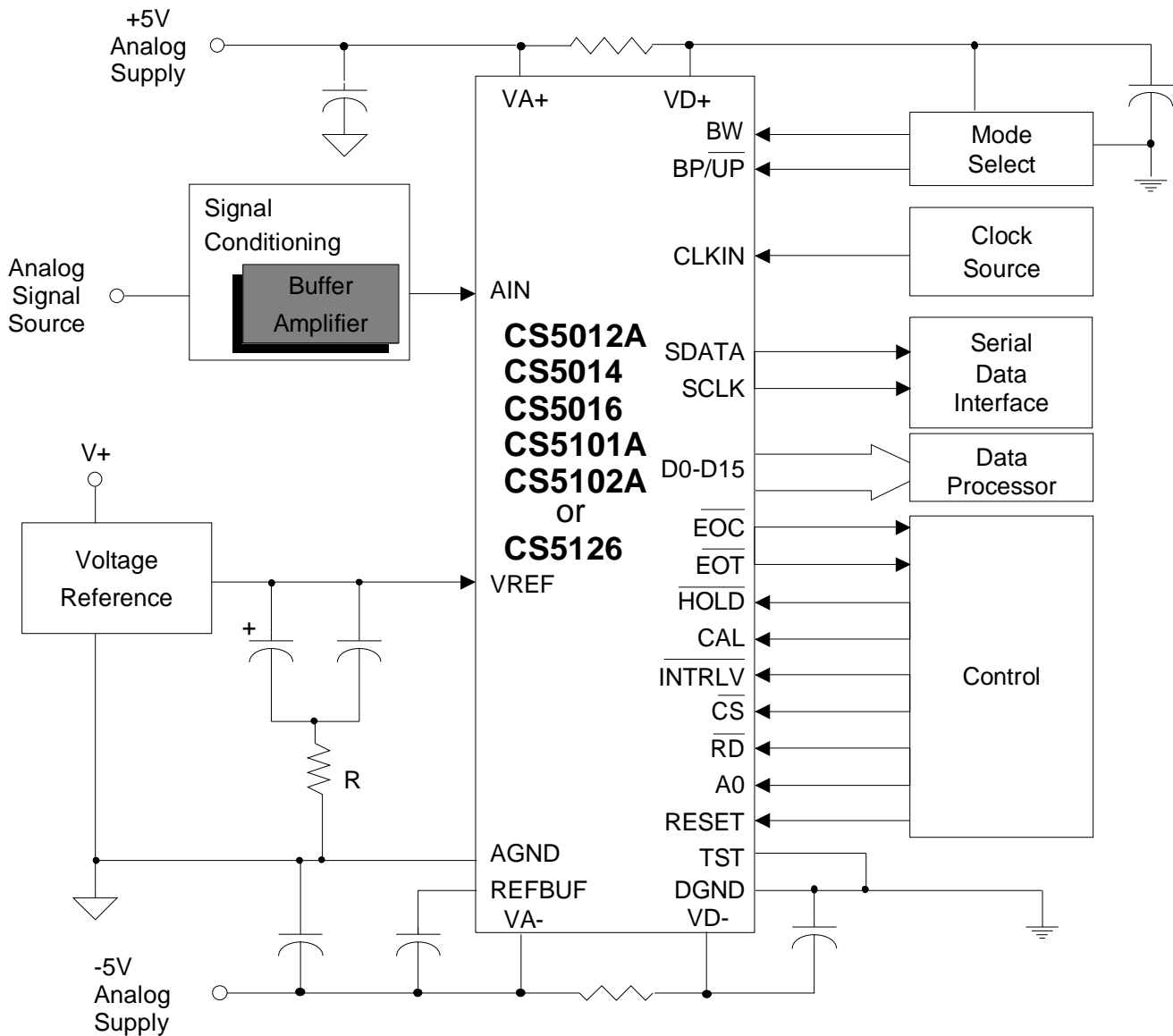
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Introduction

This application note discusses buffer amplifiers for use with Crystal Semiconductor's CS5012, CS5014, CS5016, CS5101A, CS5102A or CS5126 A/D converters. Amplifier design considerations are discussed and several circuits are proposed.

Signal Requirements for Analog to Digital Converters

Crystal Semiconductor is a source for a variety of monolithic A/D Converters. While the type of design configuration of the converters may differ, their uses could be classified into two general categories: those which require specifications in static measurement applications; and those which require specifications for signal processing or dynamic signal measurement applications.

The capability of a converter to achieve a stated static measurement requirement is generally defined by its linearity error specifications, both integral and differential, and by its offset error and gain error specifications. To assess the total error in a static measurement, the effects of temperature on the offset, gain, and linearity errors must also be investigated. In static measurement systems, these same error sources need to be scrutinized in the signal conditioning circuitry as well.

When a converter is used in dynamic signal measurement applications (generically known as "signal processing"), its signal measurement capability is indicated by specifications such as total harmonic distortion, signal to noise ratio, and signal to peak harmonic or spurious noise. Signal processing designers generally evaluate the error contribution of the signal conditioning circuitry in terms of these same parameters.

Signal conditioning circuitry generally includes all circuitry from the transducer or the signal source up to the A/D converter. This application note will concern itself primarily with the requirements of the amplifier which immediately precedes the A/D converter. This amplifier will be called a buffer amplifier.

In the design of an A/D converter system, the buffer amplifier can be a source of significant errors. The significance of these errors can only be assessed if the circuit configuration is thoroughly analyzed for its total error contribution. A thorough analysis requires a good understanding of amplifier specifications, of the limitations of the different circuit configurations, and of the benefits and limitations of feedback. A good place to begin is with a review of feedback theory.

I. OPERATIONAL AMPLIFIERS: Review Of Theory

Feedback Control Theory

The goal in using feedback is to establish a closed-loop system whose operating characteristics are primarily determined by the choice of the feedback elements. The extent to which this goal can be accomplished is explained by feedback control theory. Figure 1 illustrates the
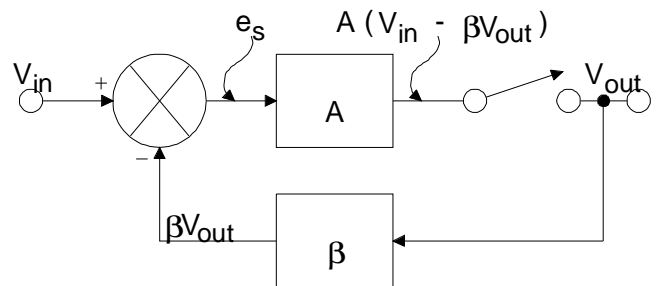

Figure 1. The Classic Feedback Control Loop

classical feedback control loop. The equations which describe this control loop are directly applicable to the noninverting operational amplifier circuit.

The control loop consist of an input voltage differencing section whose output is amplified by a positive gain section. A fractional part of the signal output is then returned to the negative terminal of the differencing section though the feedback network. The input differencing section, indicated by the circle with the X in it, determines the difference in the signals at the (+) and (-) inputs. The difference is indicated by an error signal of the quantity:

$$e_s = (V_{in} - \beta V_{out})$$

Equation 1

which is then amplified by the open-loop voltage gain of the amplifier:

$$A (V_{in} - \beta V_{out}) = V_{out}$$

Equation 2

The amplifier open-loop gain is represented in Figure 1 by the box with the A in it. The feedback portion of the loop is represented by the box with the β in it. β is defined as the feedback attenuation factor and its value is that fractional part of the output voltage which is fed back to the input. Equation 2 can be manipulated to give:

$$A_{CL} = \frac{V_{out}}{V_{in}} = \frac{A}{1 + A\beta}$$

Equation 3

This is the key equation in the feedback system. Equation 3 indicates that the closed-loop gain is

dependent upon both the open-loop gain and the feedback factor, β. The product, $A\beta$, in the denominator is called the loop gain. Its name comes from the gain seen by a signal propagating around the loop through both the A and β networks.

Equation 3 can be manipulated to give:

$$A_{CL} = \frac{V_{out}}{V_{in}} = \frac{1}{\beta} \left[\frac{1}{1 + \dfrac{1}{A\beta}} \right]$$

Ideal   Error
Term   Multiplier

Equation 4

In equation 4 the ideal term, $1/\beta$, determines the ideal closed-loop gain of the system. The value of $1/\beta$ is determined by the elements chosen for the feedback path. The intent is for these elements to determine the closed-loop characteristics of the feedback system. To the extent that this is accomplished is dependent upon the magnitude of the loop gain $A\beta$. The greater the magnitude of $A\beta$, the more closely the error multiplier term approaches unity, therefore allowing the ideal term $1/\beta$ to determine the closed-loop gain of the system. Said another way, the magnitude of the loop gain $A\beta$ is the primary factor which determines how closely the closed-loop performance of a feedback system is determined by the feedback elements. The term $1/\beta$ is known as the noise gain and also determines the gain seen by amplifier input referred noise and other input referred errors (such as offsets and drift parameters). The noise gain of the system is used to determine closed loop amplifier performance with respect to these error parameters, not the signal gain. The noise gain of the two basic op amp configurations will be discussed later in this application note.
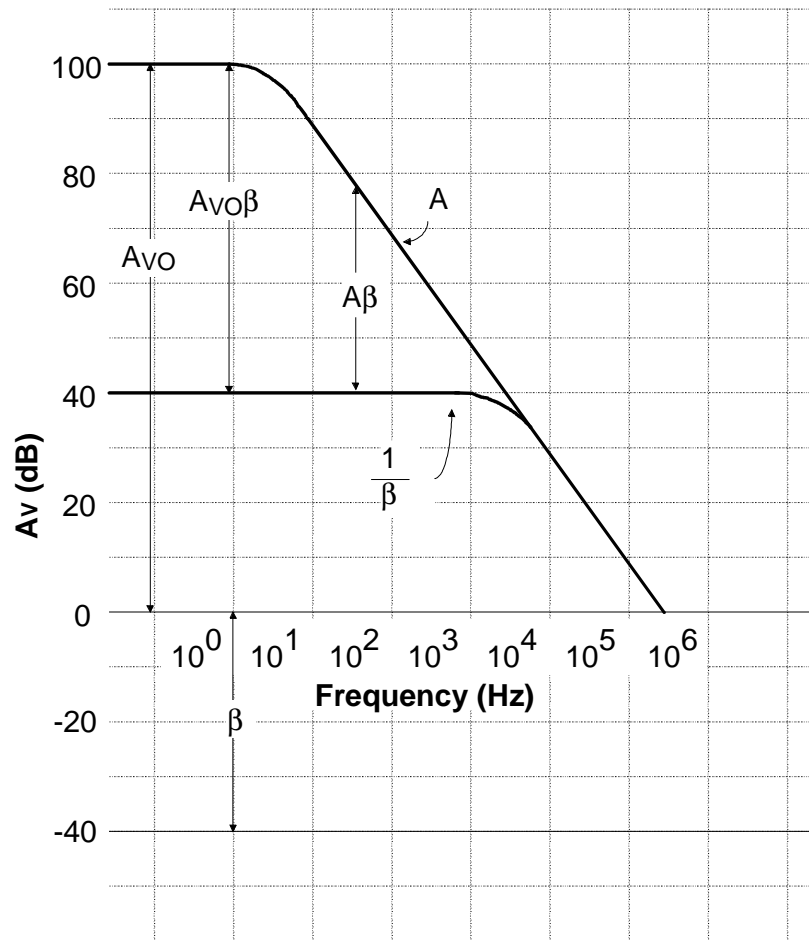
Figure 2. Bode plot illustrating the relationship of Avo, β, 1/β, and Avoβ

## Feedback and the Operational Amplifier Bode Plot

The feedback parameters which have been discussed can be depicted graphically on a Bode plot. Figure 2 depicts the relationship between open-loop gain, the feedback attenuation factor, noise gain, and loop gain as a function of frequency for the noninverting circuit.

The Bode diagram shows a typical plot of the open-loop gain characteristic of an operational amplifier. At very low frequencies a typical operational amplifier may have a dc open-loop gain, (Avo) near 100 dB. A large number of amplifiers use dominant pole frequency compensation which simplifies the compensation requirements for the user. The dominant pole, located between 0.1 and 100 Hz on various amplifiers, causes the open-loop gain characteristic (A) to decrease in magnitude at a 20 dB/decade rate as the frequency is increased. In Figure 2 the logarithm of the feedback attenuation factor (β) is shown to be negative as it is a reduction in signal amplitude. The loop gain, the product of Aβ, (or Avoβ at dc), is depicted in the figure as the sum (+100 dB plus   -40 dB = 60 dB at very low frequency) of the open-loop gain and the feedback attenuation factor, or the difference (+100 dB - (+40 dB) = 60 dB) between the open-loop gain and the noise gain (1/β). From the figure, one can observe that as frequency increases, the loop gain (Aβ) decreases for a set value of β. To obtain a greater amount of loop gain at higher frequencies
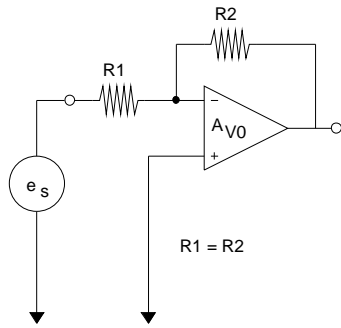
Figure 3A. Inverting:
Gain of -1
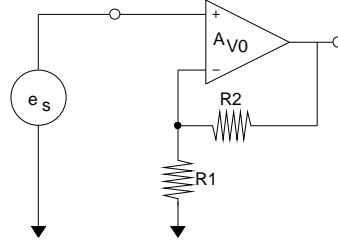
Figure 3B. Noninverting:
Nonunity Gain
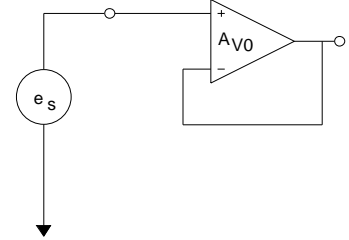
Figure 3C. Noninverting:
Gain of +1

	Figure 3A	Figure 3B	Figure 3C
Closed Loop Signal Gain	$\{A_{CL} = \dfrac{-R2}{R1}\left[\dfrac{1}{1+\left[\dfrac{1}{A\beta}\right]}\right]$	$A_{CL} = \left[\dfrac{R1+R2}{R1}\right]\left[\dfrac{1}{1+\left[\dfrac{1}{A\beta}\right]}\right]$	$A_{CL} = 1\left[\dfrac{1}{1+\left[\dfrac{1}{A\beta}\right]}\right]$
Feedback Attenuation Factor	$\beta = \dfrac{R1}{R1+R2} = \dfrac{R}{2R} = 0.5$	$\beta = \dfrac{R1}{R1+R2}$	$\beta=1$
Loop Gain	$A_{vo}\beta$		
Noise Gain	$\dfrac{1}{\beta} = \dfrac{1}{0.5} = 2$	$\dfrac{1}{\beta}$	$\dfrac{1}{\beta} = 1$
Closed Loop Corner Frequency	$f_c = \dfrac{f_u}{\lvert A_{CL}\rvert + 1}$ note: $\lvert A_{CL}\rvert = \dfrac{1}{\beta} - 1$	$\dfrac{f_u}{\left[\dfrac{1}{\beta}\right]}$	$f_c = f_u$
Closed Loop Gain Stability	$\dfrac{\Delta A_{CL}}{A_{CL}} = \dfrac{\Delta A_{OL}}{A_{OL}}\left[\dfrac{1}{1+A\beta}\right]$		
Closed Loop Distortion and Nonlinearity	$THD_{CL} = THD_{OL}\left[\dfrac{1}{1+A\beta}\right]$		
Closed Loop Output Impedance	$Z_{CL} = Z_{OL}\left[\dfrac{1}{1+A\beta}\right]$		

Figure 3. Basic Circuit Configurations

a designer must either increase the open-loop gain of the amplifier or increase the feedback factor, β (decrease the noise gain). Remember that both the open-loop gain and the feedback attenuation factor are not constant, but instead are functions of frequency. Therefore the value of the loop gain is a function of frequency as well. The quantity of loop gain at the operating frequency is the key measure of how closely an amplifier configuration approaches the ideal.

Amplifier Configurations and Feedback

Figure 3 provides an overview of the inverting and noninverting voltage amplifier configurations. General equations for various parameters of the configurations are given with special emphasis on the unity gain configuration. Signal gain is set by the choice of resistors, but the gain error (assuming perfectly accurate resistors) is a function of the loop gain in the error multiplier term as previously stated in our discussion on feedback. The unity gain noninverting amplifier is just a special case of choosing the value of resistor R1 as being infinite and R2 being zero. Notice that the feedback attenuation factor, β, as derived for both circuits yields the same equation:

$$\beta = \frac{R1}{R1 + R2}$$

Equation 5

but for the unity gain inverting amplifier this results in a value of 0.5 whereas the unity gain noninverting amplifier results in a β of 1. These unequal values of β between the two unity-gain configurations yield further differences between the inverting and noninverting circuits. Loop gain for the unity-gain inverting circuit is half that of the noninverting unity-gain circuit. This results in the inverting circuit being more easily compensated for stability, but also yields greater

errors in those parameters where loop gain is a factor. More will be said about these parameters later.

Reduced β for the inverting configuration results in greater noise gain (1/β). Error sources such as offset and noise are amplified by the noise gain and therefore the unity-gain inverting amplifier is more adversely affected by these error sources. Another negative factor of the unity-gain inverting stage is that its signal bandwidth is half that of the noninverting circuit with identical amplifiers. This bandwidth reduction is because bandwidth is a function of the noise gain, not the signal gain. Be aware of this fact when using low gain inverting stages.

The magnitude of the loop gain in a circuit affects many parameters in both the inverting and noninverting configurations. Closed loop gain stability is improved by increased loop gain as indicated in the equation:

$$\frac{\Delta A_{CL}}{A_{CL}} = \frac{\Delta A_{OL}}{A_{OL}}\left[\frac{1}{1 + A\beta}\right]$$

Equation 6

The effects of changes in the open-loop gain (such as a reduction due to increased temperature) are reduced proportionally to the amount of loop gain. Open loop distortion and nonlinearity are reduced by increased loop gain. This reduction in total harmonic distortion as indicated in the equation:

$$THD_{CL} = THD_{OL}\left[\frac{1}{1 + A\beta}\right]$$

Equation 7

The output impedance of a voltage amplifier is reduced with feedback as indicated in the equation:

$$Z_{CL} = Z_{OL}\left[\frac{1}{1 + A\beta}\right]$$

Equation 8

The input impedance of both amplifier configurations benefit from increased loop gain. Although increased loop gain is desirable in both circuit configurations the effect of feedback on the two configurations is different.

The noninverting amplifier utilizes voltage ratio feedback which increases the differential input impedance seen by the input signal. But the differential input impedance of the amplifier is shunted by the common mode input impedance of the amplifier. Because the common mode impedance cannot be increased by the use of feedback it is usually the limiting factor in increasing the input impedance.

The inverting amplifier configuration uses transadmittance feedback which decreases the impedance at the summing node of the input and feedback resistors. This decrease in impedance improves the virtual ground characteristic of the amplifier. In the inverting configuration the effect of a good virtual ground enables the effective value of the input impedance seen by the signal source to be set by the input resistor.

In both configurations the improvements to the respective impedances depend on the magnitude of loop gain. As the magnitude of loop gain generally decreases with increased frequency, all of the parameters normally improved by loop gain tend to degrade as the signal frequency increases. All real-world amplifiers have finite open loop gain and finite bandwidth, both of which affect the amount of loop gain available to a designer. A designer must make a prudent choice of amplifier

and of the circuit configuration to minimize the errors due to loop gain limitations.

Some Other Error Sources

There are many sources of error in a given amplifier configuration. As already discussed, limited loop gain is a source of gain error which can affect DC accuracy. In addition to the DC gain error, there are the various offset errors which are contributed dependent upon the characteristics of the chosen amplifier. Sources of offset errors are the input offset voltage of the amplifier, the input bias and the input offset currents of the amplifier, limited power supply rejection and limited common-mode rejection.

Which of these errors is dominant will depend upon the choice of amplifier and its application configuration. It is a routine procedure to calculate the contribution of each source of error and this should be done as a matter of course. A few comments on each of these sources of error is appropriate.

All amplifiers have input offset voltage and input bias currents which result in errors in signal measurement. The input bias currents flow through the resistances on the (+) and (-) leads of the amplifier and produce an offset voltage error at each input. These offset voltages, and the voltage offset of the amplifier itself, are then amplified by the circuit to produce an error in the output signal. To reduce the errors due to the bias currents the standard practice has been to balance the value of resistance at the inverting and noninverting inputs to an amplifier. The purpose of making these two resistances equal has been to enable the bias currents at both inputs to produce equivalent values of offset voltage which could then be rejected by the common mode capability of the amplifier. This practice is an acceptable method of reducing error due to the bias currents and is recommended except with

modern amplifier designs which have internal bias current compensation circuitry. The bias current compensation circuitry tends to reduce the bias currents an order of magnitude or more, to the extent that they are reduced to the same order of magnitude as the amplifier's input offset currents. Adding a resistor to one input to achieve equal resistances at the two inputs of these types of amplifiers is not recommended. The added resistance is not effective in reducing the error due to the bias currents, but it will add another source of thermal noise.

Initial offset errors as well as gain errors generally can be reduced to zero with initial system calibration adjustments at room temperature. The effects of temperature-induced offset drift and gain drift remain unless a method of ongoing correction or recalibration is used to remove these effects. This correction may be accomplished with a computer after the analog signals are digitized and is recommended when maximum accuracy of measurement is demanded.

Even if the effects of temperature-induced offset errors are removed from the final data by software, it remains desirable to examine the total errors at each gain stage throughout the system. Voltage offsets due to temperature drift can be removed in software, but may still consume a significant portion of the dynamic range available to the signal. This is especially true in 16-bit converter systems with wide temperature range requirements such as required by some military specifications (-55 to +125 ° C).

Limited power supply rejection and limited common mode rejection are two more sources of errors. Most commercially-available amplifiers are designed such that the offset voltages induced by power supply variations or common-mode signals are very small; but these errors can be significant when amplifying very low level signals with high gain. It is therefore recommended

to examine the error contribution of each of these sources.

Figure 4a shows an inverting amplifier circuit. The operational amplifier and the circuit components have been chosen for illustration purposes. The errors in the circuit due to the various amplifier parameters will be examined. Not included are those errors due to the signal source impedance (the impedance is assumed to be zero), output loading (which reduces open loop gain), resistor tolerance and temperature coefficient, and component long term drift effects.

A table in Figure 4a contains a selected subset of specifications for a "generic" OP-27C. No specific manufacturer is implied. The subset of data is for the total error band of the stated parameters over the -55° to +125°C temperature range. Manufacturers do not always specify temperature drift coefficients in their component data sheets. Instead, the specification sheets contain a table of data for the amplifier at room temperature (25° C) along with a table showing the total error band of the various parameters over a stated temperature span (say 55° to 125° C). Usually the specification data tables are supplemented by supporting graphs which indicate typical drift characteristics for the various parameters. These graphs can be very informative. For example, graphs in the manufacturer's data sheets (see the Precision Monolithics or the Linear Technology data book) for the OP-27 indicate that input bias currents and input offset currents show much more drift at temperatures approaching -55° C than at temperatures above 25° C. Another graph indicates that the direction of the input offset voltage drift in the OP-27 is unpredictable.

The normal procedure to calculate the error contribution of each of the operational amplifier drift parameters is to multiply the rate of drift times the temperature span over which the circuit is to be subjected. These errors due to drift are then added to the initial errors of each of the parame-
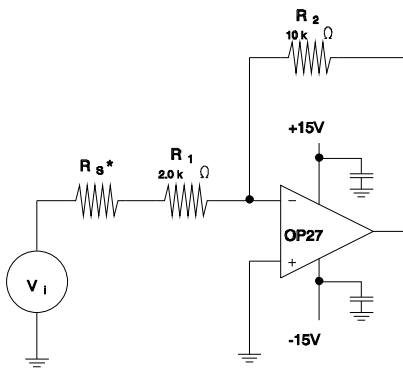
* Assumed to be zero.

$$R_e = \frac{R_2 R_1}{R_1 + R_2} = 1.667\ k\Omega$$

$$\text{Ideal Signal Gain} = \frac{-R_2}{R_1} = -5$$

$$\text{Feedback Attenuation Factor } \beta = \frac{R_1}{R_1 + R_2} = \frac{1}{6}$$

$$\text{Noise Gain} = \frac{1}{\beta} = 6$$

$$\text{Closed Loop Bandwidth } f_c = \frac{f_u}{|A_{CL}| + 1}\left[\frac{8\ x\ 10^6}{6}\right] = 1.33\ MHz$$

Generic OP-27 Specifications
Total Error Band for -55° to +125°C Temperature Span

		Typical	Worst Case
Input Offset Voltage	$V_{IO_{\Delta t}}$	70 μV	300 μV
Input Bias Current[†]	$I_{B_{\Delta t}}$	±35 nA	±150 nA
Large Signal Open Loop Gain	A_0	800×10^3 V/V	300×10^3 V/V
Power Supply Rejection Ratio	P.S.R.R.	4×10^{-6} V/V (108 dB)	51×10^{-6} V/V (86 dB)
Common Mode Rejection Ratio	C.M.R.R.	1.6×10^{-6} V/V (116 dB)	20×10^{-6} V/V (94 dB)

[†] Bias currents are usually of one polarity. Bias currents of both polarities indicate the use of bias current cancellation circuitry in the input stage.

Figure 4a. OP-27 Circuit and Total Error Band Specifications

Gain	Input Offset Voltage	Input Bias Current	P.S.R.	C.M.R.	Noise

$$V_o = -V_i\left[\frac{R_2}{R_1}\right]\left[\frac{1}{1 + \frac{1}{A_0\beta}}\right] + V_{IO\Delta t}\left[\frac{1}{\beta}\right] \quad + \quad I_{B\Delta t}R_1\left[\frac{R_2}{R_1}\right] \quad + \quad \frac{2\Delta V_{IO}}{\Delta V_{SUP}}\left[\frac{1}{\beta}\right] \quad + \quad \frac{\Delta V_{IO}}{\Delta V_{CM}}\left[\frac{1}{\beta}\right] \quad + \text{Noise}$$

$$V_o = -V_i\left[\frac{R_2}{R_1}\right]\left[\frac{1}{1 + \frac{1}{(300x10^3)\frac{1}{6}}}\right] + (\pm 300x10^{-6})(6) + (\pm 150x10^{-9})(2x10^3)(5) + (2)(51x10^{-6})(100x10^{-3})(6) + (\approx 0) + \text{Noise}$$

$$V_o = \quad -.99998\ V_i \quad\quad \pm 1.8x10^{-3}\ V \quad\quad \pm 1.5x10^{-3}\ V \quad\quad \pm 61.2x10^{-6}\ V \quad\quad \pm \approx 0 \quad\quad + \text{Noise}$$

Worst Case Error % Full Scale Output[‡]

0.002%	+ 0.040%	+ 0.033%	+ 0.00136	+ ≈ 0%	+ Noise

[‡] Based upon: 4.5 V FSO; 100 mV power supply change on each supply.

Figure 4b. Total Error Band Calculations

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ters at the ambient operating temperature. Because amplifier manufacturers specify total error band rather than drift rates, the method of computing the error contribution of each parameter must be modified. The equation in Figure 4b illustrates the errors calculated using the total error band specifications on the OP-27C in Figure 4a. The calculations indicate the relative contribution of each source of error in the worst case with the exception of noise, which is yet to be discussed. As can be seen from the numbers, real world amplifiers can contribute significant errors in a high precision data acquisition system due to their non-ideal characteristics.

Noise and its Effects on Measurement

Noise can have a significant detrimental effect in high precision data acquisition systems. Although one can encounter many different sources of noise and of interference in system design, only certain noises made by the components themselves will be discussed here. Thermal noise, also called Johnson noise, is fundamental to all components. The thermal noise in a resistor can be calculated by use of the formula:

$$e_n = \sqrt{(4k\text{TBR})}$$

Equation 9

where $k = 1.38 \times 10^{-23}$ Joules/ degree K (Boltzman's constant), T = Absolute temperature of the resistor, B = the effective "brick wall" Bandwidth over which the noise is to be measured, in Hz, R = Resistance value.

The amount of noise generated by a resistor can be made easier to calculate by remembering that the amount of noise generated by a 1 kΩ resistor in a 1 Hz bandwidth is 4 nV rms. The amount of noise per $\sqrt{\text{Hz}}$ generated by any other valued resistor can be computed from this normalized value:

$$e_r = \frac{4\text{nV}}{\sqrt{(\text{Hz})}} \sqrt{\frac{R}{1\text{k}\Omega}}$$

Equation 10

This noise value assumes a one Hz bandwidth. The noise within a wider bandwidth can be computed by:

$$e_r = \frac{4\text{nV}}{\sqrt{(\text{Hz})}} \sqrt{\frac{R}{1\text{k}\Omega} B}$$

Equation 11

Components other than resistors generate thermal noise. The OP-27 monolithic amplifier is classified by its manufacturers as a low noise amplifier. It is optimized for low voltage noise and requires low source impedances to achieve good noise performance. A plot of the OP-27 noise voltage and noise current characteristics is given in the manufacturer's data sheet. The amplifier's noise is uniform across the higher frequencies, but increases at frequencies approaching DC. This increase is called flicker noise, or 1/f noise.

A thermal noise model of the circuit of Figure 4a is shown in Figure 5. Five noise sources are shown in the model. The amplifier has a voltage noise source e_n and two current noise sources; one associated with each input of the amplifier. Each of the amplifier current noise sources will generate a corresponding noise voltage which is a function of the impedance seen by the current noise source. In addition to the voltage and current noise sources, each of the resistors has a noise voltage source associated with it. The amount of noise contributed at the input of the amplifier by the each of the resistor noise sources is reduced by the loading of the other resistor. For example, consider noise source e_{R2} as having resistor R2 as its source impedance with resistor R1 acting as the load. The noise seen at the input of the amplifier from source e_{R2} will be only
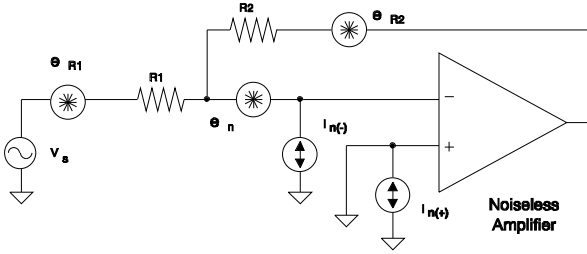
Noise Model of Amplifier in Figure 4a.

Effective Amplifier Bandwidth

OP-27 typical unity gain frequency = 8 MHz

$$\text{circuit bandwidth} = \frac{f_u}{|A_{CL}|+1} = \frac{8x10^6}{5+1} = 1.33 \text{ MHz}$$

effective noise bandwidth
$$B = (1.33x10^6)(1.57)^\dagger = 2.1 \text{ MHz}$$

$\dagger$ The effective noise bandwidth of a single pole, lowpass filter is 1.57 times greater than the 3 dB corner frequency.

Noise Sources of the Model

Amplifier Noise Voltage $\quad e_n$ max (f_0 = 1 kHz) 25 °C = 4.5 nV/$\sqrt{Hz}$ $\quad\Big\}$ From data sheet

Amplifier Noise Current $\quad i_n$ max (f_0 = 1 kHz) 25 °C = 0.6 pA/$\sqrt{Hz}$ $\qquad$ specifications

$$e_{R1} = \frac{4.5 \text{ nV}}{\sqrt{Hz}} \sqrt{\frac{2 \text{ k}}{1 \text{ k}}} = \frac{5.65 \text{ nV}}{\sqrt{Hz}}$$

$$e_{R2} = \frac{4.5 \text{ nV}}{\sqrt{Hz}} \sqrt{\frac{10 \text{ k}}{1 \text{ k}}} = \frac{12.6 \text{ nV}}{\sqrt{Hz}}$$

Equivalent Input Referred Noise (Thermal)

$$e_t = \sqrt{(e_n)^2 + \left[i_{n(-)}\left[\frac{R_1 R_2}{R_1 + R_2}\right]\right]^2 + \left[i_{n(+)}(0)\right]^2 + \left[e_{R1}\left[\frac{R_2}{R_1 + R_2}\right]\right]^2 + \left[e_{R2}\left[\frac{R_1}{R_1 + R_2}\right]\right]^2}$$

$$e_t = \frac{6.8 \text{ nV}}{\sqrt{Hz}}$$

Total Output Noise (Thermal)

$$E_T = e_t\sqrt{B} \; \frac{1}{\beta} = \frac{6.8 \text{ nV}}{\sqrt{Hz}} \sqrt{2.1 \text{ x } 10^6} \; \frac{1}{1/6} = 59 \text{ µVrms}$$

Peak Noise will be much greater.

Figure 5. Noise Calculations

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that portion of its output which is developed across resistor R1 (assuming the input impedance of the op amp is very high). The noise generated by e_{R1} is reduced by the loading of resistor R2. The amount of noise generated at the input of the amplifier by each of the sources is tabulated in Figure 5. The two current sources each have the same value of current noise. Using the values of the noise sources, the effective input-referred voltage noise of the circuit has been calculated. It must be remembered that the noise sources are uncorrelated and therefore add in root-mean-square fashion. This equivalent noise source then represents the total input referred thermal noise. To obtain the value of the noise at the output of the amplifier which will be input to the A/D converter, the input referred noise is amplified by the noise gain of the amplifier while at the same time taking into consideration the effective noise bandwidth of the circuit.

Arriving at a value for the noise bandwidth of the OP-27 circuit is not as obvious as it might seem. If the noise gain of the circuit in Figure 4a is used to compute the 3 dB signal bandwidth the result will be 1.33 MHz. The effective noise bandwidth of a single pole filter is actually 1.57 times greater than the 3 dB corner frequency. But, above 1.33 MHz the OP-27 gain-phase characteristics are not those of a single pole system, but are more complex. The internal gain-phase compensation of the OP-27 will actually cause gain peaking in the circuit of Figure 4a. The gain peaking will occur at the point where the closed loop gain and open loop gain crossover. Also, at frequencies approaching the unity-gain-crossover of the OP-27, the amplifier gain will differ from the roll off of a single pole filter. The effects of the gain peaking and the complex gain-phase characteristics of the OP-27 above the 3 dB corner frequency make an accurate estimate of the resultant noise difficult. One can use the single pole filter characteristics and can approximate the noise bandwidth of the circuit as being 1.57 times the 1.33 MHz corner frequency (2.1 MHz), but the resultant noise calculation using

this bandwidth will yield only a coarse approximation of the actual noise .

Using the assumption that the approximation is adequate, the noise at the output of amplifier has been calculated as shown in Figure 5. The calculated value is the amount of thermal noise in rms volts.

Thermal noise is both white and Gaussian. "White" describes the noise as having equal spectral density at all frequencies. "Gaussian" defines the probability density function which describes the amplitude characteristics of the noise. Gaussian noise follows the Normal Distribution. Therefore, once the rms value of the noise has been determined, the probability of occurrence of any value greater than a particular amplitude can be determined. The peak (+ and -) noise associated with a stated probability of occurrence is indicated in the following table:

Probability of Having a higher Amplitude Occurrence	Peak to Peak Amplitude
10 %	3.29 x RMS
1 %	5.15 x RMS
0.1 %	6.58 x RMS
.001 %	7.78 x RMS

Since the peak noise can adversely affect A/D measurements it should be investigated by both analysis and measurement.

Minimization of thermal noise in system design is accomplished with the application of three design principles. First, it is good practice to use the lowest resistor values possible (this assumes a voltage amplifier system) limited only by the constraints necessary to meet other system requirements. Second, choose an appropriate amplifier. Some amplifiers, such as the popular

LM324, do not include noise specifications in their data sheet. If low noise is a system requirement, amplifiers which have no noise specifications are not likely to be an appropriate choice. Also, choose an amplifier which is optimized to work with the source impedance requirements of the system. Bipolar-input amplifiers are generally optimized to work with low impedances as they have lower voltage noise than current noise while FET-input amplifiers are generally optimized for high impedances due to their lower current noise. The optimum choice of amplifier will depend not only on the amplifier, but its associated gain elements and circuit configuration. Analysis of the various possible configurations is necessary to disclose which will be optimum to meet design requirements. Third, one of the easiest ways to reduce the effects of noise is to restrict the bandwidth. System bandwidth should be restricted to only that amount necessary to meet system requirements. This should be done as a matter of good practice.

While only the effects of thermal noise have been discussed be aware of other noise sources (see the reference material at the end of this application note). Note that in the circuit of Figure 4a the effects of the 1/f noise were not investigated. If the system requirements demand the lowest noise possible the effects of the 1/f noise needs to be examined. The example calculations on thermal noise were done at room temperature. An increase in temperature to 125° C will result in about 1.3 dB greater noise.

Last of all, the calculated answers are only theoretical estimates. The calculations provide a theoretical minimum value but the final determinant of design should be in the evaluation of total system function and/or measurement of the actual amount of noise in the system. Remember that the value of the noise calculated provides only a reference point for the minimum amount of noise in the circuit; the actual amount present will never be less than the theoretical amount calcu-

lated, but can be more, due to other noise sources which have not been accounted for. For a more thorough discussion of noise as it applies to amplifier design see references 2 through 6 listed at the end of this application note.

Settling Time

Amplifier circuits have limitations which restrict just how quickly they can produce an accurate output signal at the application of a step change of the input signal. For small changes in signal amplitude, the ability of the amplifier to respond is dependent upon its 3 dB upper corner frequency. If the amplifier gain-phase characteristics approximate a single pole response above the 3 dB frequency the output signal will asymptotically approach a steady state output value Vs as defined by the equation:

$$V_o(t) = V_s \left[1 - e^{\left(\frac{-t}{\tau_c}\right)} \right]$$

Equation 12

Where the time constant, τ_c, is given as a function of the corner frequency:

$$\tau_c = \frac{1}{2\pi f_c}$$

Equation 13

Settling time is defined as the elapsed time from when the input step voltage is applied until the output signal reaches and stays within a given error band of a steady state value.

If the input step change is large, the slew rate limit of the amplifier will restrict the speed at which its output can change. The limit at which an amplifier can slew is a function of how fast it can charge or discharge its compensation capacitor. The maximum frequency of a given

amplitude that can be faithfully reproduced by an amplifier with a stated slew rate is defined by the equation:

$$f_{max} = \frac{SR}{2\pi V_p}$$

Equation 14

where Vp is the peak output voltage.

When large changes of signal at the input occur, the settling time of the amplifier will be a combination of initial delay, slew rate limited excursion, and small signal settling time as indicated in Figure 6. Note that the small signal settling illustrated in Figure 6 is not that of a single pole system, but is instead representative of an actual wideband amplifier.

A first order approximation of settling time can be estimated for a circuit under the following conditions. First, the signal must not cause the amplifier to enter slew rate limiting. Second, the 3 dB corner frequency of the amplifier must be known and it's roll-off must be at 20dB/decade for at least a decade of frequency above the 3 dB corner frequency. Under these conditions the following equation yields a good approximation to the settling time:

$$t = -\frac{1}{2\pi f} \ln \left| \frac{V_o}{V_s} - 1 \right|$$

Equation 15

where f is the 3dB frequency. To settle to 1/2 LSB at N bits (N = 16 in a 16-bit A/D) the equation can be written as:

$$t = -\frac{1}{2\pi f} \ln \left| \frac{2^N - 0.5}{2^N} - 1 \right|$$

Equation 16

Which can be simplified to the following:

$$t = \frac{(1 + N)(0.11)}{f}$$

Equation 17

Settling time is not readily predicted in other circumstances. It varies with signal amplitude and is as much dependent upon the circuit configuration and circuit components (including things like stray capacitance) as it is upon the amplifier characteristics. An assessment of circuit settling time is often best be obtained from observation of the circuit under applicable conditions.
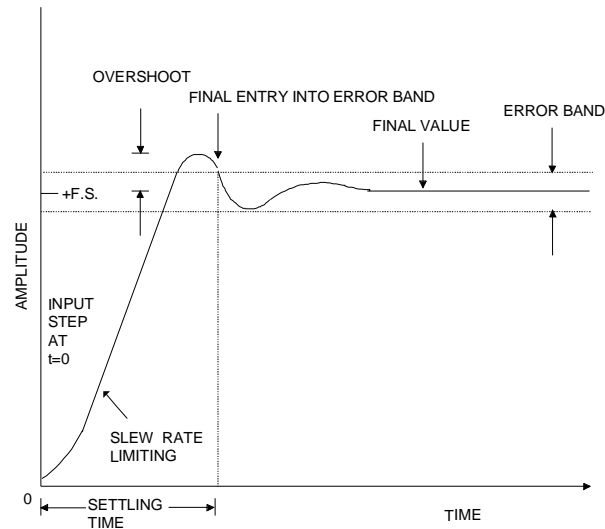

Figure 6.

II. THE CS5016 FAMILY A/D CONVERTER INPUT STRUCTURE

The analog input pin (AIN) of the CS5016 series converter acts as a load to the buffer amplifier output. A good understanding of the internal workings of this pin on the converter will help in the design of an appropriate buffer amplifier.

Figure 7a depicts a simplified circuit diagram of the circuitry internal to the A/D converter as seen from the AIN pin. From the metal pin of the
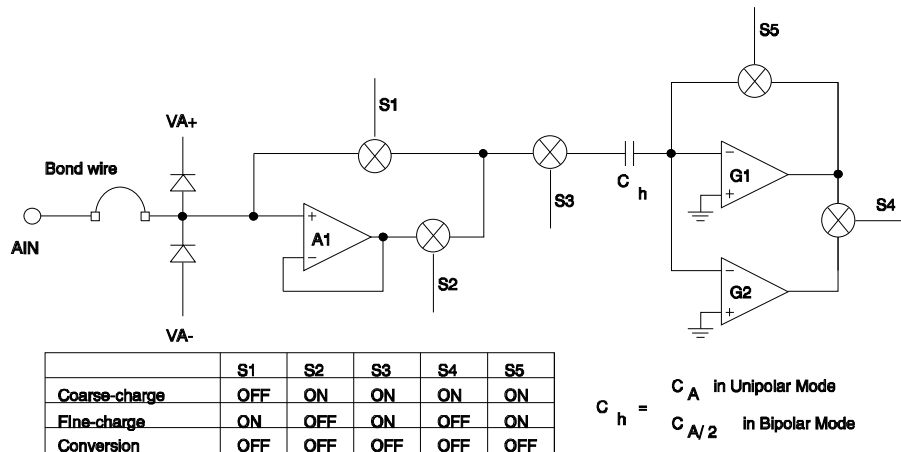
	S1	S2	S3	S4	S5
Coarse-charge	OFF	ON	ON	ON	ON
Fine-charge	ON	OFF	ON	OFF	ON
Conversion	OFF	OFF	OFF	OFF	OFF

$$C_h = \begin{cases} C_A & \text{in Unipolar Mode} \\ C_{A/2} & \text{in Bipolar Mode} \end{cases}$$

Figure 7a CS5016 Family Analog Signal Input Model

package a bond wire connects to the semiconductor chip. Clamp diodes on the chip connect to both of the supplies. Under abnormal conditions, excess signal amplitude may forward bias the diodes. The diodes protect the chip from voltage breakdown. Unless the current under such fault conditions is limited, the diodes may short out or the bonding wire may "blow its fuse". The current should be limited to under one hundred mA transient or under 10 mA steady state to eliminate any possibility of damage. Methods of limiting input current to the A/D converter are discussed below. Once the input signal travels beyond the protection circuitry, it sees a buffer amplifier A1, CMOS switches S1, S2, and S3, a hold capacitor C_h, and transconductance amplifiers G1 and G2. To accomplish a complete conversion cycle, the states of the CMOS switches are altered. These state changes cause the effective load at the AIN pin to change dynamically during the three different phases of the conversion cycle. These three phases are called coarse-charge, fine-charge and conversion. An understanding of the function of each of these three phases will explain the reasons for the dynamic change in loading. The conversion phase begins with the activation of the hold command ($\overline{\text{HOLD}}$ goes low).

When hold is activated, the "sample capacitor" of the track-and-hold section of the converter immediately traps a charge on the sample capacitor which is representative of the input signal. The binary representation of the value of the charge is then determined. The number of master clock cycles necessary for this determination to occur is a function of the number of bits of the converter and the particular mode of operation (loopback or asynchronous). The occurrence of the $\overline{\text{EOC}}$ (end of conversion) signal indicates that the conversion time is complete. The converter must then acquire a new sample of the input signal for the next conversion. The coarse-charge and fine-charge times accomplish this. First to occur is the coarse-charge phase. A buffered version of the analog input signal is first connected to the sample capacitor. The input impedance of the buffer is very high and therefore does not load the input signal source. The output of the buffer is connected via switches S2 and S3 to the sample capacitor (switch S1 is open). The buffer (Figure 7a, A1) furnishes the majority of the current necessary to charge the capacitor toward the new voltage value. The buffer therefore reduces the transient current demand from the signal source if the input signal has changed from the value previously stored on the sample capacitor. The sample capacitor is connected to the output of the buffer for six cycles of the master clock (CLKIN) frequency. At the end of the six cycles the coarse-charge phase is complete.

The sample capacitor is then directly connected to the analog input signal for the fine-charge phase (Switches S1 and S3 are closed, S2 is opened). Immediately before being connected for the fine-charge phase, the voltage on the sample capacitor may still differ slightly from the analog input value. This is due to the offset voltage of the buffer amplifier (A1). This offset voltage is typically 50 mV but may be up to 150 mV in the worst case. At the beginning of the fine-charge phase a small transient demand of current from the external signal source may occur as the capacitor charges to its final value. The fine-charge phase will last until the hold command becomes active again. In loopback mode the fine-charge phase lasts nine master clock cycles until the end of track ($\overline{\text{EOT}}$) signal reactivates the hold command. When the hold command is activated asynchronously, the fine-charge phase should last a minimum of nine master clock cycles and may continue indefinitely until the hold command is activated.

Simplified models of the impedances seen by the analog input signal are depicted in Figures 7b and 7c. For the conversion and coarse-charge phases, the impedance seen at the AIN pin is the input impedance of the buffer A1. This impedance is approximately 100 MΩ shunted by 15 pF. When in the coarse-charge phase the sample ca-
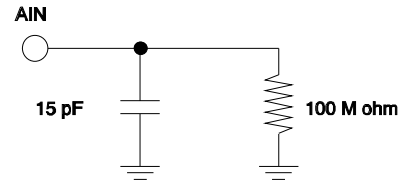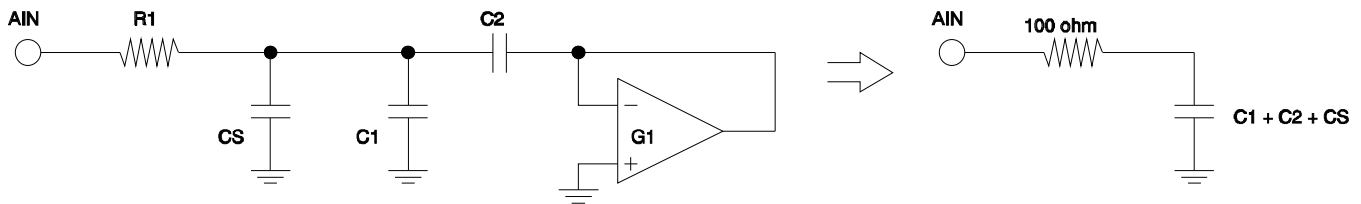

Figure 7b. Simplified Input Model During Coarse-charge / Conversion

pacitor is charged by the buffer (A1) output. The speed at which the voltage on the sample capacitor can track the input signal is limited to the rate at which the buffer output current can charge the capacitor. The slew rate of the buffer is 5 V/μs when the converter is in unipolar mode and 10 V/μs when in the bipolar mode. The reason for the difference is that the sample capacitor in bipolar mode is only half the value of that in unipolar mode.

The simplified model of the impedance seen in fine-charge is that of Figure 7c. Resistor R1 is the effective resistances of the S1 and S3 CMOS analog switches of Figure 7a. The sample capacitor consists of C2, whereas capacitor C1 and CS are stray capacitance. G1 is a transconductance amplifier with an effective input resistance of about 35 Ω at DC. The slew rate in the fine-charge mode is limited to the rate at which the output current of the transconductance amplifier

	C1	C2	CS	R1	Gin
Unipolar	170 pF	170 pF	20 pF	100 ohm	35 ohm
Bipolar	85 pF	85 pF	30 pF	100 ohm	35 ohm

Figure 7c Simplified Input Model During Fine-charge.

G1 can charge capacitor C2. In unipolar mode the slew rate is 0.25 V/μs. In bipolar mode when the capacitance of C2 is less, the slew rate increases to 0.5 V/μs. Acquisition of fast slewing signals (step functions) can be hastened if the step occurs during the conversion cycle or during the coarse-charge cycle since at these times the slew rate of the converter input is faster. It should be noted that in fine-charge, any external impedance on the AIN pin becomes part of the total network and will contribute to the settling time response characteristics.

Also, Figure 7a shows that when switches S1 and S3 are turned on (S2 is off) in the fine-charge phase, the source impedance of the external circuitry connected to the AIN pin actually becomes part of the feedback network of amplifier G1. The external circuitry should offer an impedance less than 400 Ω at frequencies greater than 2 MHz or amplifier G1 may oscillate.

The input circuitry of the analog front end of the A/D converter uses CMOS analog switches which are similar to analog switches available in individual integrated circuits. The resistances of the CMOS switches, such as shown in Figure 7c, exhibit non-linear effects with changes in signal amplitude and frequency. These dynamic changes in switch characteristics are a source of distortion at high frequencies.

III. EXAMPLE BUFFER CIRCUITS

Buffer Circuit Test Method

Several example buffer circuits have been constructed and tested. Evaluation was restricted to dynamic testing at room temperature (25° C). The testing was performed using a CDB5016 evaluation board connected to an IBM compatible computer via a 16-bit parallel I/O card. Signal processing software developed at Crystal was used to evaluate the data. The signal source

was a Khron-Hite 4400A Low Distortion Oscillator modified to produce low broadband noise per the article in Reference 1 (Reprints available from Crystal upon request). The oscillator was adjusted to the appropriate full-scale value for each circuit. A frequency of 1.5 kHz was chosen as the test frequency.

The output data from the A/D converter was processed to yield three indicators of dynamic performance. These are:

1) S/(N+D):   The ratio of the rms value of the signal to the rms sum of all other spectral components below the Nyquist rate (except DC), including distortion components.

2) S/D: The ratio of the rms signal value to the ratio of the rms sum of all harmonics.

3) S/PN: The ratio of the rms signal value to the rms value of the next largest spectral component below the Nyquist rate (except DC).

Benefits of an RC Isolation Network

All of the example circuits show an RC network coupling the output of the buffer to the input of the A/D converter. The 200 Ω resistor and 1 nF capacitor network is recommended for the CS5012A, CS5014, CS5016, and CS5126. The 200 Ω resistor should be replaced with 50 Ω for the CS5101A and CS5102A. The RC filter enhances circuit operation in four ways. First, the network reduces the amount of broadband noise. Second, it decouples the input capacitance of the A/D converter from the amplifier. This reduces the possibility of the amplifier having stability problems driving a capacitive load. Third, the circuit isolates the output of the amplifier from the high frequency pulsed charge effects of the sampling front end of the A/D converter. And finally, the passive network offers a well-behaved low source impedance to the internal transconduc-
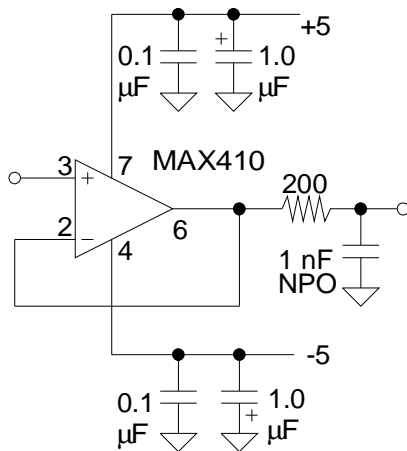
Gain	1
Input	1.5kHz, $\pm$3.5Vpk
VREF	3.5 V
S(N+D)	90.54 dB
S/D	100.1 dB
S/PN	104.7 dB

Figure 8 . MAX410 Noninverting Amplifier

tance amplifier, satisfying its stability needs. The component values are chosen to have a time constant of 200 ns to provide appropriate settling time when the converter (16 bits) is sampling at 50 kHz. The NPO dielectric characteristic minimizes the effect of voltage coefficient of capacitance which can adversely affect performance at the 16-bit level. Other dielectrics may be adequate while some may result in non-linear capacitance with signal level and therefore introduce distortion. Empirical testing may be necessary to insure whether a given dielectric is adequate for a particular application.

## $\pm$ 5 Volt Supply Op Amp Circuits

The first example circuit is a unity gain buffer circuit shown in Figure 8. The MAX410 op amp is designed for operation from $\pm$ 5 V power supplies. The input common mode range of the amplifier is specified as $\pm$ 3.5 V, therefore the reference voltage for the A/D converter was set to use +3.5 V as its full scale reference value. The circuit yields quite good results when the reduced signal level is considered.

The second circuit, Figure 9, configures the MAX410 in the inverting mode. The minimum output voltage swing for the MAX410 is specified as $\pm$ 3.6 V (2 kΩ load) with a typical range of $\pm$ 3.7 V. A 3.5 volt reference was used for the A/D converter. Performance was good using the 3.5 volt reference.

$\pm$ 15 Volt Supply Op Amp Circuits

Most precision operational amplifiers are specified for operation from $\pm$ 15 V supplies. Figure 10 shows an OP-27 used to reduce signal levels of $\pm$ 10 V to $\pm$ 4.5 V. The performance is excellent. Figure 11 then shows the OP-27 in the non-inverting configuration.

The performance levels being achieved with the OP-27 result from operating the amplifier well within its specifications for input range and output amplitude capability. The Signetics NE5534A worked equally well in both circuit configurations (Figures 10 and 11). Note that low value resistors are used to minimize the component noise in the circuits.
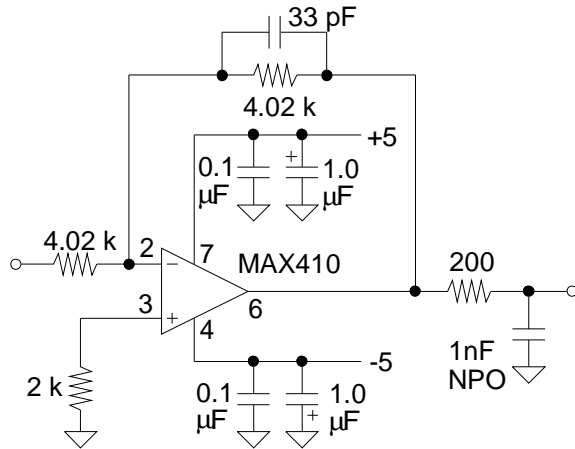
Gain	-1
Input	1.5kHz, $\pm$3.5 Vpk
VREF	3.5 V
S/(N+D)	90.1 dB
S/D	97.7 dB
S/PN	102.0 dB

Figure 9. MAX410 Inverting Amplifier

If an OP-27 type amplifier is used, the inverting circuit is preferred for signal processing applications. This is because some brands of OP-27 amplifiers exhibit much higher distortion at frequencies above 10 KHz or so when used in the non-inverting configuration. It may be that the internal bias current cancellation circuitry does not track the input stage well when subjected to the rapidly-varying (high frequency) common mode voltages such as those experienced by the positive gain configuration.

Achieving $\pm$ 4.5 Volt Output with $\pm$ 5 Volt Supplies

Some designs may require that the entire system operate from $\pm$5V, but achieve the full dynamic range of the A/D converter when using a 4.5 V reference. The Signetics NE5534A op amp, known to be excellent for audio use, can be combined with a discrete transistor output stage to yield excellent results when using only $\pm$ 5 V supplies. Figure 12 illustrates the NE5534A in the inverting configuration, reducing a $\pm$ 10 V signal to $\pm$ 4.5 V. The OP-27 (without the external compensation capacitor) yielded similar noise

and distortion results but had slightly slower rise time when tested with a transient input.

An Instrumentation Amplifier Circuit

Some systems require an instrumentation amplifier front end. One instrumentation amplifier was tested; the AD625C from Analog Devices. The data sheet specifies a maximum nonlinearity of 0.001%. Although the device may have good static linearity, its dynamic performance was well below 16-bit performance. The AD625C, shown in Figure 13, was tested with two different gains. The instrumentation amplifier was tested with a gain of one, and then with a gain of nine. The gain of nine configuration is with the 5 kΩ resistor connected to pins 2 and 15. The data indicates that the part actually has greater distortion (indicative of greater nonlinearity) in the lower gain configuration.

Signal Limiting Circuits

When utilizing op amps with $\pm$ 15 V supplies to drive A/D converters with $\pm$ 5 V supplies it is possible under certain input conditions for the
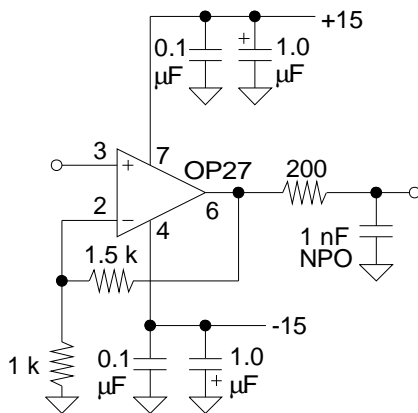
Figure 10. OP-27 Inverting Amplifier
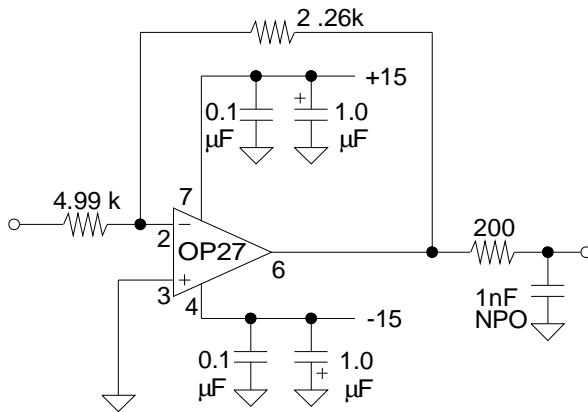
Gain	-0.45
Input	1.5kHz, ±10Vpk
VREF	4.5 V
S(N+D)	91.8 dB
S/D	100.5 dB
S/PN	102.6 dB

amplifier output voltage to attempt to exceed the supply rails of the converter. As described previously, the converter has protection diodes at the analog input and therefore will clamp the voltage whenever the signal forward biases the diodes. If high current amplifiers are used, excess current from the amplifier may damage the converter. If excess current is a possibility, then the voltage swing of the amplifier must be limited so as to not exceed the supplies of the converter; or some means of current-limiting must be used. Many amplifiers have current limiting circuitry as part of their output stage and will limit their output current if a fault condition exists. Even though the amplifier may protect itself in this manner it

may not be desirable from a system performance point-of-view. System measurement accuracy can be degraded due to offset and gain errors which occur as a result of amplifier self-heating.

Several approaches to amplifier output limiting can be used. Zener or diode bounding circuits can be used. Some bounding/clamping circuits reduce the circuit gain by reducing the effective feedback resistance when an overvoltage signal exists. Others limit the signal by shunting it to ground when it exceeds the desired amplitude. Reference 6 documents some of these circuits and discusses their strengths and weaknesses.

Gain	+2.5
Input	1.5 kHz, ±1.8 Vpk
VREF	4.5 V
S(N+D)	90.7 dB
S/D	98.0 dB
S/PN	102.3 dB

Figure 11.   OP27 Noninverting Amplifier

Figure 12. Op Amp with Transistor Buffer Stage
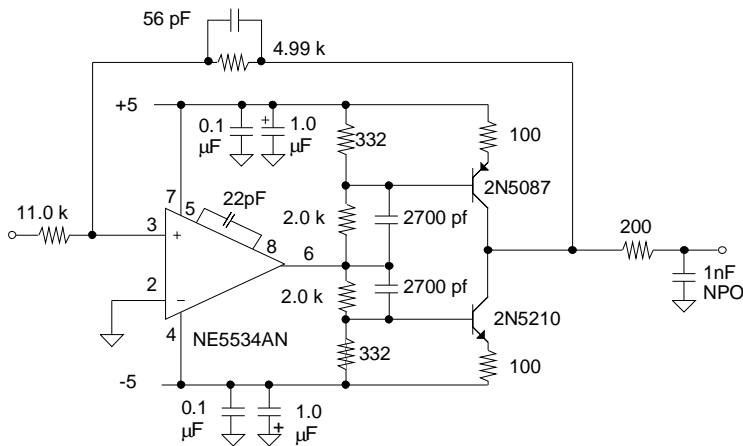
| Gain	-0.45
Input	1.5 kHz, ±10Vpk
VREF	4.5 V
S (N+D)	91.7 dB
S/D	99.7 dB
S/PN	103.3 dB

Voltage Clamping via the Compensation Pin

Figure 14 indicates a simple means of clamping available on some op amps. Illustrated is a Harris HA-2600 with diodes connected to its compensation pin (8). The ± 5 V supplies of the A/D converter provide the clamp voltage reference values for the diodes. The output stage of the HA-2600 has unity voltage gain but high current gain. The signal on pin 8 of the amplifier is a low current signal of identical amplitude to the output signal. Limiting of the output signal swing

is accomplished by clamping the signal at pin 8 to the desired level. Even if the on voltage of the clamp diodes on the op amp exceed the on voltage of the clamp diodes inside the A/D, the 200 Ω resistor will limit the current to an acceptable level.

A Novel Method to Aid Current Limiting

Another method of protecting the A/D converter from excess signal conditions is illustrated in Figures 15 and 16. The circuits make use of
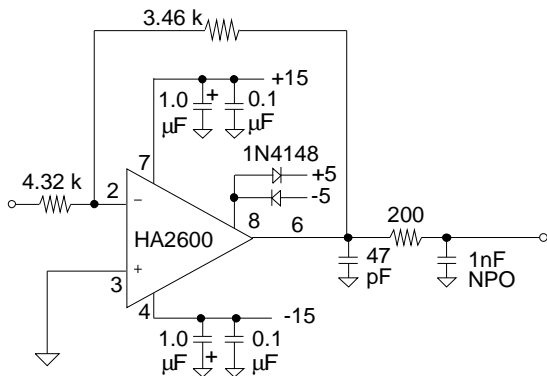

Figure 13. Instrumentation Amplifier
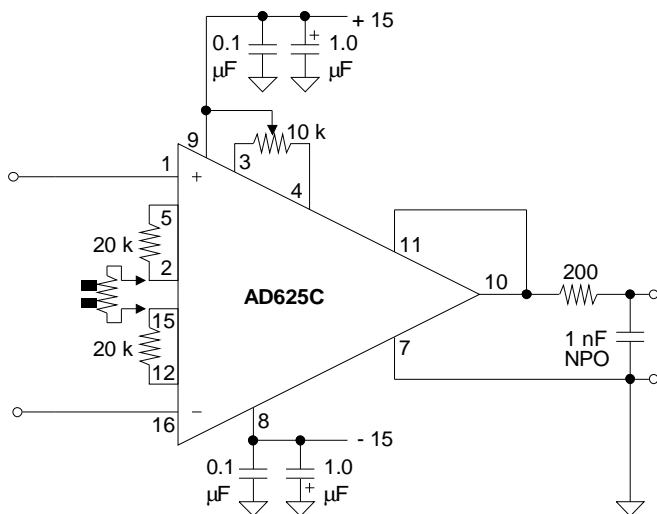
Gain	1
Input	1.5 kHz, ±4.5 Vpk
VREF	4.5 V
S/(N+D)	73.1 dB
S/D	81.5 dB*
S/PN	83.7 dB*

* Primarily 2nd harmonic

Gain	9*
Input	1.5 kHz, ±0.5 Vpk
VREF	4.5 V
S/(N+D)	74.1 dB
S/D	87.3 dB
S/PN	84.7 dB

* 5 K resistor connected

Figure 14. Compensation Pin Clamping

Gain	-0.8
Input	1.5 kHz, ±5.6Vpk
VREF	4.5 V
S/(N+D)	90.5 dB
S/D	97.0 dB
S/PN	98.1 dB

additional series resistance between the op amp and the converter to limit the amount of signal current available. The resistor is placed inside of the feedback loop of the amplifier where the loop gain of the circuit reduces the effect of the 1 kΩ resistor under normal operating conditions. When a fault condition exists, the signal output from the amplifier may attempt to exceed the power supply rails of the A/D converter. Under this condition the current into the A/D converter input will be limited to less than 10 mA by the 1 kΩ resistor.

The added 1 kΩ resistor increases the open loop output impedance of the circuit. This increase in output impedance adversely affects the effective open loop gain of the circuit when driving lower

impedance loads. Therefore, it is desirable to take advantage of op amps with higher open loop gains. Decompensated op amps offer greater gain-bandwidth products but with the restriction that they are generally specified to be stable only with higher gain configurations. For example, the OP-37 is specified for operation with a minimum gain of 5 but offers higher open loop gain than the OP-27 (about 15 dB higher at 10 kHz). The circuits in Figures 15 and 16 take advantage of the added open loop gain of the OP-37 yet still meet the requirements for stability demanded by the amplifier. At low frequencies (below 10 kHz) the loop gain of the circuit reduces the effect of the 1 kΩ resistor significantly. At the same time the effective load to the amplifier output (including the 1 kΩ output resistor) is dominated by the
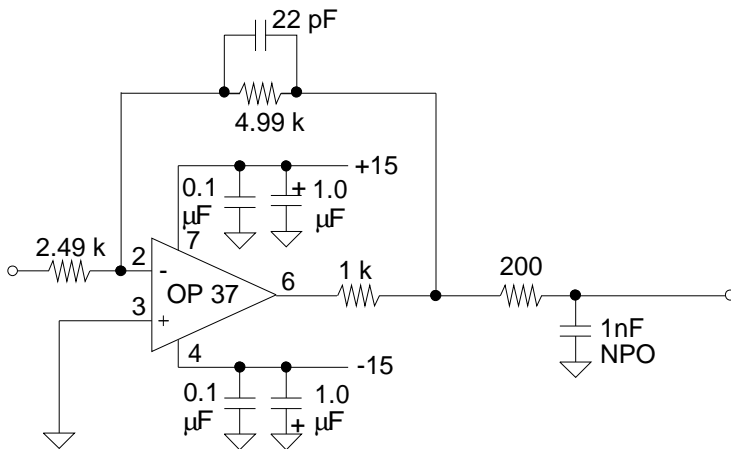
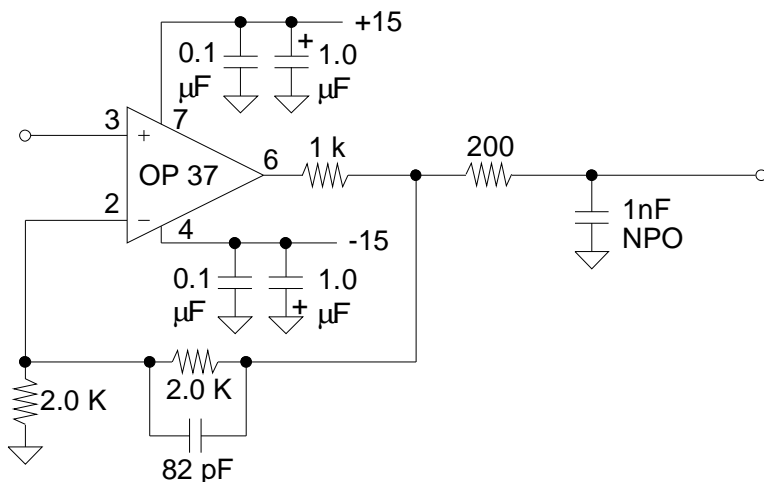| Gain	-2
Input	1.5kHz, ±9Vpk
VREF	4.5 V
S/(N+D)	91.2 dB
S/D	97.9 dB
S/PN	99.2 dB

Figure 15. Inverting Amplifier with current limiting

feedback resistor. At high frequencies (above 1 MHz) the impedance of the 1 nF capacitor in the output filter begins to look like a short circuit therefore the load seen by the op amp circuit is dominated by the 200 Ω resistor. At the higher frequencies the open loop gain of the op amp is decreasing. The corresponding reduction in loop gain allows the effect of 1 kΩ resistor to begin to take effect, increasing the output impedance to the feedback node. The combined effect of the higher output impedance due to the 1 kΩ resistor and the loading effect of the 200 Ω resistor causes an effective loop gain reduction of about 200/(1000 + 200) or a factor of 6. This gain reduction in combination with the phase compensation of the feedback capacitor allows the circuit to maintain stability while it also provides current limiting under fault conditions.

This application note has discussed the making of a good buffer circuit and has illustrated several examples with relevant test data. For further information on design and dynamic testing of amplifier circuits refer to the following references.

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Gain	+2	
Input	1.5 kHz,	±2.25Vpk
VREF	4.5 V	
S(N+D)	92.0 dB	
S/D	100.4 dB	
S/PN	102.8 dB	

Figure 16. Noninverting Amplifier with Current Limiting