A Cirrus Logic Company

AN08

Application Note

A Collection of Application Hints for the CS501X Series of A/D Converters

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- Jam ADC into Coarse Charge for High Slew Signals
- Single Control Input Acts as a "Start Convert" Command
- Synchronizing Multiple CS501X Series A/D Converters
- ±5V Input Signal Range Operation

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Here are several application hints which extend the flexibility of the CS501X series of A/D converters.

Jam ADC Into Coarse Charge For High Slew Signals

The CS501X family of A/D converters have within their capacitor-based architecture a track-and-hold function. Upon completing a conversion the A/D converter immediately begins to track the input signal. The design is such that the input signal is buffered (internal to the A/D) from the capacitor array for six cycles of the master clock. Then the buffer is bypassed and the array is directly connected to the AIN pin of the converter. This allows the converter to settle to its final value within the accuracy specifications. The period of time that the buffer is connected is known as the coarse charge time. The time when the buffer is bypassed to sample the input signal directly is known as fine charge time. Slew rate capability during coarse charge time is much greater than the slew rate in fine charge. Any step changes of the input signal should occur either prior to or during the coarse charge time. Under normal operation, once the converter has completed the coarse charge time and entered into the fine charge time it will stay in the fine charge state until the $\overline{\text{HOLD}}$ input goes low. When $\overline{\text{HOLD}}$ goes low the charge on the capacitor array is immediately trapped and conversion begins.

In applications which exhibit step changes in the input signal, it is not desireable that the converter remain waiting in the fine charge mode (with its slower slew rate capability). Extending the coarse charge time allows the ADC to track high slew signals.

Figure 1 depicts the logic by which the master clock to the converter is stopped during the coarse charge time to lock the converter into coarse charge. At the end of each conversion the End of Conversion ($\overline{\text{EOC}}$) signal indicates the

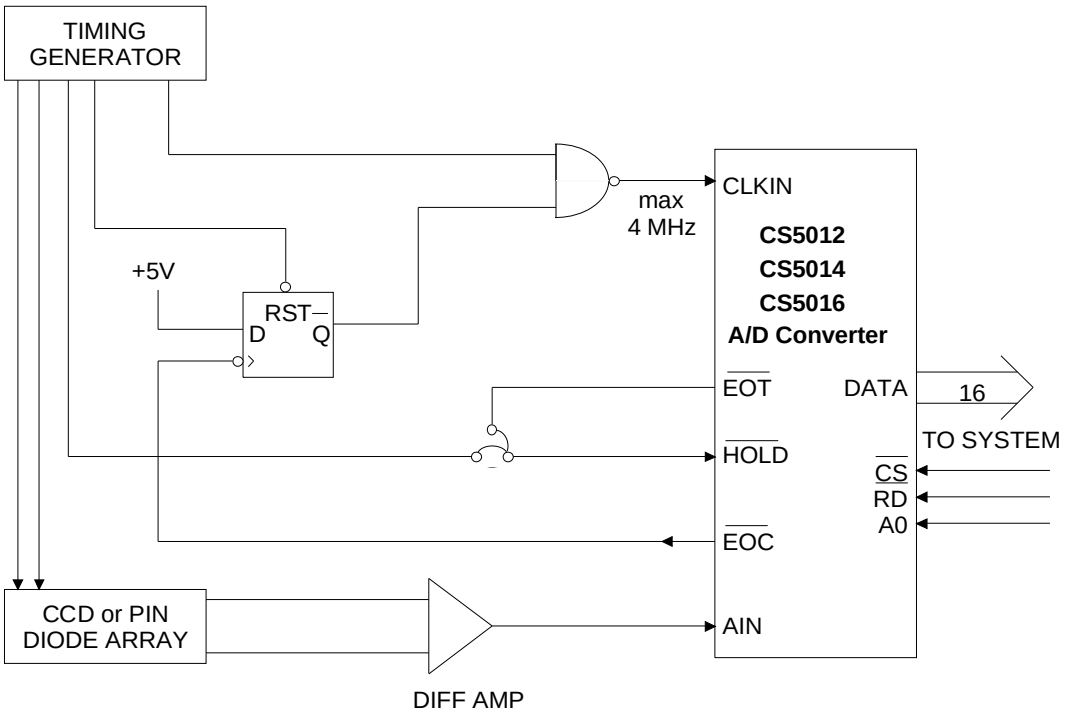


Figure 1. Sample Logic Jams Converter into High Slew Rate Mode

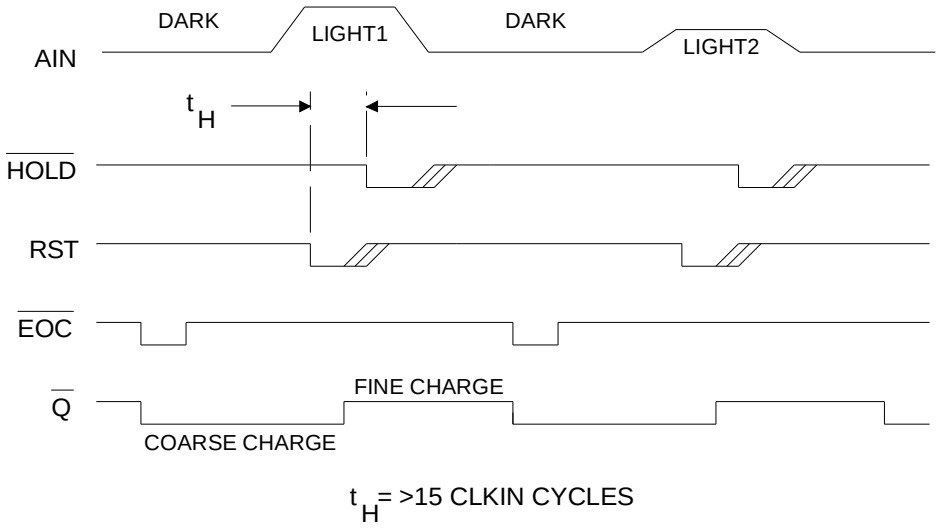


Figure 2. Extending Coarse Charge Time Allows Tracking of Dark to Light Transition

end of a conversion and the beginning of a coarse charge time. $\overline{EOC}$ falling toggles the flip-flop, causing its $\overline{Q}$ output to go low. This jams the NAND gate output high which locks the converter into the coarse charge mode until the timing generator circuitry resets the flip-flop.

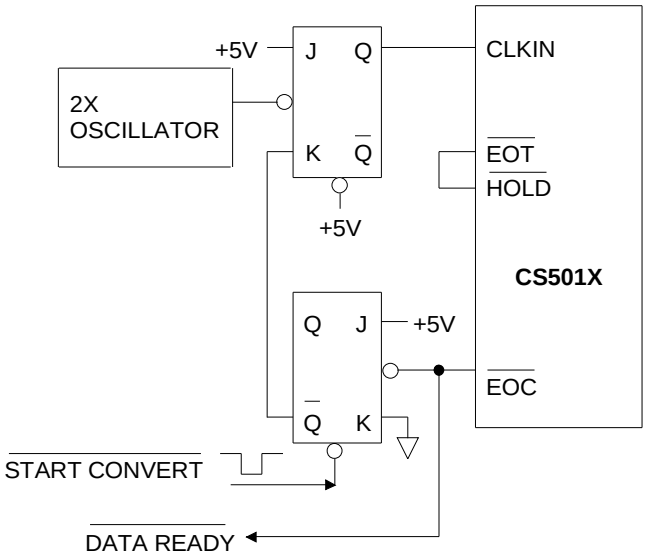


Figure 3.Coarse Charge Jamming with "StartConvert" Control

Figure 2 illustrates the timing of the various signals of the circuit in Figure 1. CCD or PIN diode array outputs exhibit step changes in their signal levels as each array element is selected for output. After each conversion the converter is stopped in the coarse charge mode until the video output signal from a particular element of the sensor array is stable. The clock to the A/D converter is then restarted. The converter then proceeds through the coarse and fine charge times and awaits a $\overline{HOLD}$ signal. If the $\overline{EOT}$ output of the converter is tied to the $\overline{HOLD}$ conversion will begin as soon as the track time is complete.

While this coarse charge jamming circuit is designed to operate with the CS501X series of converters, note that the CS5101 A/D converter offers a CRS/$\overline{FIN}$ (coarse/fine) pin as an input to allow user control of the tracking mode.

Creating a Single "Track, Hold, and Convert" Command

The coarse charge jamming circuitry of Figure 1 is altered to allow a single control line to initiate a sample and convert sequence. First, the $\overline{EOT}$ output from the converter must be directly tied to

$\overline{\text{HOLD}}$ input. This connection will enable the converter to initiate a conversion upon completion of 9 clock cycles of fine charge (the minimum fine charge time necessary for adequate settling).

At the end of each conversion the $\overline{\text{EOC}}$ signal will toggle the flip-flop and lock the converter in coarse charge. The converter will track the input signal in the coarse charge mode until the "start convert" input resets the flip-flop to restart the clock. With $\overline{\text{EOT}}$ tied to $\overline{\text{HOLD}}$ the converter will proceed through coarse charge, fine charge, and conversion at which time it will stop and await another "start convert" command. Data in the output port will remain available until a new start convert command is issued, but due to internal logic, the port cannot be read in the byte-wide (BW = 0) mode.

Figure 3 illustrates an example of the "start convert" circuitry using a dual J-K flip-flop. Note that the input clock is twice that required by the converter and that the low time of "start convert" pulse should be less than the conversion time of the converter. The "start convert" signal should be held low during calibration.

Synchronizing Multiple CS501X Series A/D Converters

Simultaneous sampling of several channels is often required. For example, in measurements of the outputs of three-axis magnetometers or three-axis inclinometers it is desireable that all three signals be simultaneously sampled and then converted. Because the CS501X converters offer very good repeatibility from part to part they can yield very good channel to channel measurement correlation even though each channel is converting with its own A/D converter.

Figure 4 illustrates how multiple CS501X series converters can be synchronized, allowing simultaneous sampling. The circuit uses a flip-flop to synchronize a reset (RST) signal common to all of the A/D converters such that the reset signal goes low on a falling edge of the master clock (CLKIN) to each converter. A common $\overline{\text{HOLD}}$ command can then be connected to all of the converters to initiate simultaneous sampling. Or, if the synchronous loopback mode of sampling is desired, the $\overline{\text{EOT}}$ output from one of the converters can be input to the $\overline{\text{HOLD}}$ inputs of all of the converters.

When several converters are galvanically isolated from the digital processing system, synchronazation is useful. The data is passed across the isolation barrier in serial form. If several converters are in the system, normally both SDATA and SCLK signals from each converter are passed across the isolation barrier. However, if the converters are synchronized, the SDATA outputs of several converters can be clocked into serial to parallel registers on the digital side by sending a single SCLK signal across the barrier.

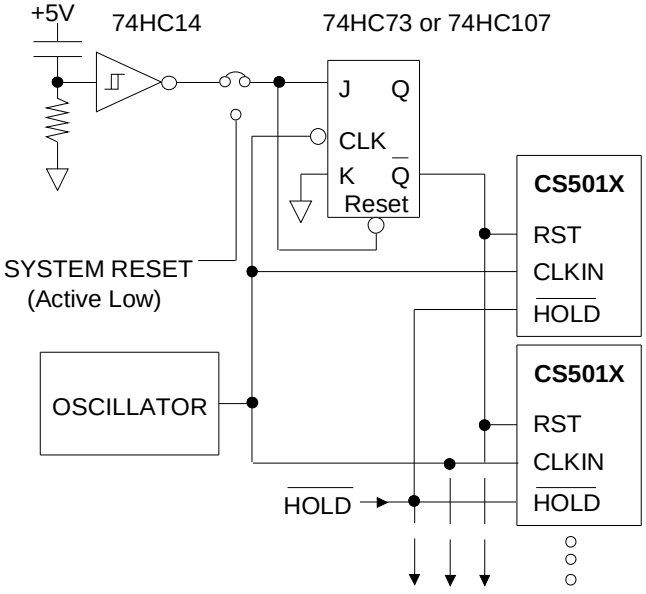


Figure 4. Controlled Reset for Synchronizatoin of Multiple Converters

± 5V Input Signal Range Operation

Some system specifications may require signal levels of ± 5 V. Operating the CS501X series of A/D converters with ± 5 V signals requires a 5 V reference and therefore the supplies have to be raised. The supplies should be adjusted to output voltages in the range from 5.3 to 5.5 volts. The positive and negative supplies should be of equal magnitude and the system connections recommended in the A/D converter data sheet should be maintained.

An easy means of achieving the proper supply voltages is to use LM317L and LM337L regulators. These devices are acceptable as the power requirements of the A/D converter are very low. See Figure 5 for the appropriate resistor values to set the regulator voltages. An alternative is to use LM78L05AC and LM79L05AC regulators with adjustment resistors to increase their output voltages. This is illustrated in Figure 6.

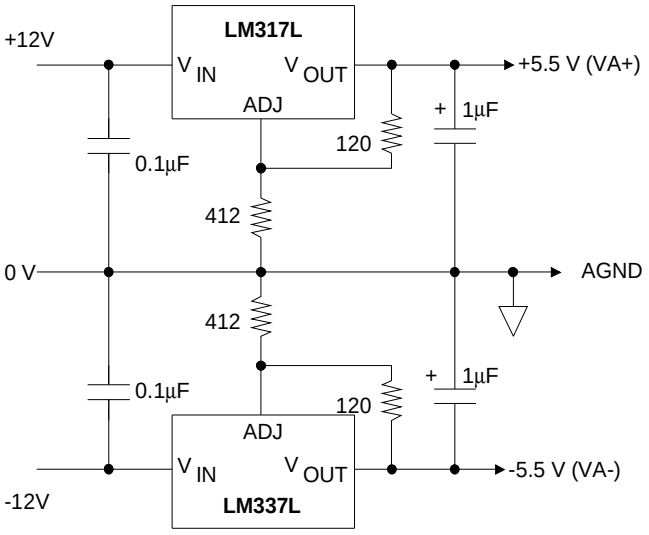


Figure 5. LM317L/LM337L Voltage Regulators

References which output 5 V require a minimum input voltage from 6.5 to 11 volts. This increased voltage is necessary to accommodate the 1 to 6 volt input to output voltage differential needed by the reference. Supply voltages of +12 V or +15 V are common. Care should be excercised to insure

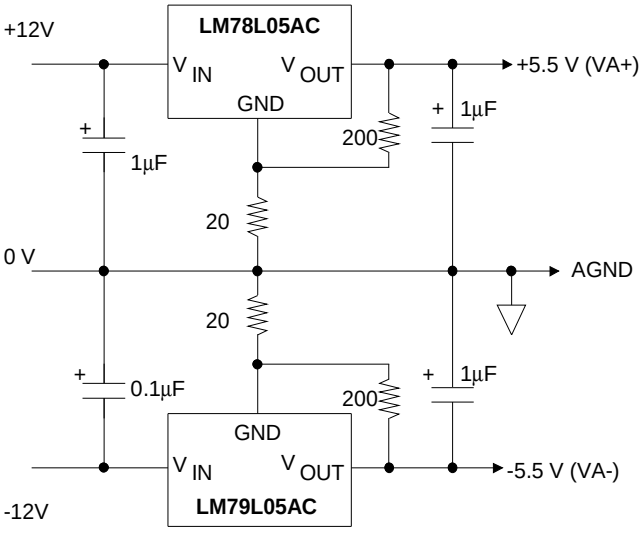
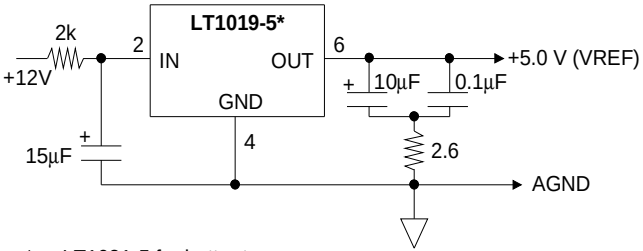


Figure 6. LM78L05/LM79L05 Voltage Regulators

that the voltage reference output does not source current into the A/D converter VREF pin before the power supplies on the A/D are established. One means of insuring this is to add an RC filter in front of the voltage reference as illustrated in Figure 7. This will delay the reference output until the regulated supplies (Figure 5 or 6) for the A/D are established.

With raised supply voltages on the A/D converter, the digital outputs will output logic 1's with a higher output voltage (V_{OH}). To accommodate this increase the digital logic in the system can use 74HC4049 or 74HC4050 logic level translators to restore the logic outputs back to the 5 V level. Alternatively, the logic system (if 74HC logic is used) can also use a supply voltage elevated to the value of the A/D supply. This problem is also eliminated if the ADC is isolated using opto-couplers.



* or LT1021-5 for better tempco.
or LT1019-4.5 for 4.5V output

Figure 7. 5Volt Reference with RC Input Delay

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